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Data Book

Analog/Digital
Bipolar/CMOS
Integrated Circuits

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Advanced and Preliminary Information

In this data book the following conventions are used in designating a data sheet "Advanced" or "Preliminary."

Advanced— indicates a product still in the design cycle, and any specifications are based on design goals only. Sample availability is indicated in the text.

Preliminary— indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and SSI should be consulted for current information.

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TELECOMMUNICATION PRODUCTS

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SSI TPD Product Selector Guide

TELECOMMUNICATIONS CIRCUITS

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SSI Telecommunications Capabilities

Silicon Systems offers a broad line of standard telecommunications circuits aimed at providing cost-effective solutions for common customer application problems. At the heart of SSi's efforts in the communications market is its pioneering work with CMOS switched capacitor filters. Our early success with the DTMF receiver has enabled us to develop a family of chips utilizing the switched capacitor filter technology.

As a trendsetter in the field, Silicon Systems is leading the way towards a whole new era of VLSI circuits for telecommunications. Our broad selection of DTMF receivers demonstrates not only technological leadership in our own semiconductor field but also our capability to anticipate the growing needs of the fast-paced telecommunications marketplace.

Here are a few completed circuits that demonstrate our broad telecommunications IC capability:

BIPOLAR

Integrated Circuit Function	Application
Audio System Receiver	Telephone Answering Machine
VHF/UHF Gain Mixer	Radio Receiver
Pulse Width Modulator	Switching Power Supply
Controller	Home Appliance
Digital Receiver	Remote Control
PCM Encoder/Decoder	Telecom System
Digital Correlator/ Integrator	Radio Telescope

MOS

Integrated Circuit Function	Application
DTMF Receiver	*Decodes Touch-Tone® Telephone Signals
300 Baud Modem	Data Transmission
1200/2400 Baud Receiver	FSK/PSK Modem
Error Corrector	Military Radio
Remote Transmitter	Telephone Answering Machine
Phoneme Based Speech Synthesizer	Text-to-Speech
Display Timing Generator	TV Sets
Video Processor	Infrared Video System
16 Channel Switching Matrix	Bank Communications System
Digital Loop Detector	Traffic Signal Control
Programmable Digital Receiver	Home Appliance Remote Control
Vocal Tract System	Speech Synthesis

PROCESSES

Silicon Systems offers circuits in junction-isolated, bipolar, single and double-layer metal. Plus, SSi has a CMOS capability that includes not only a metal-gate process but also a silicon-gate process that produces circuits packed with more functions in a smaller size for high-speed, low-power performance. These are the most popular and reliable processes in the two basic technologies, and SSI's advanced ultra-clean wafer fab produces higher yields than ordinary facilities.

PRODUCT QUALITY

Silicon Systems has made a major investment in product test and in-line quality control equipment. For example, a state-of-the-art LTX CP80 is used for functional and parametric testing of sophisticated analog, digital, and combination A/D circuits. In this way, SSi is dedicated to the delivery of complex VLSI circuits to meet the incoming quality level you require.

CUSTOMER SERVICE

Silicon Systems provides individualized service for every customer. Our Customer Service Department is dedicated to responsive service and is staffed with personnel trained to consider our customers' needs as their most urgent requirement. Product quality and service are both viewed as cornerstones for SSi's continued growth.

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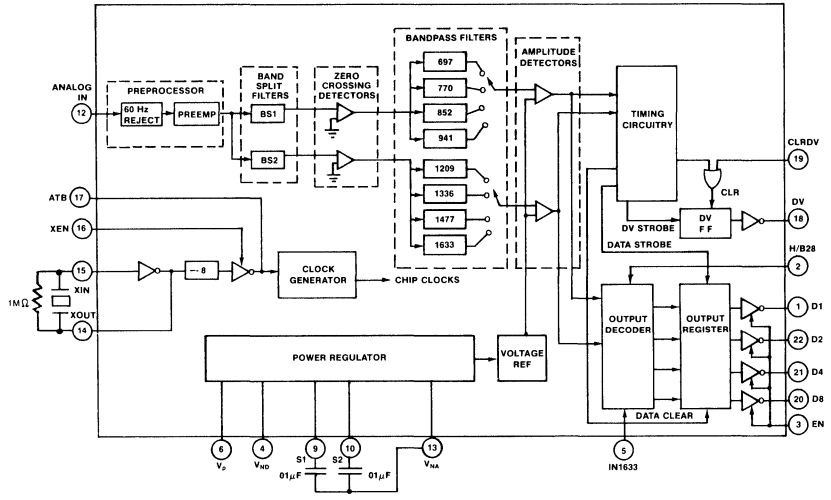
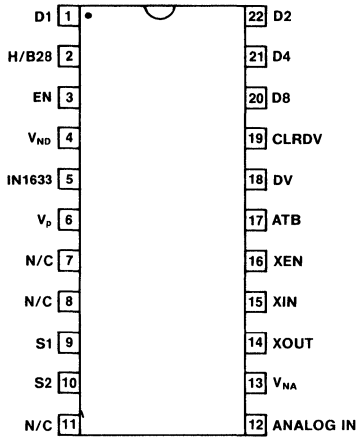
INNOVATORS IN INTEGRATION

Integrated DTMF Receiver SSI 201

Data Sheet



SSI 201 Block Diagram



SSI 201 Pin Out
(Top View)

FEATURES

- **Central office quality**
- **NO front-end band-splitting filters required**
- **Single, low-tolerance, 12-volt supply**
- **Detects either 12 or 16 standard DTMF digits**
- **Uses inexpensive 3.579545-MHz crystal for reference**
- **Excellent speech immunity**
- **22-pin DIP package for high system density**
- **Output in either 4-bit hexadecimal code or binary coded 2 of 8**
- **Synchronous or handshake interface**
- **Three-state outputs**

DESCRIPTION

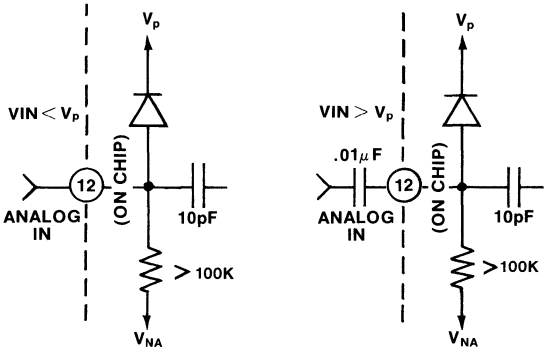
The SSI 201 is a complete Dual Tone Multiple Frequency (DTMF) receiver detecting a selectable group of 12 or 16 standard digits No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.58-MHz television "colorburst" crystal (for frequency reference) and two low-tolerance bypass capacitors. Extremely high system density is made possible by using the clock output of a crystal connected SSI 201 receiver to drive the time bases of additional receivers. The SSI 201 is a monolithic integrated circuit fabricated with low-power, complementary symmetry MOS (CMOS) processing. It requires only a single low tolerance voltage supply and is packaged in a standard 22 pin DIP.

The SSI 201 employs state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semiconductor process The analog input is pre-processed by 60-Hz reject and band splitting filters and then hard-limited to provide AGC Eight bandpass filters detect the individual tones The digital post-processor times the tone durations and provides the correctly coded digital outputs Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures

Integrated DTMF Receiver
SSI 201

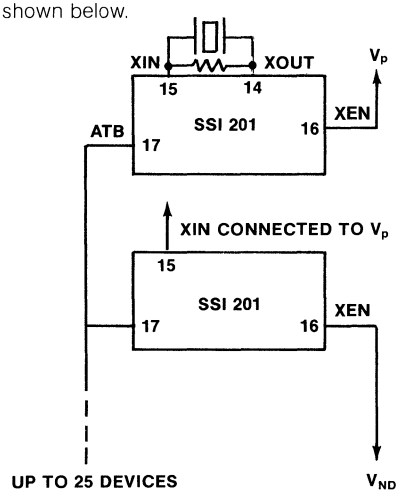
ANALOG IN (pin 12)

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated below.



CRYSTAL OSCILLATOR

The SSI 201 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal The crystal oscillator is enabled by tying XEN (pin 16) high. The crystal is connected between XIN (pin 15) and XOUT (pin 14) A 1 MEGΩ 10% resistor is also connected between these pins In this mode, ATB (pin 17) is a clock frequency output. Other SSI 201's may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device XIN and XEN of the auxiliary devices must then be tied high and low respectively Twenty-five devices may run off a single crystal-connected SSI 201 as shown below.



H/B28 (pin 2)

This pin selects the format of the digital output code When H/B28 is tied high, the output is hexadecimal When tied low, the output is binary coded 2 of 8 The table below describes the two output codes

	Hexadecimal				Binary Coded 2 of 8			
Digit	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

IN1633 (pin 5)

When tied high, this pin inhibits detection of tone pairs containing the 1633-Hz component For detection of all 16 standard digits, IN1633 must be tied low

OUTPUTS D1, D2, D4, D8 (pins 1, 22, 21, 20) and EN (pin 3)

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedence) when disabled by pulling EN low These digital outputs provide the code corresponding to the detected digit in the format programmed by the H/B28 pin The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed

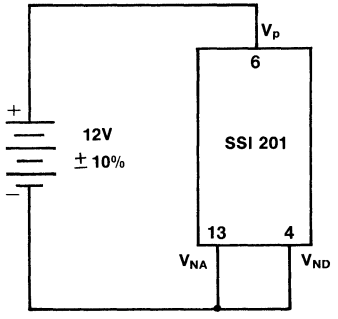
DV (pin 18) and CLRDV (pin 19)
DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, D8 DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier

INTERNAL BYPASS PINS
S1, S2 (pins 9, 10)
In order for the SSI 201 DTMF Receiver to function properly, these pins must be bypassed to V_{NA} with 0 01 μF ±20% capacitors

POWER SUPPLY PINS
V_P (pin 6) V_{NA} (pin 13) V_{ND} (pin 4)

The analog (V_{NA}) and digital (V_{ND}) supplies are brought out separately to enhance analog noise immunity on the chip. V_{NA} and V_{ND} should be connected externally as shown below

12V SYSTEM



N/C PINS (pins 7, 8, 11)
These pins have no internal connection and may be left floating.

DTMF DIALING MATRIX

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

Note Column 3 is for special applications and is not normally used in telephone dialing

DETECTION FREQUENCY

Low Group f_o	High Group f_o
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

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ABSOLUTE MAXIMUM RATINGS*

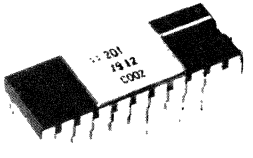
DC Supply Voltage V_p ..... +16 V
(Referenced to V_{NA}, V_{ND})
Operating Temperature..... -40°C to +85°C Ambient
Storage Temperature.....-65°C to 150°C
Power Dissipation (25°C).....1 W
(Derate above T_A = 25°C @ 10mW/°C)

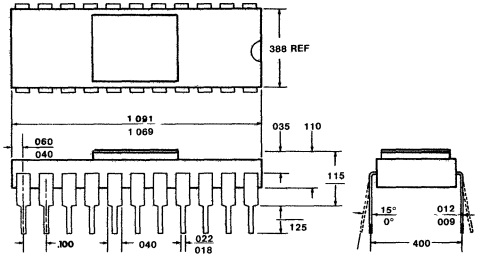
Input Voltage .....(V_p + 5V) to (V_{ND} - .5V)
(All inputs except ANALOG IN)
ANALOG IN Voltage.....(V_p + 5V) to (V_p - 22V)
DC Current into any Input.....±1.0mA
Lead Temperature ..... 300°C
(soldering, 10 sec.)

*Operation above absolute maximum ratings may damage the device
Note All SSI 201 unused inputs must be connected to V_p or V_{ND}, as appropriate

ELECTRICAL CHARACTERISTICS ($-40°C \leq T_A \leq +85°C$, $V_p - V_{ND} = V_p - V_{NA} = 12V \pm 10\%$)

Parameter	Conditions	Min	Typ	Max	Units
Frequency Detect Bandwidth		±(1.5 + 2 Hz)	±2.3	± 3.0	% of f_O
Amplitude for Detection	each tone	-24		+6	dBm referenced to 600Ω
Minimum Acceptable Twist	twist = high tone / low tone	-8		+4	dB
Detection Time		20	25	40	ms
Pause Time		25	32	40	ms
60-Hz Tolerance				2	Vrms
Dial Tone Tolerance	"precise" dial tone			0 dB	dB referenced to lower amplitude tone
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs (except XOUT)	"0" level, 750μA load "1" level, 750μA load	V_{ND} V_p - 0.5		V_{ND} + 0.5 V_p	V V
Digital Inputs (except H/B28, XEN)	"0" level "1" level	V_{ND} V_p - 3(V_p - V_{ND})		V_{ND} + 3(V_p - V_{ND}) V_p	V V
Digital Inputs H/B28, XEN	"0" level "1" level	V_{ND} V_p -1		V_{ND} +1 V_p	V V
Power Supply Noise	wide band			25	mV p-p
Supply Current	T_A = 25°C $V_p - V_{NA} = V_p - V_{ND} = 12V \pm 10\%$		29	50	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB referenced to lowest amplitude tone
Input Impedence	$V_p \geq V_{in} \geq V_p$-22	100KΩ//15pF			





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SSI 202/203 5V Low-Power DTMF Receiver

Data Sheet

DESCRIPTION

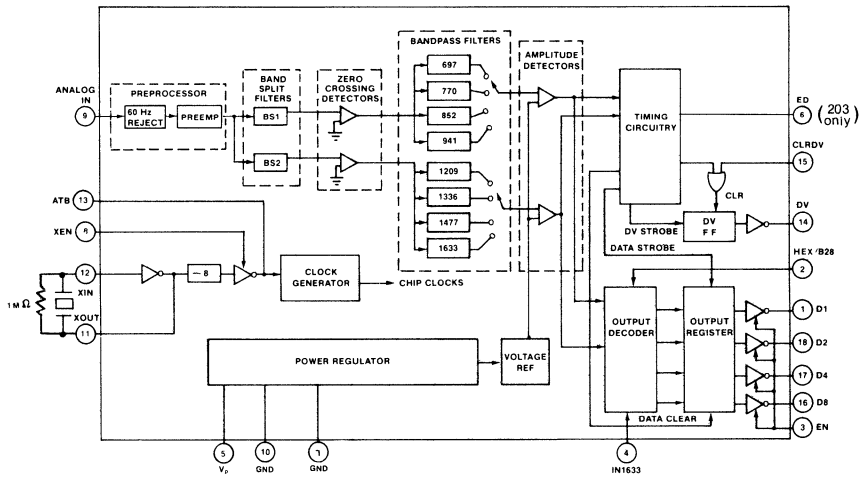
The SSI 202 and 203 are complete Dual Tone Multiple Frequency (DTMF) receivers detecting a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.58-MHz television "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is made possible by using the clock output of a crystal connected SSI 202 or 203 receiver to drive the time bases of additional receivers. Both are monolithic integrated circuits fabricated with low-power, complementary symmetry MOS (CMOS) processing. They require only a single low tolerance voltage supply and are packaged in a standard 18 pin plastic DIP.

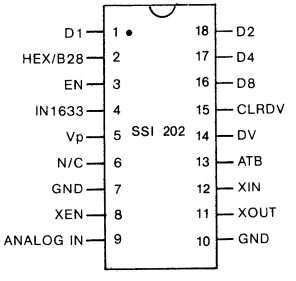
The SSI 202 and 203 employ state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is pre-processed by 60-Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

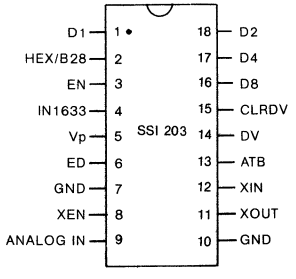
FEATURES

- **Central office quality**
- **NO front-end band-splitting filters required**
- **Single, low-tolerance, 5-volt supply**
- **Detects either 12 or 16 standard DTMF digits**
- **Uses inexpensive 3.579545-MHz crystal for reference**
- **Excellent speech immunity**
- **Output in either 4-bit hexadecimal code or binary coded 2 of 8**
- **18-pin DIP package for high system density**
- **Synchronous or handshake interface**
- **Three-state outputs**
- **Early detect output (SSI 203 only)**

SSI 202/203 Block Diagram





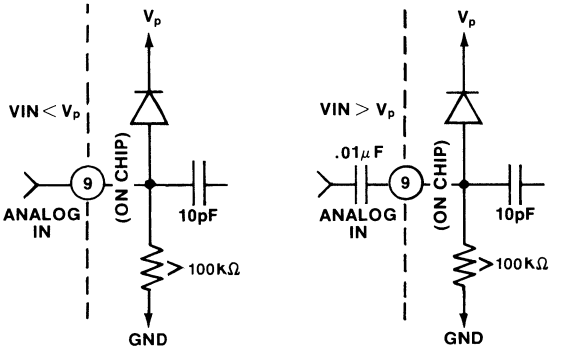


Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

ANALOG IN

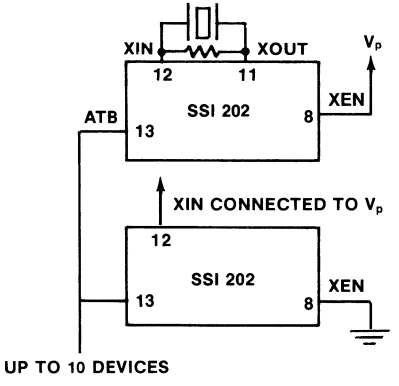
This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated below.



The SSI 202 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental

CRYSTAL OSCILLATOR

The SSI 202 and 203 contain an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 202's (or 203's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 202 or 203 as shown below.



HEX /B28

This pin selects the format of the digital output code When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2 of 8 The table below describes the two output codes

	Hexadecimal				Binary Coded 2 of 8			
Digit	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633-Hz component For detection of all 16 standard digits, IN1633 must be tied low

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedence) when disabled by pulling EN low These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier

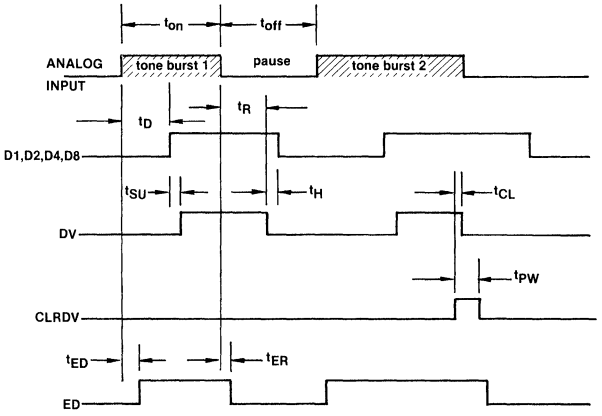
ED (SSI 203 only)

The ED output goes high as soon as the SSI 203 begins to detect a DTMF tone pair and falls when the 203 begins to detect a pause. The D1, D2, D4, and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high

N/C PINS

These pins have no internal connection and may be left floating

SSI 202/203 TIMING



DTMF DIALING MATRIX

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

Note Column 3 is for special applications and is not normally used in telephone dialing

DETECTION FREQUENCY

Low Group f_o	High Group f_o
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
TONE TIME. for detection	t_{ON}	40	—	—	ms
for rejection	t_{ON}	—	—	20	ms
PAUSE TIME: for detection	t_{OFF}	40	—	—	ms
for rejection	t_{OFF}	—	—	20	ms
DETECT TIME	t_D	25	—	46	ms
RELEASE TIME	t_R	35	—	50	ms
DATA SETUP TIME	t_{SU}	7	—	—	µs
DATA HOLD TIME	t_H	4.2	—	5.0	ms
DV CLEAR TIME	t_{CL}	—	160	250	ns
CLRDV pulse width	t_{PW}	200	—	—	ns
ED Detect Time	t_{ED}	7	—	22	ms
ED Release Time	t_{ER}	2	—	18	ms
OUTPUT ENABLE TIME C_L = 50pF R_L = 1KΩ	—	—	200	300	ns
OUTPUT DISABLE TIME C_L = 35pF R_L = 500Ω	—	—	150	200	ns
OUTPUT RISE TIME C_L = 50pF	—	—	200	300	ns
OUTPUT FALL TIME C_L = 50pF	—	—	160	250	ns

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ABSOLUTE MAXIMUM RATINGS*

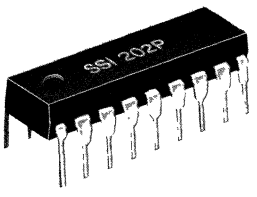
DC Supply Voltage V_p ..... +7 V
Operating Temperature..... -40°C to +85°C Ambient
Storage Temperature..... -65°C to 150°C
Power Dissipation (25°C) ..... 65 mW
(Derate above T_A = 25°C @ 6.25 mW/°C)

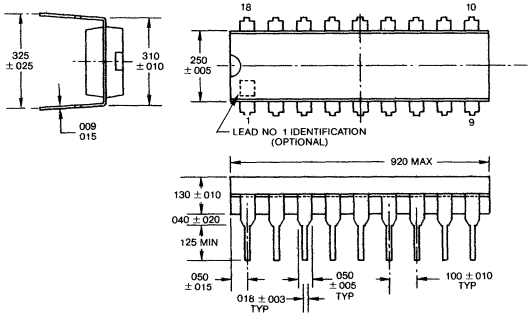
Input Voltage ..... (V_p + .5V) to - .5V
(All inputs except ANALOG IN)
ANALOG IN Voltage..... (V_p + 5V) to (V_p - 10 V)
DC Current into any Input..... ±1.0mA
Lead Temperature ..... 300°C
(soldering, 10 sec.)

*Operation above absolute maximum ratings may damage the device
Note All SSI 202/203 unused inputs must be connected to V_p or Gnd, as appropriate

ELECTRICAL CHARACTERISTICS ($-40°C \leq T_A \leq +85°C$, $V_p = 5V \pm 10\%$)

Parameter	Conditions	Min	Typ	Max	Units
Frequency Detect Bandwidth		±(1 5 + 2 Hz)	±2 3	± 3 5	% of f_O
Amplitude for Detection	each tone	-32		-2	dBm referenced to 600 Ω
Minimum Acceptable Twist	twist = high tone / low tone	-10		+10	dB
60-Hz Tolerance				0 8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB referenced to lower amplitude tone
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs (except XOUT)	"0" level, 400 μA load "1" level, 200 μA load	0 V_p - 0 5		0 5 V_p	V V
Digital Inputs	"0" level "1" level	0 0 7V_p		0 3V_p V,	V V
Power Supply Noise	wide band			10	mV p-p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB referenced to lowest amplitude tone
Input Impedence	$V_p \geq V_{in} \geq V_p$-10	100 kΩ // 15pF			





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SSI 204
5V Low Power DTMF Receiver

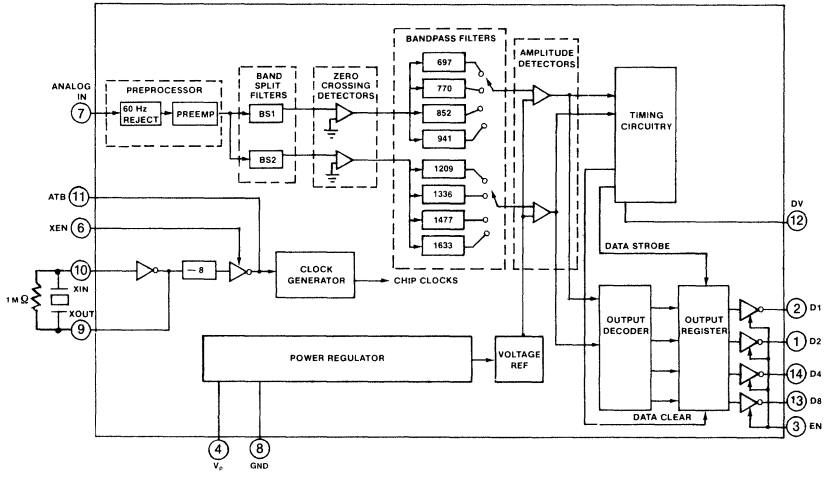
Data Sheet

DESCRIPTION

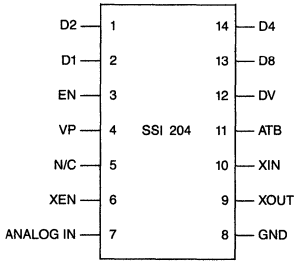
The SSI 204 is a complete Dual Tone Multiple Frequency (DTMF) receiver that detects all 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.58-MHz television "color-burst" crystal for frequency reference and a bias resistor. An Alternate Time Base (ATB) is provided to permit operation of up to 10 SSI 204's from a single crystal. The SSI 204 employs state-of-the-art "switched-capacitor" filter technology, resulting in approximately 40 poles of filtering, and digital circuitry on the same CMOS chip. The analog input signal is pre-processed by 60-Hz reject and band split filters and then zero-cross detected to provide AGC. Eight bandpass filters detect the individual tones. Digital processing is used to measure the tone and pause durations and to provide output timing and decoding. The outputs interface directly to standard CMOS circuitry and are three-state enabled to facilitate bus-oriented architectures.

FEATURES

- **Intended for applications with less requirements than the SSI 202**
- **14-Pin plastic DIP for high system density**
- **NO front-end band splitting filters required**
- **Single low-tolerance 5-volt supply**
- **Detects all 16 standard DTMF digits**
- **Uses inexpensive 3.579545-MHz crystal**
- **Excellent speech immunity**
- **Output in 4-bit hexadecimal code**
- **Three-state outputs for microprocessor interface**



Block Diagram



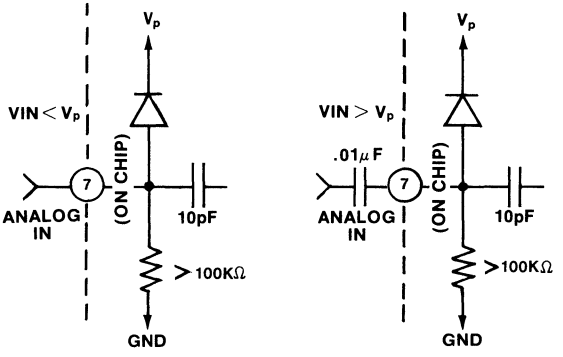
SSI 204 Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

SSI 204
5V Low Power Subscriber DTMF Receiver

ANALOG IN

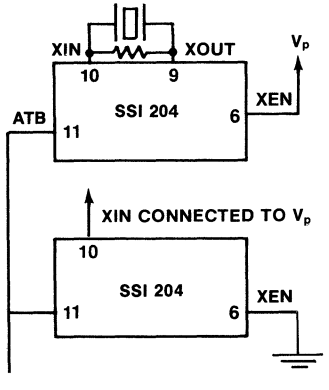
This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated below.



The SSI 204 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 204 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 204's (or 202's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 204 (or 202) as shown below.



UP TO 10 DEVICES

OUTPUTS D1, D2, D4, D8, and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the hexadecimal code corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed. The table below describes the hexadecimal codes.

	OUTPUT CODE			
Digit	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

DV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, D8. DV remains high until a valid pause occurs.

N/C PIN

This pin has no internal connection and may be left floating.

DTMF DIALING MATRIX

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

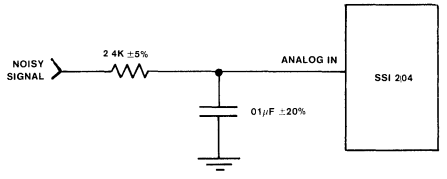
Note: Column 3 is for special applications and is not normally used in telephone dialing

DETECTION FREQUENCY

Low Group f_o	High Group f_o
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

APPLICATION NOTES

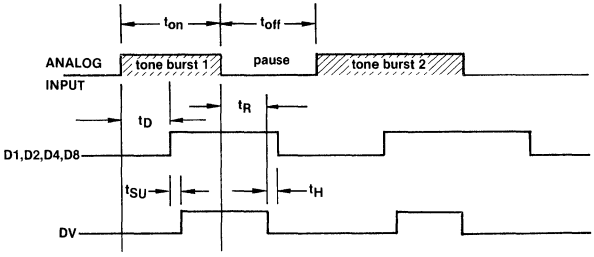
The SSI 204 will tolerate total input rms noise up to 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to the SSI 204 unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28kHz, the simple RC filter as shown below may be employed to band limit the incoming signal.



Filter for use in extreme high frequency input noise environment

Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case leave XOUT floating.

SSI 204 TIMING



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
TONE TIME· for detection	t_{ON}	40	—	—	mS
for rejection	t_{ON}	—	—	20	mS
PAUSE TIME. for detection	t_{OFF}	40	—	—	mS
for rejection	t_{OFF}	—	—	20	mS
DETECT TIME	t_D	25	—	46	mS
RELEASE TIME	t_R	35	—	50	mS
DATA SETUP TIME	t_{SU}	7	—	—	μS
DATA HOLD TIME	t_H	42	—	50	mS
OUTPUT ENABLE TIME C_L = 50pF R_L = 1KΩ	—	—	200	300	nS
OUTPUT DISABLE TIME C_L = 35pF R_L = 500Ω	—	—	150	200	nS
OUTPUT RISE TIME C_L = 50pF	—	—	200	300	nS
OUTPUT FALL TIME C_L = 50pF	—	—	160	250	nS

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V_p ..... +7 Volts

Operating Temperature ..... −40°C to +85°C Ambient

Storage Temperature ..... −65°C to 150°C

Power Dissipation (25°C) ..... 65 mW
(Derate above T_A = 25°C @ 6.25 mW/°C)

Input Voltage ..... (V_p + 0.5V) to − 0.5V
(all inputs except ANALOG IN)

ANALOG IN Voltage ..... (V_p + 0.5V) to (V_p −10V)

DC Current into any Input ..... ±1.0mA

Lead Temperature ..... 300°C
(soldering, 10 sec.)

*Operation above absolute maximum ratings may damage the device.

Note All SSI 204 unused inputs must be connected to V_p or Gnd as appropriate

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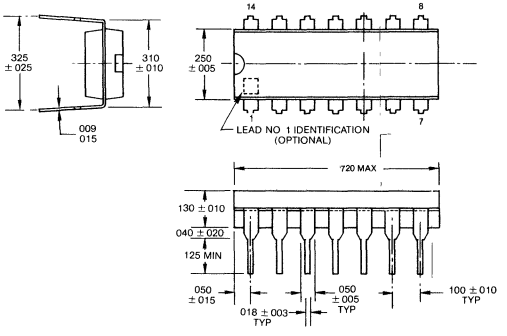
ELECTRICAL CHARACTERISTICS ($-40°C \leq T_A \leq +85°C$, $V_p = 5V \pm 10\%$)

Parameter	Conditions	Min	Typ	Max	Units
Frequency Detect Bandwidth		±(1 5 + 2 Hz)	±2 3	± 3 5	% of f_O
Amplitude for Detection	each tone	-32		-2	dBm referenced to 600 Ω
Minimum Acceptable Twist	twist = high tone / low tone	-8		+4	dB
60-Hz Tolerance				0 8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB referenced to lower amplitude tone
Talk-Off	MITEL tape #CM 7290		2		hits
Digital Outputs (except XOUT)	"0" level, 400 μA load "1" level, 200 μA load	0 V_p - 0 5		0 5 V_p	V V
Digital Inputs	"0" level "1" level	0 0 7V_p		0 3V_p V_p	V V
Power Supply Noise	wide band			10	mV p-p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB referenced to lowest amplitude tone
Input Impedance	$V_p \geq V_{in} \geq V_p$-10V	100KΩ// 15pF			



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SSI 207 Integrated MF Receiver

Preliminary Data Sheet

GENERAL DESCRIPTION

The SSI 207 is a complete Multi-Frequency (MF) receiver that can detect all 15 tone-pairs, including ST and KP. This receiver is intended for use in equal access applications and thus meets Bell and CCITT R1 central office register signalling specifications.

No anti-alias filtering is needed if the input signal is band-limited to 26 KHz. The only external component required is an inexpensive television "color burst" 3.58 MHz crystal.

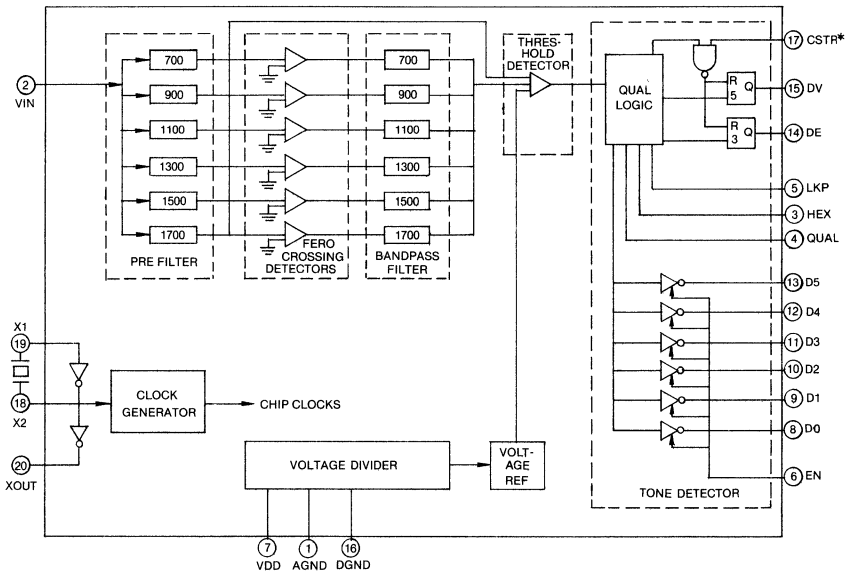
The SSI 207 employs state-of-the-art switched capacitor filters in CMOS technology. The receiver consists of a bank of channel-separation bandpass filters followed by zero-crossing detectors and frequency-measurement bandpass filters, an amplitude check circuit, a timer and decoder circuit, and a clock generator. The device does not attempt to identify strings of digits by the KP (key pulse) and ST (stop) tone pairs.

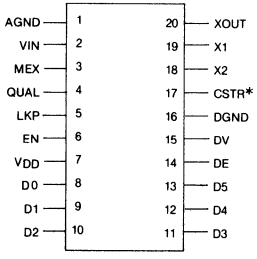
The outputs interface directly with standard DMOS or TTL circuitry and are three-state enabled to facilitate bus-oriented architecture.

FEATURES

- **Meets Bell and CCITT R1 specifications.**
- **20-pin plastic DIP.**
- **Single low-tolerance 5V supply.**
- **Detects all 15 tone-pairs including ST and KP**
- **Long KP capability**
- **Built-in amplitude discrimination.**
- **Excellent noise tolerance.**
- **Outputs in either "n of 6" or hexadecimal code.**
- **Three-state outputs, CMOS-compatible and TTL-compatible.**

SSI 207 Block Diagram

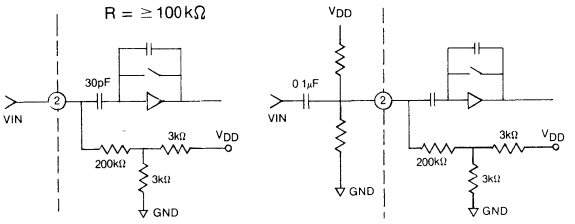




Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

VIN
This pin accepts the analog input. It is internally biased to half the supply and is capacitively coupled to the channel separation filters. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated below.



Crystal Oscillator
The SSI 207 contains an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television "color-burst" crystal. The on-chip clock signals are generated based on the oscillator. The crystal is connected between X1 and X2. X-OUT is a 3.58 MHz square wave capable of driving other circuits as long as the capacitive load does not exceed 50 pF.

The digital output format is neither "n of 6" or 4-bit hexadecimal.

DV : Data Strobe
DE . Data Error Strobe
DO to D5 : Tristate Digital Outputs

n of 6 MODE (HEX pulled low)
Whenever a valid 2 of 6 code has been recognized, the DV strobe rises. It remains high until the code goes away, or the CSTR* line is activated. It will not reactivate until a new code is detected. Whenever an invalid 2 of 6 code is recognized, (1 of 6, 3 of 6, etc.) the DE strobe rises to indicate a transmission error. The DE strobe remains high until all errors stop, a valid tone pair is detected, or the CSTR* line is activated. Once cleared by CSTR, it will not reactivate until a new invalid condition is detected. The DE and DV strobes will never be high simultaneously.

The off-chip output register can be clocked by either the rising or falling edge of the strobe. The outputs will be cleared to zero when no valid tone is present.

In the "n of 6" mode (HEX pulled low), each output represents one of the six frequencies according to the following table:

Frequency	Output Pin
700	D0
900	D1
1100	D2
1300	D3
1500	D4
1700	D5

HEX MODE (HEX pulled high)
In the "hex" mode, D0 to D3 provide a 4-bit code identifying one of the 15 **valid** tone combinations according to the following table:

Channels	Tone Pair Freq.	Name	D3	D2	D1	D0
0-1	700, 900	1	0	0	0	1
0-2	700, 1100	2	0	0	1	0
1-2	500, 1100	3	0	0	1	1
0-3	700, 1300	4	0	1	0	0
1-3	900, 1300	5	0	1	0	1
2-3	1100, 1300	6	0	1	1	0
0-4	700, 1500	7	0	1	1	1
1-4	900, 1500	8	1	0	0	0
2-4	1100, 1500	9	1	0	0	1
3-4	1300, 1500	0	1	0	1	0
2-5	1100, 1700	KP	1	0	1	1
4-5	1500, 1700	ST	1	1	0	0
1-5	900, 1700	ST1	1	1	0	1
3-5	1300, 1700	ST2	1	1	1	0
0-5	700, 1700	ST3	1	1	1	1
	any other signal	-	0	0	0	0

NOTE In the hex mode, D4 = DE and D5 = DV

The outputs will be cleared to zero when no valid tone pair is present.

LKP
The KP timer control. When high, the KP pulse must be longer than the other tone pairs before it will be detected. When low, the KP pulse is treated as any other pulse.

QUAL
Enables tone pair qualification. When low, the threshold detector outputs are passed to the data outputs (DO-D5), without validation, in the format selected by the HEX pin. These outputs, plus strobes DV and DE, are updated once per 2.3 ms frame. (DV and DE represent "2-of-6" indicators in this mode). Note that the strobes will cycle once per frame (even when the inputs are stable). As always, data changes only when both strobes are low.

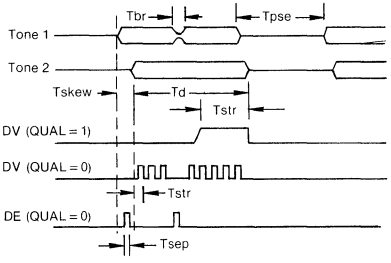
CSTR*
This input clears both the DV and DE strobes. After CSTR* is released, the strobes will remain low until a new detect (or error) occurs. The output data is latched by CSTR* and will not change while CSTR* is low, even in the event that a new detect is qualified internally. (Note that improper use of CSTR* may result in missed detects.

EN*
The tristate enable control — When low, the DO-D5 outputs are in the low impedence state. In an interrupt oriented microprocessor interface, EN* and CSTR* will often be tied together to provide automatic reset of the strobes when the output data is enabled.

DC Specifications ($0°C \leq TA \leq 70°C$, $V_{DD} = 5V \pm 10\%$)

Rating	Symbol	Min.	Max.	Unit
Supply Current	Idd	—	20	mA
Output Logic 0	Vol	—	—	—
Iol = 8mA	—	—	0.5	V
Iol = 1mA	—	—	0.4	V
Output Logic 1	Voh	—	—	—
Ioh = −4mA	—	VDD-1.0	—	V
Ioh = −1mA	—	VDD-0.5	—	V
Input Logic 1	Vih	2.0	—	V
Input logic 0	Vil	—	0.8	V
Analog Input Impedance (Input between VDD and AGND)	Zin	100k/30pF	—	Ω
Digital Input Current (Input between VDD and OGND)	Iin	−50	50	μA

SSI 207 Timing



Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
TONE DETECTION	Td	—	—	—
KP (LKP = VDD)	—	55	—	ms
KP (LKP = DGND)	—	30	—	ms
All others	—	30	—	ms
TONE REJECTION	Tr	—	—	—
KP (LKP = VAN)	—	—	30	ms
KP (LKP = DGND)	—	—	10	ms
All others	—	—	10	ms
Tone Skew Tolerance	Tskew	4	—	ms
Pause Duration	Tpse	20	—	ms
Bridged Pause Duration	Tbr	—	10	ms
Minimum Strobe PW	Tstr	—	—	—
QUAL High	—	20	—	ms
QUAL Low	—	2	—	ms
Minimum Strobe Separation	Tsep	—	—	—
QUAL High	—	20	—	ms
QUAL Low	—	2	—	ms
Rise Time	Tr	—	100	ns
Fall Time	Tf	—	100	ns
CSTR* Width	Tw	50	—	ns
Data Enable Time	Ten	—	100	ns
Data Disable Time	Tdis	—	100	ns
Strobe Reset Time	Trst	—	100	ns

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Absolute Maximum Ratings

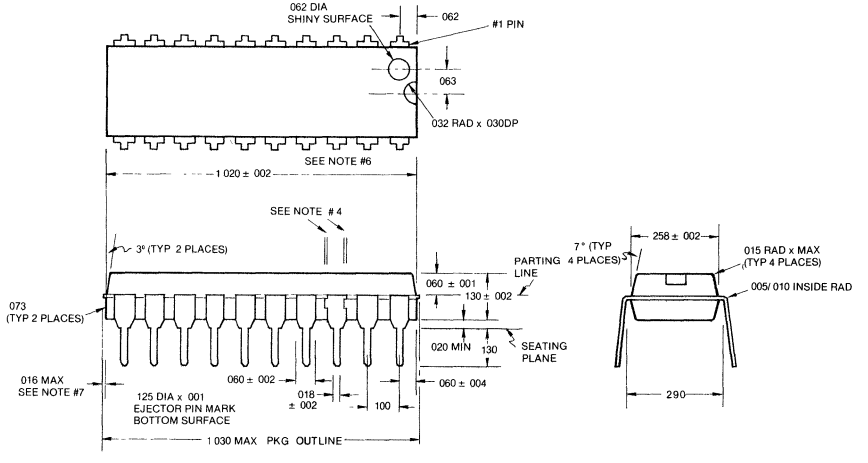
DC Supply Voltage Vp ..... +7V
Operating Temperature ..... 0°C to 70°C Ambient
Storage Temperature ..... 65°C to 150°C
Power Dissipation (25°C) 650mW
(Derate above TA = 25°C @ 6.25 mW/°C)

Input Voltage ..... (Vp to 3V) to −0.3V
DC Current into any input ..... ±10mA
Lead Temperature ..... 300°C
(Soldering, rosel)

*Operating above absolute maximuum ratings may damage the device.

AC Characteristics (0°C ≤ TA 70°C, V_{DD} = 5V ±10%)

Parameter	Conditions	Symbol	Min	Max	Units
Frequency for Detect	—	F	±(0.015* Fo+5)	—	Hz
Amplitude for Detect	each tone	A	−25	0	dBm
			0.123	2.191	Vpp
Amplitude for No Detect	—	An	—	−35	dBm
			—	0.039	Vpp
Twist Tolerance	$TW = \frac{\text{high tone}}{\text{low tone}}$	TW	6	—	dB
Third MF Tone Reject Amp	relative to highest tone	T3	−15	—	dB
Noise Tolerance	$N_n = \frac{\text{one false operation}}{\text{2500 (10 digits)}}$	Nn	20	—	dB
60 HZ Tolerance	same as above	N60	81	—	dBrn
			0.777	—	Vpp
180 HZ Tolerance	same as above	N180	68	—	dBrn
			0.174	—	Vpp



Notes:
1. Package to frame mismatch not greater than .004" in any direction To be measured in molded strip form
2. Side to side and end to end package mismatch (top half vs bottom half alignment) not greater than 003"
3. Leads to be within .010"of true position
4. Shoulder intrusion/protrusion not greater than 002"
5. Raised letters spelling "Singapore" on one bottom ejector pin area. Letters must not extend out past bottom package surface and are to be less than 003" in depth Letters to be arranged in a radial pattern with at least a 040"character size
6. Maximuum flash between leads to be 003"
7. End flash not to exceed 010" Total package length including this flash must be maintained as shown on drawing
8. Package surface to be matte finish (23-27 charmilles) except for ejector pin, index notch and pin 1 identification markings

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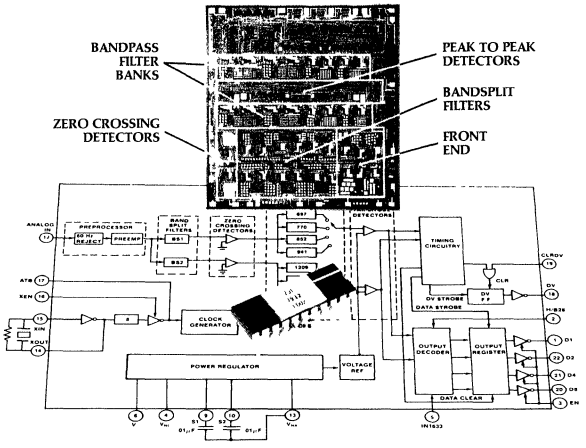
Application Guide for SSi Monolithic Dual-Tone Multi-Frequency (DTMF) Receivers



The SSi integrated DTMF Receivers are complete Touch-Tone detection systems. Each can operate in a stand-alone mode for the majority of telecommunications applications, thereby providing the most economical implementation of DTMF signaling systems possible. Each combines precision active filters and analog circuits with digital control logic on a monolithic CMOS integrated circuit. SSi DTMF Receiver use is straightforward and the external component requirements are minimal. This application guide describes device operation, performance, system requirements, and typical application circuits for the SSi DTMF Receiver circuits

How the SSi DTMF Circuits Work

General Description of Operation

The task of a DTMF Receiver is to detect the presence of a valid tone pair on a telephone line or other transmission medium. The presence of a valid tone pair indicates a single dialed digit; to generate a valid digit sequence, each tone pair must be separated by a valid pause.

The following table gives the established Bell system standards for a valid tone pair and a valid pause:

One Low-Group Tone	697 or 770 or 852 or 941 Hz
—and—	
One High-Group Tone	1209 or 1336 or 1477 or 1633 Hz
Frequency Tolerance	$f_O \pm (1.5\% + 2\ Hz)$
Amplitude Range	$-24\ dBm \leq A \leq +6\ dBm\ @\ 600\Omega$ (Dynamic Range 30 dB)
Relative Amplitude (Twist)	$-8\ dB \leq \frac{\text{High-Group Tone}}{\text{Low-Group Tone}} \leq +4\ dB$
Duration	40ms or longer
Inter-tone Pauses	40ms or longer

The SSi DTMF Receivers meet or exceed these standards.

Similar device architecture is used in all the SSi DTMF Receivers. Figure 1 shows the SSI 202 Block Diagram. In general terms, the detection scheme is as follows: The input signal is pre-filtered and then split into two bands, each of which contains only one DTMF tone group. The output of each band-split filter is amplified and limited by a zero-crossing detector. The limited signals, in the form of square waves, are passed through tone frequency band pass filters. Digital logic is then used to provide detector sampling and determine detection validity, to present the digital output data in the correct format, and to provide device timing and control.

Detailed Description of Operation

Noise and Speech Immunity

The two largest problems confronting a DTMF Receiver are:

1) Distinguishing between valid tone pairs (or pauses) and other stray signals (or speech) that contain valid tone pair frequencies.

2) Detecting valid tone pairs in the presence of noise, which is typically found in the telephone (or other transmission medium) environment.

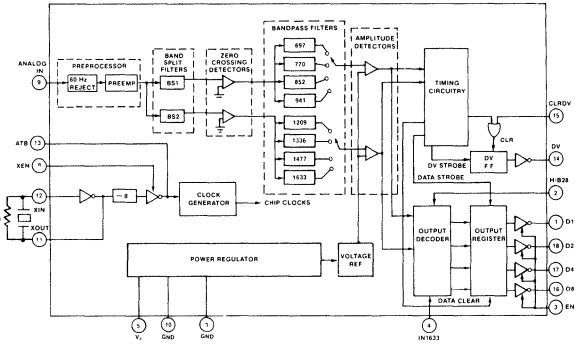


Figure 1. SSi 202 Block Diagram

The SSi DTMF Receivers use several techniques to distinquish between valid tone pairs and other stray signals. These techniques are explained in later sections. Briefly, the techniques are:

1) Pre-filtering of audio signal. Removes supply noise and dial tone from input audio signal and emphasizes the voice frequency domain.

2) Zero-cross detection. Limits the acceptable level of noise during detection of a tone pair. Important for speech rejection.

3) Valid tone pair/pause sampling. Samples the detection filters and checks for consistency before determining that a received tone pair or pause is valid.

Audio Preprocessor

The Audio Preprocessor is an analog filter that band limits the input analog signal between 500 Hz and 6 KHz. In addition, it emphasizes the 2 KHz to 6 KHz voice region.

Band limiting suppresses power supply and dial tone frequencies, and high frequency noise. The emphasized voice region helps to equalize the audio response since many phone lines tend to roll off at about 1 KHz. The upper voice frequencies are important in providing speech immunity.

Tone Band Splitting

After the analog signal is preprocessed, it is then split into two bands, each of which contains only one DTMF tone group. The band-split filters are actually band-stop filters to maintain all frequencies except the *other* tone group, this is done to maintain all analog information to enhance speech immunity but not allow the other tone group to act as interfering noise for the band being detected. These band-stop filters have "floors" that limit the amount of tone pair twist which further enhances speech immunity. See device data sheets for acceptable twist limits

Zero-Crossing Detectors

The output of each band-split filter is amplified and limited by a zero-crossing detector (limiter). The function of the zero-crossing detector is to produce a square wave at the prime frequency emanating from the band-split filter. If a pure tone is not present, as in the case of voice or other interfering noise, a rectangular wave with a variable period will result. Proportional to the interference, the limiter output power is spread over a broad frequency range as the zero crossings "dither". When a high level of noise (or speech) occurs, no single bandpass filter pair will contain significant power long enough to result in a tone detection. The zero-crossing detector also acts as AGC (Automatic Gain Control) in that the output amplitude is independent of input amplitude; this additionally establishes an acceptable signal-to-noise ratio not dependent on tone amplitude.

Bandpass Filters and Amplitude Detectors

The bandpass filters perform tone frequency discrimination. Their responses are tailored so that if the frequency of the limited square wave from the zero-crossing detector is within the tone frequency tolerance, the filter output will exceed the amplitude detector threshold. The amplitude detectors are interrogated periodically by the digital control circuity to ascertain the presence of one and only one tone in each band for the required duration. In a similar fashion, valid pauses are measured by the absence of valid tone pairs for the specified time.

Timing and Logic

The only precision external element needed for the SSi DTMF Receivers is a 3.58 MHz crystal (color-burst frequency) for the on-board oscillator. This generates the precise clock for the filters and for the logic timing and control of the receive.

Circuit Implementation

Standard CMOS technology is used for the entire circuit. Logic functions use standard low-power circuitry while the analog circuits use precision switched-capacitor-filter technology.

How to Use the SSi DTMF Receivers

Precautions

Although static protection devices are provided on the high-impedance inputs, normal handling precautions observed for CMOS devices should be used.

A destructive high current latch-up mode will occur if pin voltages are not constrained to the range between VN − .5 Volt and VP + .5 Volt (except AIN as described below). In applications where voltage spikes may occur, protection must be provided to ensure that the maximum voltage ratings are not exceeded. This may require the use of clamping diodes on the Analog Input to protect against ringer voltage, for example, or on the power supply to protect against supply spikes.

Power Supply

Excessive power supply noise should be avoided and to aid the user in this regard, power supply hook-up options are provided on some devices.

Since the digital circuitry of the devices possess the high noise immunity characteristics of CMOS logic, limited power supply noise is required only for the analog section. On those SSi DTMF receivers that have separate Analog Negative and Digital Negative supply connections (grounds), namely VNA and VND, an unfiltered supply may be used at VND. It is necessary that VND and VNA differ no more than 0.5 Volts

The analog circuitry of the devices require low power supply noise levels as specified on the device Data Sheet. Power supply noise effects will be slightly less if the analog input is referenced to VP. This is normally accomplished by connecting VP to ground and utilizing a negative power supply. The effects of excessive power supply noise will cause decreased tone amplitude sensitivity and less tone detection frequency bandwidth.

Digital Inputs

The digital inputs are directly compatible with standard CMOS logic devices powered by VP and VN (or VND). The input logic levels should swing within 30% of VP or VN to insure detection. Any unused input must be tied to VN or VP. Figure 2 shows methods for interfacing TTL outputs to 12 Volt SSi DTMF Receivers.

Analog Input

The Analog Input is the signal input pin for the devices, and is specially biased to facilitate its connection to external circuitry, as shown in Figure 3. The signal level at the Analog Input pin must not exceed or fall more than a few volts below the positive supply as stated on the device Data Sheets If this condition cannot be guaranteed by the external circuitry, the signal must be AC coupled into the chip with a .01μF ± 20% capacitor.

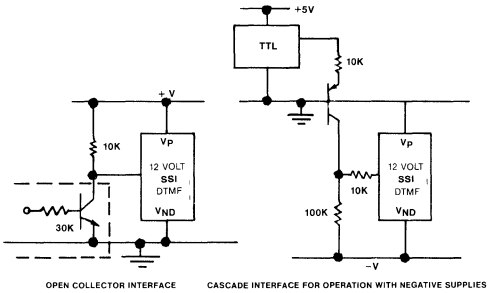


Figure 2 Interface circuits for conversion from TTL output levels to 12 volt SSi DTMF input levels

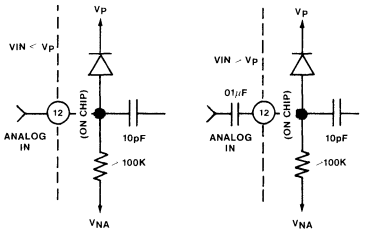


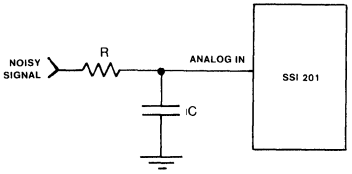
Figure 3. Direct and AC coupled configurations

Analog Input Noise

The SSi DTMF Receivers will tolerate wide-band input noise of up to 12dB below the lowest amplitude tone fundamental during detection of a valid tone pair. Any single interference frequency (including tone harmonics) between 1 KHz and 6 KHz should be at least 20 dB below the lowest amplitude tone fundamental. Adherence to these conditions will ensure reliable detection and full tone detection frequency bandwidth Because of the internal band limiting, noise with frequencies above 8 KHz can remain unfiltered. However, noise near the 56 KHz internal switched-capacitor-filter sampling frequency will be aliased (folded back) into the audio spectrum, noise above 28 KHz therefore should be low-pass filtered with a circuit as shown in Figure 4 using a cut-off frequency (Fc) of 6.6 KHz.

A 1 KHz cut-off frequency filter can be used on "normal" phone lines for special applications. When a phone line is particularly noisy, tone pair detection may be unreliable. A 1 KHz low pass filter will remove much of the noise energy but maintain the tone groups; however, a decreased speech immunity will result. This usage should only be considered for applications where speech immunity is not important, such as control paths that carry no speech.

Some DTMF tone pair generators output distorted tones which the SSi DTMF Receivers may not detect reliably (inexpensive extension telephones are an example). Most of the interfering harmonics of these tones may be removed by the use of a 3 KHz low-pass filter as in Figure 4. Some speech immunity degradation will result, but not as bad as using the 1 KHz filter mentioned above.



F_C (KHz)	R (KΩ) (± 5%)	C (μF) (± 20%)
10	16	01
31	51	01
66	24	01

SUGGESTED COMPONENT VALUES

Figure 4 Filter for use in noisy environments

Telephone Line Interface

In applications that use an SSi DTMF Receiver to decode DTMF signals from a phone line, a DAA (Direct Access Arrangement) must be implemented. Equipment intended for connection to the public telephone network must comply with and be registered in accordance to FCC Part 68 For PBX applications refer to EIA Standard RS-464

Some of the basic guidelines are:

1) Maximum voltage and current ratings of the SSi DTMF Receivers must not be exceeded; this calls for protection from ringing voltage, if applicable, which ranges from 80 to 120 Volts RMS over a 20 to 80 Hz frequency range.

2) The interface equipment must not breakdown with high-voltage transient tests (including a 2500 Volt peak surge) as defined in the applicable document.

3) Phone line termination must be less than 200 Ohms DC and approximately 600 Ohms AC (200-3200 Hz).

4) Termination must be capable of sustaining phone line loop current (off-hook condition) which is typically 18 to 120 mA DC

5) The phone line termination must be electrically balanced in respect to ground.

6) Public phone line termination equipment must be registered in accordance to FCC Part 68 or connected through registered protection circuitry. Registration typically takes about six months.

Ready made DAA devices are also available. One source is Cermetek Microelectronics, Sunnyvale, California.

Figure 5 shows a simplified phone line interface using a 600 Ohm 1:1 line transformer. Transformers specially designed for phone line coupling are available from many transformer manufacturers.

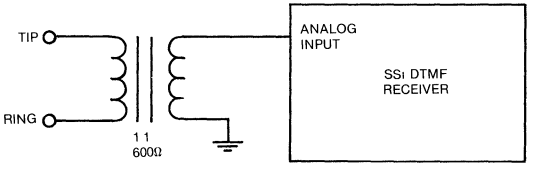


Figure 5 Simplified Phone Line Interface

Figure 6 shows a more featured version of Figure 5. These added options include:

1) A 150 Volt surge protector to eliminate high voltage spikes.

2) A Texas Instruments TCM1520A ring detector, optically isolated from the supervisory circuitry.

4) Back-to-back Zener diodes to protect the DTMF (and optional multiplexer Op-Amp) from ringer voltage.

5) Audio multiplexer which allows voice or other audio to be placed on the line (a recorded message, for example) and not interfere with incoming DTMF tone detection.

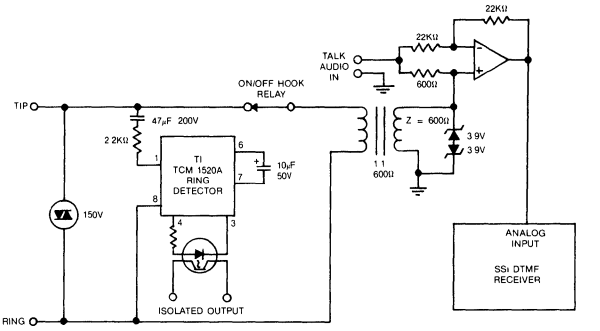


Figure 6 Full Featured Phone Line Interface

An integrated voice circuit may also be implemented for line coupling, such as the Texas Instruments TCM1705A, however, this approach is typically more expensive than using a transformer as shown above.

Outputs

The digital outputs of the SSi DTMF Receivers (except XOUT) swing between VP and VN (or VND) and are fully compatible with standard CMOS logic devices powered from VP and VN The 5 Volt DTMF devices will also interface directly to LSTTL. The 12 Volt DTMF devices can interface to TTL or low voltage MOS with the circuit in Figure 7.

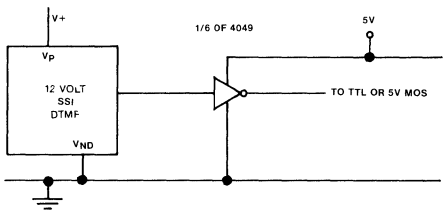


Figure 7 SSi 12 Volt DTMF to TTL Level Interface

Data Outputs D8, D4, D2, and D1 are three-state enabled to facilitate interface to a three-state bus. Figure 8 shows the equivalent circuit for the data outputs in the high impedance state. Care must be taken to prevent either substrate diode in Figure 8 from becoming forward biased or damage may result.

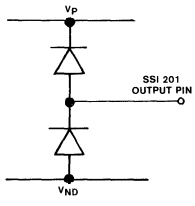


Figure 8. Equivalent Circuit of SSi DTMF Receiver Data Output in High Impedance State

Timing

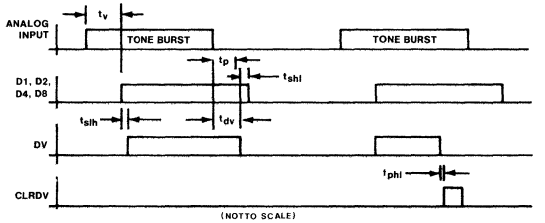
Within 40 ms of a valid tone pair appearing at the DTMF Receiver Analog Input, the Data Outputs D8, D4, D2 and D1 will become valid. SSI 201 timing is shown in Figure 9 (refer to the device Data Sheet for other timing diagrams). Seven microseconds after the data outputs have become valid DV will be raised. DV will remain high and the outputs valid while the valid tone pair remains present. Within 40 ms after the tone pair stops, the DTMF will recognize a valid pause. DV is lowered approximately 45 ms following the end of the tone pair, and the data outputs all set to zero 4.56 ms following DV going low. DV will strobe at least for the same duration as the received tone pair.

System Interface

Provision has been made on the SSi DTMF Receivers for handshake interface with an outside monitoring system. In this mode, the DV strobe is polled by the monitoring system at least once every 40 ms to determine whether a new valid tone pair has been detected. If DV is high, the coded data is stored in the monitoring system and then CLRDV is pulsed high. With some systems operating in the handshake mode, it may be desirable to know when a valid pause has occurred. Ordinarily this would be indicated by the falling edge of DV. However, in the handshake mode, DV is cleared by the monitoring system each time a new valid tone pair is detected and, therefore, cannot be used to determine when a valid pause is detected. The detection of a valid pause in this case may be observed by detecting the clearing of the Data Outputs. Since, in hexidecimal format (the mode normally used with a handshake interface), the all zero state represents a commonly unused tone pair (D), the detection of a valid pause may be detected by connecting a four-input NOR gate to the device outputs and sensing the all zero state.

Time Base

The SSi DTMF Receivers contain an on-chip oscillator for a 3.5795 MHz parallel resonant quartz crystal or ceramic resonator. The crystal (or resonator) is placed between XIN and XOUT in parallel with a 1 Mohm resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the oscillator, the tone detect band frequency tolerance is proportional to the time base tolerance. The SSi DTMF Receiver frequency response and timing is guaranteed with a time base accuracy of at least ±.01%. To obtain this accuracy the CTS Part No. MP036 or Workman Part No. CY1-C or equivalent quartz crystal is recommended. In less critical applications a suitable ceramic resonator may be implemented.



KEY

SYMBOL	DEFINITION	SPEC MIN	TYP	MAX	UNIT	CONDITION V_P - (V_{NA} = V_{ND}) = 12V ±10% TA = 0°C-70°C
t_v	TONE DETECTION TIME	20	--	40	ms	--
t_{slh}	DATA OVERLAP OF DV RISING EDGE	7	--	--	µs	CLRDV = V_{ND}, EN = V_P
t_p	PAUSE DETECTION TIME	25	--	40	ms	--
t_{dv}	TIME BETWEEN END OF TONE AND FALL OF DV	40	45	50	ms	--
t_{shl}	DATA OVERLAP OF DV FALLING EDGE	4	4.56	4.8	ms	--
t_{phl}	PROP DELAY RISE OF CLRDV TO FALL OF DV MEASURED AT 50% POINTS	--	--	1	µs	CI = 300 pF
---	OUTPUT ENABLE TIME MEASURED FROM 50% POINT OF RISING EDGE OF EN TO THE 50% POINT OF THE DATA OUTPUT WITH RI TO OPPOSITE RAIL	--	--	1	µs	CI = 300pF, RI = 10K
---	OUTPUT DISABLE TIME MEASURED FROM 50% POINT OF FALLING EDGE OF EN TO TIME AT WHICH OUTPUT HAS CHANGED 1V WITH RI TO OPPOSITE RAIL	--	--	1	µs	CI = 300pF, RI = 1K ΔV = 1V
---	OUTPUT 10-90% TRANSITION TIME	--	--	1	µs	CI = 300pF

Figure 9. SSI 201 Timing Diagram and Specifications

For the SSi 201, a muRata Part No. FX-5135 is recommended which will provide an accuracy of approximately ±0.3%. The use of a ceramic resonator requires the addition of two 30pF ±10% capacitors; one between XIN and VN (or VND) and the other between XOUT and VN (or VND). Extra caution should be used to avoid stray capacitance on the resonant circuit when using a ceramic resonator instead of a quartz crystal.

When the oscillator connected as above and XEN tied high, the ATB (alternate time base) pin delivers a square wave output at one-eighth the oscillator frequency (447.443 KHz nominal). The ATB pin can be converted to a time base input by tying XEN low; ATB can then be externally driven from another device such as the ATB output of another DTMF. No crystal is required for the ATB input device; XIN must be tied high if unused. Several SSi DTMF Receivers can be driven with a single crystal (refer to device data sheet for fan-out limit).

XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. If a 3.58 MHz clock is needed for more than one device and it is desirable to use only one resonant device, an outside inverter should be used for the time base, buffered by a second inverter or buffer. The buffer output would then drive XIN of the SSi DTMF Receiver as well as the other device(s); XOUT must be left floating and XEN tied high.

Dial Tone Rejection

The SSi DTMF Receivers incorporate enough dial tone rejection circuitry to provide dial tone tolerance of up to 0 dB. Dial tone tolerance is defined as the total power of precise dial tone (350 Hz and 440 Hz as equal amplitudes) relative to the lowest amplitude tone in a valid tone pair. The filter of Figure 10 may be used for further dial tone rejection. This filter exhibits an elliptic highpass response that provides a minimum of 18 dB rejection at 350 Hz and 24 dB rejection at 440 Hz so long as the component tolerances indicated are observed. The DTMF on-chip filter rejects 350 Hz at least 6 dB more than 440 Hz. Therefore, employing the filter of Figure 10 yields a dial tone tolerance of +24 dB.

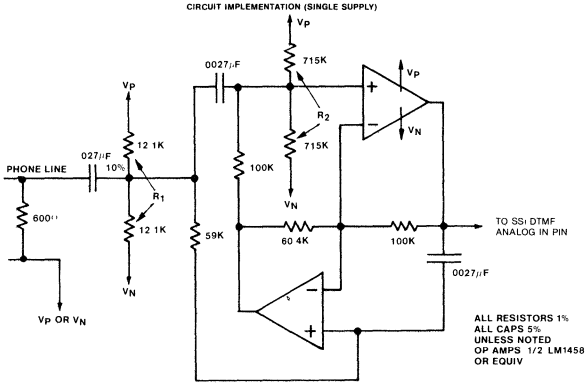


Figure 10. Dial Tone Reject Filter

Printed Circuit Board Implementation

The SSi DTMF Receivers are analog in nature and should be treated as such; circuit noise should be kept to a minimum. To be certain of this, all input and output lines should be kept away from noise sources (high frequency data or clock lines); this is especially true for the Analog Input. Noise in the ground or power supply lines can be avoided by running separate traces to supportive logic circuits or by running thicker (lower resistance) busses. Capacitance power supply bypassing should be performed at the device. Refer to the Power Supply section above.

Performance Data

A portion of the final SSi DTMF Receiver device characterization uses the Mitel CM7290 tone receiver test tape. The evaluation circuit shown in Figure 11 was used to characterize the SSI 201. The speed and output level of the tape deck must be adjusted so that the calibration tone at the beginning of the tape is at exactly 1000 Hz and 2V rms.

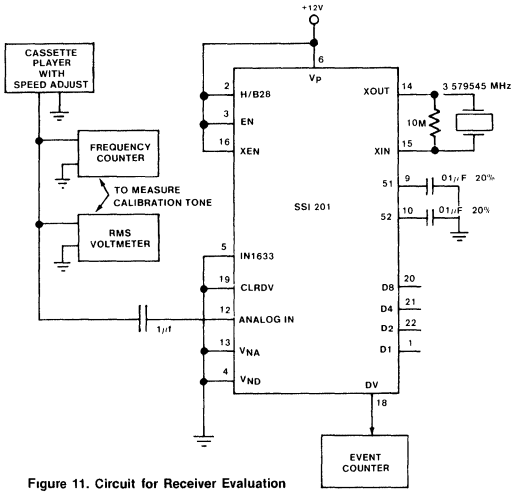


Figure 11. Circuit for Receiver Evaluation

The Mitel tape tests yield similar results on all of the SSI DTMF Receivers. Test results for the SSI 201 are summarized in Table 1. In short, the measured performance data demonstrates that the SSI DTMF Receivers are monolithic realizations of a full "central office quality" DTMF Receiver.

TEST #	RESULTS
2a,b	B W = 5 0% of fo
2c,d	B W = 5 0% of fo
2e,f	B W = 5 3% of fo
2g,h	B W = 4 9% of fo
2i,j	B W = 5 0% of fo
2k,l	B W = 5 3% of fo
2m,n	B W = 5 3% of fo
2o,p	B W = 4 8% of fo
3	160 decodes
4	Acceptable Amplitude Ratio (Twist) = −19 1dB to +15 2dB
5	Dynamic Range = 32 5dB
6	Guard Time = 23 3 ms
7	100% Successful decodes at N/S Ratio of − 12dBV
8	2-3 Hits Typical on Talk-Off Test

Table I Mitel #CM7290 Tape Test Results for SSI 201 (Averaged for 10 parts)

Applications

Creating Hexadecimal "0" Output upon Digit "0" Detection

To be consistent with pulse-dialing systems, the SSI DTMF Receivers provide a hexadecimal "10" output upon the detection of a digit 0 tone pair when in the hexadecimal code format. However, some applications may instead require a hexadecimal "0" with a digit "0" detection. The circuit of Figure 12 shows an easy method to recode the hexadecimal outputs to do this using only 4 NOR gates.

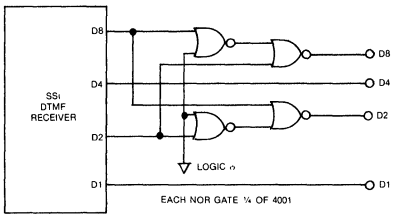


Figure 12. Hex "0" Out with Digit "0" Detect Conversion Circuit

Note that this circuit will not give proper code for the "*", "B", or "C" digits and will cause both digits "D" and "0" to output hexadecimal "0". This circuit should therefore be considered for numeric digits only. The output code format is shown in Table II.

	HEXADECIMAL				HEXADECIMAL AND FIG 12 CIRCUIT			
Digit	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	0	0	1
0	1	0	1	0	0	0	0	0
*	1	0	1	1	0	0	0	1
#	1	1	0	0	1	1	0	0
A	1	1	0	1	1	1	0	1
B	1	1	1	0	0	1	0	0
C	1	1	1	1	0	1	0	1
D	0	0	0	0	0	0	0	0

Table II. Output Code of Figure 12

This circuit is useful for applications that require a display of dialed digits; the digit display usually requires a hexadecimal "0" input for a "0" to be displayed.

16-Channel Remote Control

DTMF signaling provides a simple, reliable means of transmitting information over a 2-wire twisted pair. The complete schematic of a 16-channel remote control is shown in Figure 13. When one of the key pad buttons is depressed, a tone pair is sent over the transmission medium to the SSI DTMF Receiver.

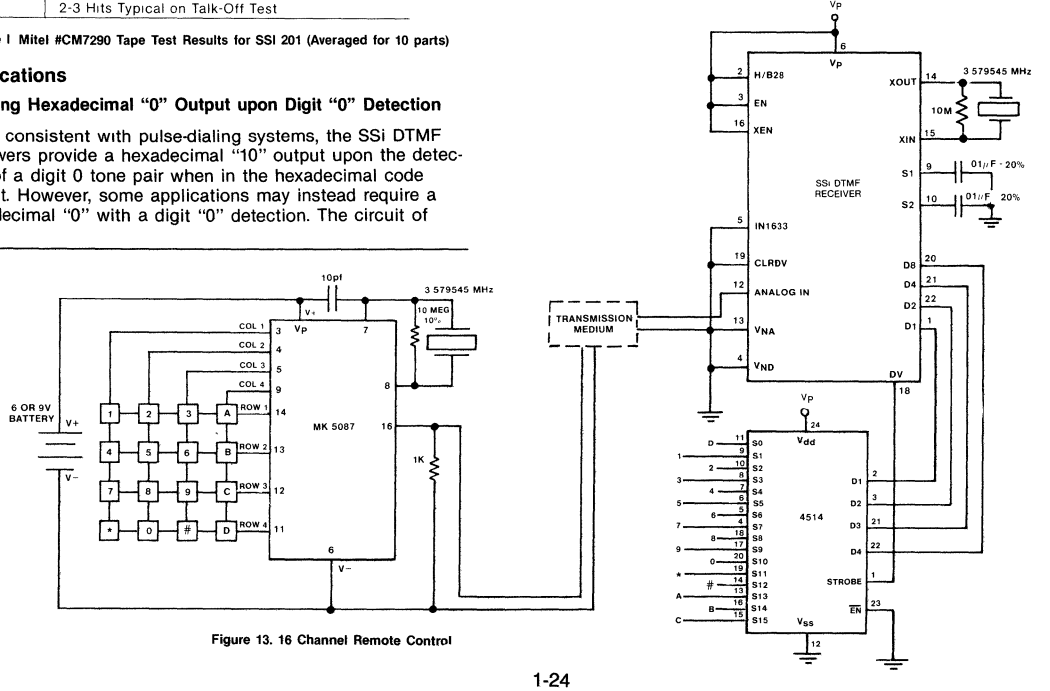


Figure 13. 16 Channel Remote Control

The 4514 raises one of its 16 outputs in response to the 4-bit output code from the DTMF. The output at the 4514 will remain high until the next button is depressed.

2-of-8 Output Decode

The circuit shown in Figure 14 can be used to convert the binary coded 2-of-8 to the actual 2 of 8 code (or 2 of 7 if detection of 1633 Hz tone is inhibited). The output data will be valid while DV is high. If it is desired to force the eight outputs to zero when a valid tone is not present, DV should be inverted and connected to both E-NOT inputs of the 4555.

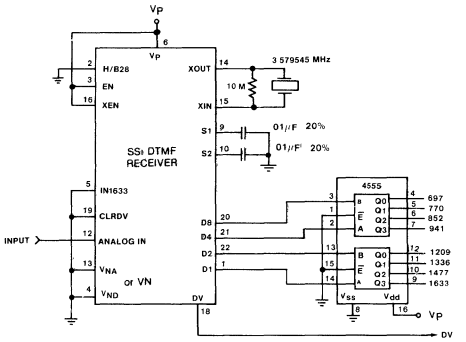


Figure 14 Touch Tone to 2-of-8 Output Converter

DTMF to Rotary Dial Pulse Converter

The 2-of-8 output of Figure 14 can be modified to interface with a pulse dialer as shown in Figure 15 If a 12 Volt DTMF is used the 4049 will translate the 12 Volt outputs to the 5 Volt swings required for the MK5099 pulse dialer

Figure 16 shows the interface for adding pulse detection and counting to a SSi DTMF Receiver.

The loop detector provides a digital output representing the telephone loop circuit "make" and "break" condition associated with rotary pulse dialing. For the circuit of Figure 16, Ground represents a "make" and V_p a "break".

The loop detector feeds dial pulses to IC-1, a binary counter, and to IC-2A, a re-triggerable "one-shot'. When a dial pulse appears the Q1-NOT output of IC-2A immediately goes low, resetting IC-1. The clock input to IC-1 is delayed by R1-C1 so that reset and count input do not overlap The binary outputs of IC-1 will reflect the pulse count and 0 2 seconds after the last pulse the Q1-NOT output will go high. C3-R3 differentiate this pulse and clock the output latch, IC-3, holding the output pulse until the next digit.

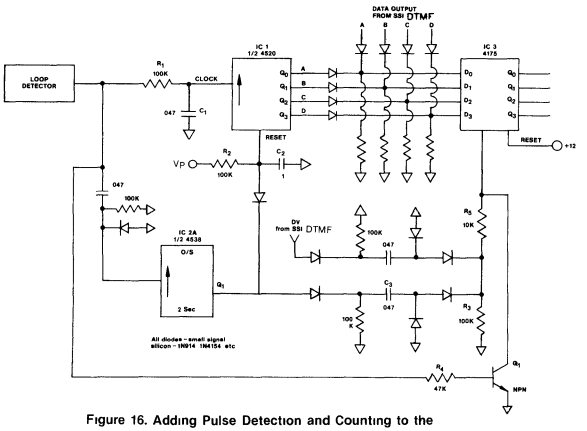


Figure 16. Adding Pulse Detection and Counting to the SSi DTMF Receivers

The 0.2 second timeout of IC-2A indicates the end of dial pulsing since even a slow (8 pps) dial would input another pulse every 0 125 seconds. The binary outputs of IC-1 are paralleled with those of the SSi DTMF Receiver circuit through diodes to the inputs of IC-3 A pulldown resistor is necessary on each IC-3 input pin IC-1 must be a binary, not BCD, counter.

With a 4175 for IC-3 the output data is latched until the next valid input, whether from a rotary dial or dual tone instrument A unique situation exists, however, when going on-hook. The loop detector will output a continuous level of VP which would trigger IC-2A and put a single count into IC-1 A high level from the loop detector also turns on Q1, pulling the clock input of IC-3 to ground Since the loop detector output will be low at the completion of dialing, all outputs are valid even when the telephone is placed on-hook, an important consideration if output data is recorded.

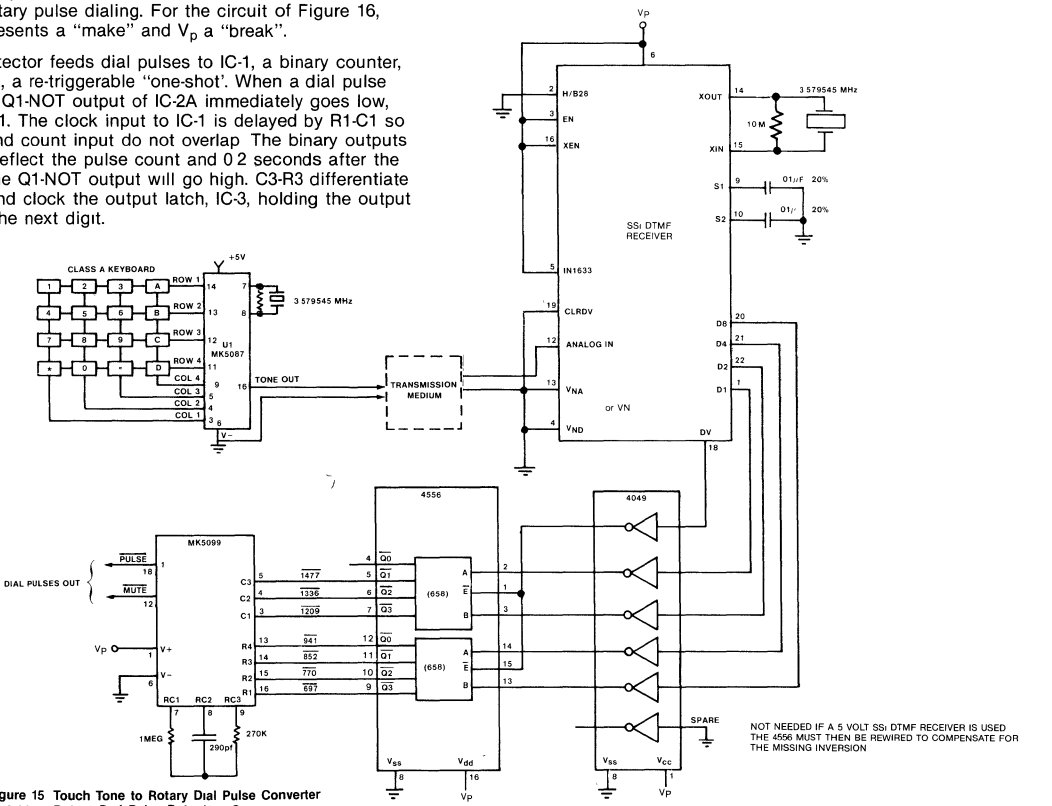


Figure 15 Touch Tone to Rotary Dial Pulse Converter Adding Rotary Dial Pulse Detection Capabilities

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SSI 20C89
DTMF Transceiver

Data Sheet

GENERAL DESCRIPTION

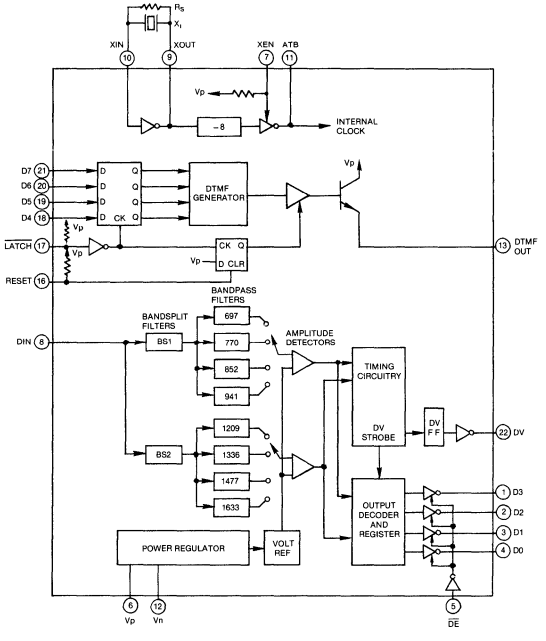
Silicon Systems' new SSI 20C89 is a complete Dual Tone Multiple Frequency (DTMF) Transceiver that can both generate and detect all 16 standard Touch-Tone digits. The SSI 20C89 circuit integrates the performance proven SSI 202 DTMF Receiver with a new DTMF generator circuit.

The DTMF Receiver electrical characteristics are identical to the standard SSI 202 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

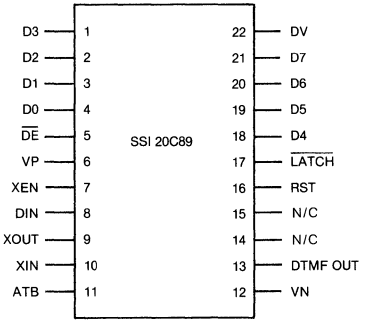
The only external components necessary for the SSI 20C89 are: a 3.58 MHz "colorburst" crystal with a parallel 1 MΩ resistor. This provides the time base for digital functions and switched capacitor filters in the device. No external filtering is required.

FEATURES

- **DTMF Generator and Receiver on one chip**
- **22-Pin plastic DIP**
- **Low-power 5 Volt CMOS**
- **DTMF Receiver exhibits excellent speech immunity**
- **Three-state outputs (4-bit hexadecimal) from DTMF Receiver**
- **AC coupled, internally biased analog input**
- **Latched DTMF Generator inputs**
- **Analog input range from −32 to −2 dBm (ref 600Ω)**
- **DTMF output typ. −8 dBm (Low Band) and −5.5 dBm (High Band)**
- **Uses inexpensive 3.579545 MHz crystal for reference**
- **Easily interfaced for microprocessor dialing**



Block Diagram



Pin Out
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

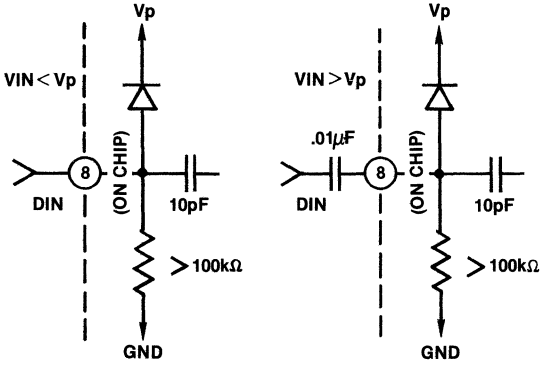
CIRCUIT OPERATION

Receiver

The DTMF Receiver in the SSI 20C89 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60 Hz reject and band splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

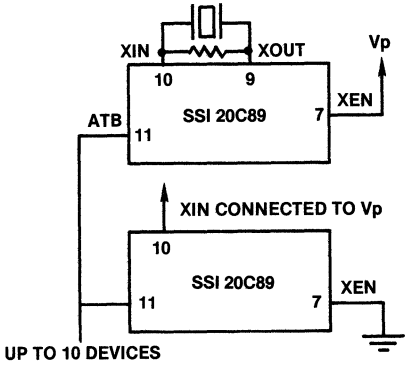
This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated below.



The SSI 20C89 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental.

Crystal Oscillator

The SSI 20C89 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1 Mohm resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the 20C89 depends on the time base tolerance. The SSI DTMF Receiver frequency response and timing is specified for a time base accuracy of at least ±0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SSI 20C89 as shown below.



Receiver Outputs and the $\overline{DE}$ Pin

Outputs D0,D1,D2,D3 are CMOS push-pull when enabled ($\overline{DE}$ low) and open-circuited (high impedance) when disabled ($\overline{DE}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. The table below shows that code.

Digit	Input: / Output:	Hexadecimal code D7 / D3	D6 / D2	D5 / D1	D4 / D0
1		0	0	0	1
2		0	0	1	0
3		0	0	1	1
4		0	1	0	0
5		0	1	0	1
6		0	1	1	0
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
0		1	0	1	0
★		1	0	1	1
#		1	1	0	0
A		1	1	0	1
B		1	1	1	0
C		1	1	1	1
D		0	0	0	0

Table 1

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

Generator

The DTMF generator on the SSI 20C89 responds to a hexadecimal code input with a valid tone pair. Pins D4-D7 are the data inputs for the generator. A high to low transition on $\overline{\text{LATCH}}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

Digital Inputs

The D4,D5,D6,D7, $\overline{\text{LATCH}}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Table 1 shows the code for each digit. The dialing matrix and detection frequency table below list the frequencies of the digits.

DTMF DIALING MATRIX

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

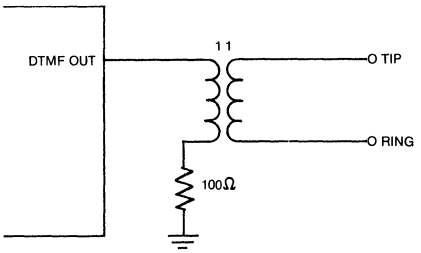
Note Column 3 is for special applications and is not normally used in telephone dialing

DETECTION FREQUENCY

Low Group f_o	High Group f_o
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0 V. However, the output level is directly proportional to the supply, so variations in it will affect the DTMF output. A recommended line interface for this output is shown below.



Absolute Maximum Ratings*

DC Supply Voltage (Vp-Vn) ..... +7V
Voltage at any Pin (Vn = 0) ..... −0.3 to Vp + 0.3 V
DIN Voltage ..... Vp + 0.5 to Vp-10 V
Current through any Protection Device ..... ±20mA
Operating Temperature Range ..... −40°C to +85°C
Storage Temperature ..... −65°C to 150°C

*Operation above absolute maximum ratings may damage the device

Recommended Operating Conditions

Parameter	Min.	Max.	Unit
Supply Voltage	4.5	5.5	V
Power Supply Noise (wide band)	—	10	mV pp
Ambient Temperature	0	70	°C
Crystal Frequency (F Nominal = 3.579545 MHz)	−.005	+.005	%
Crystal Shunt Resistor	0.8	1.2	MΩ
DTMF OUT Load Resistance	100	—	Ω

Digital and DC Requirements

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn = 0 unless otherwise stated.

Parameter	Test Conditions	Min.	Max.	Unit
Supply Current*	—	—	30	mA
Power Dissipation	—	—	225	mW
Input Voltage High	—	0.7Vp	—	V
Input Voltage Low	—	—	0.3Vp	V
Input Current High	—	—	10	μA
Input Current Low	—	−10	—	μA
Output Voltage High	Ioh = −0.2mA	Vp-0.5	—	V
Output Voltage Low	Iol = +0.4mA	—	Vn + 0.5	V

*with DTMF output disabled

DTMF Receiver
Electrical Characteristics

Parameter	Test Conditions	Min.	Typ	Max.	Unit
Frequency Detect Bandwidth	—	±(1.5+2Hz)	±2.3	±3.5	%Fo
Amplitude for Detection	Each Tone	−32	—	−2	dBm/tone
Twist Tolerance	—	−10	—	+10	dB
60Hz Tolerance	—	—	—	0.8	Vrms
Dial Tone Tolerance	Precise Dial Tone	—	—	0	dB*
Speech Immunity	MITEL Tape #CM7290	—	2	—	hits
Noise Tolerance	MITEL Tape #CM7290	—	—	−12	dB*
Input Impedance	—	100	—	—	kΩ

*Referenced to lowest amplitude tone

Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit
Tone Time for Detect	ton	40	—	ms
Tone Time for No Detect	ton	—	20	ms
Pause Time for Redetection	toff	40	—	ms
Pause Time for Bridging	toff	—	20	ms
Detect Time	td1	25	46	ms
Release Time	tr1	35	50	ms
Data Set Up Time	tsu1	7	—	μs
Data Hold Time	thd1	4.2	5.0	ms
Output Enable Time		—	200	ns
Output Disable Time		—	200	ns

DTMF Generator

Electrical Characteristics

Parameter	Test Conditions	Min.	Max.	Unit
Frequency Accuracy	—	−1.0	+1.0	%Fo
Output Amplitude	R1 = 100Ω to Vn, Vp − Vn = 5.0 V	—	—	—
Low Band	—	−9.2	−7.2	dBm
High Band	—	−6.6	−4.6	dBm
Output Distortion	DC to 50kHz	—	−20	dB

Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit
Start-Up Time	tstart	—	2.5	μs
Data Set-Up Time	tsu2	100	—	ns
Data Hold Time	thd2	50	—	ns
RESET Pulse Width	trp	100	—	ns
$\overline{\text{LATCH}}$ Pulse Width	tpw	100	—	ns

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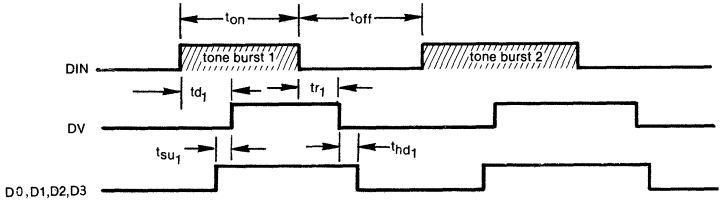
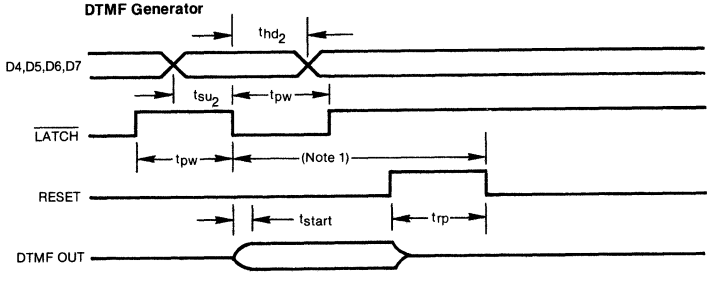
Timing Diagrams

DTMF Decoder

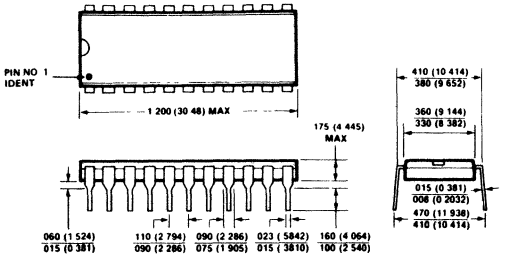


DTMF Generator



Note 1 The indicated time may be as small as 0 sec meaning that the $\overline{\text{LATCH}}$ and RESET lines may be tied together

PLASTIC DIP
22 Pins



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SSI 20C90
DTMF Transceiver with Call Progress Detection

Data Sheet

GENERAL DESCRIPTION

Silicon Systems' new SSI 20C90 is a complete Dual Tone Multiple Frequency (DTMF) Transceiver that can both generate and detect all 16 standard Touch-Tone digits. The SSI 20C90 circuit integrates the performance proven SSI 202 DTMF Receiver with a new DTMF generator circuit.

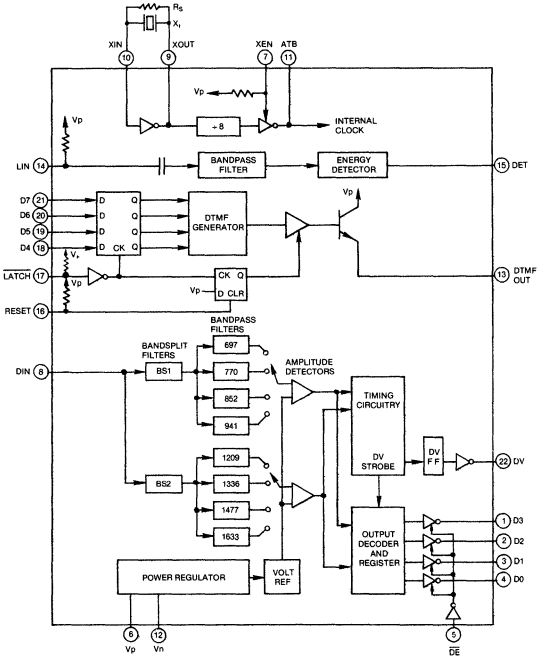
The DTMF Receiver electrical characteristics are identical to the standard SSI 202 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

An additional feature of the 20C90 is "imprecise" call progress detector. The detector detects the presence of signals in the 305-640 Hz band.

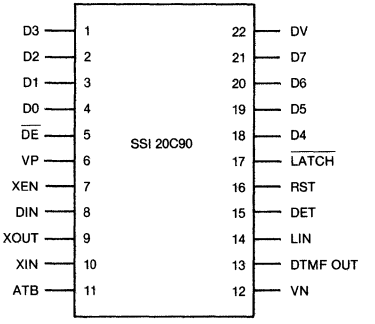
The only external components necessary for the SSI 20C90 are a 3.58 MHz "colorburst" crystal with a parallel 1 MΩ resistor. This provides the time base for digital functions and switched capacitor filters in the device. No external filtering is required.

FEATURES

- **DTMF Generator *and* Receiver on one chip**
- **22-Pin plastic DIP**
- **Low-power 5 Volt CMOS**
- **DTMF Receiver exhibits excellent speech immunity**
- **Three-state outputs (4-bit hexadecimal) from DTMF Receiver**
- **AC-coupled, internally-biased analog input**
- **Latched DTMF Generator inputs**
- **Analog input range from −32 to −2 dBm (ref 600Ω)**
- **DTMF output typ. −8 dBm (Low Band) and −5.5 dBm (High Band)**
- **Uses inexpensive 3.579545 MHz crystal for reference**
- **Easily interfaced for microprocessor dialing**
- **Call progress detection**



SSI 20C90 Block Diagram



Pin Out
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

SSI 20C90
DTMF Transceiver with Call Progress Detection

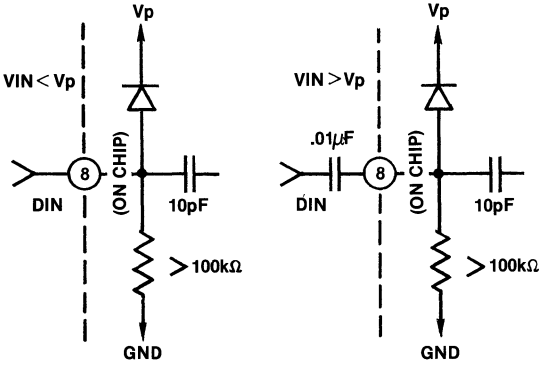
CIRCUIT OPERATION

Receiver

The DTMF Receiver in the SSI 20C90 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60 Hz reject and band splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

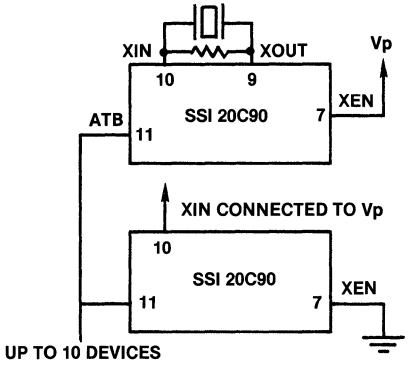
This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated below.



The SSI 20C90 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental.

Crystal Oscillator

The SSI 20C90 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1 Mohm resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the 20C90 depends on the time base tolerance. The SSI DTMF Receiver frequency response and timing is specified for a time base accuracy of at least ±0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SSI 20C90 as shown below.



Receiver Outputs and the $\overline{DE}$ Pin

Outputs D0,D1,D2,D3 are CMOS push-pull when enabled ($\overline{DE}$ low) and open-circuited (high impedance) when disabled ($\overline{DE}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. The table below shows that code.

Digit	Input: / Output:	Hexadecimal code D7 D3	D6 D2	D5 D1	D4 D0
1		0	0	0	1
2		0	0	1	0
3		0	0	1	1
4		0	1	0	0
5		0	1	0	1
6		0	1	1	0
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
0		1	0	1	0
★		1	0	1	1
#		1	1	0	0
A		1	1	0	1
B		1	1	1	0
C		1	1	1	1
D		0	0	0	0

Table 1

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

Generator

The DTMF generator on the SSI 20C90 responds to a hexadecimal code input with a valid tone pair. Pins D4-D7 are the data inputs for the generator. A high to low transition on $\overline{\text{LATCH}}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

Digital Inputs

The D4,D5,D6,D7, $\overline{\text{LATCH}}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Table 1 shows the code for each digit. The dialing matrix and detection frequency table below list the frequencies of the digits.

DTMF DIALING MATRIX

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

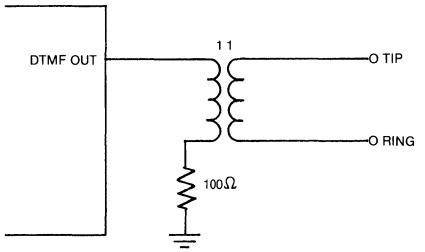
Note Column 3 is for special applications and is not normally used in telephone dialing

DETECTION FREQUENCY

Low Group f_o	High Group f_o
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0 V. However, the output level is directly proportional to the supply, so variations in it will affect the DTMF output. A recommended line interface for this output is shown below.



Call Progress Detection

The Call Progress Detector consists of a bandpass filter and an energy detector for turning the on/off cadences into a microprocessor compatible signal.

LIN Input

This analog input accepts the call progress signal and should be used in the same manner as the receiver input DIN.

DET Output

This output is TTL compatible and will be of a frequency corresponding to the various cadences of Call Progress signals such as, on 0.5 sec/off 0.5 sec for a busy tone, on 0.25 sec/off 0.25 sec for a reorder tone and on 0.8-1.2 sec/off 2.7-3.3 sec for an audible ring tone.

Absolute Maximum Ratings*

DC Supply Voltage (Vp-Vn) . . . . . +7V
Voltage at any Pin (Vn = 0) . . . . . −0.3 to Vp + 0.3 V
DIN Voltage . . . . . Vp + 0.5 to Vp-10 V
Current through any Protection Device . . . . . ± 20 mA
Operating Temperature Range . . . . . −40°C to +85°C
Storage Temperature . . . . . −65°C to 150°C

*Operation above absolute maximum ratings may damage the device

Recommended Operating Conditions

Parameter	Min.	Max.	Unit
Supply Voltage	4.5	5.5	V
Power Supply Noise (wide band)	—	10	mV pp
Ambient Temperature	0	70	°C
Crystal Frequency (F Nominal = 3.579545 MHz)	−.005	+.005	%
Crystal Shunt Resistor	0.8	1.2	MΩ
DTMF OUT Load Resistance	100	—	Ω

Digital and DC Requirements

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: LIN, DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn = 0 unless otherwise stated.

Parameter	Test Conditions	Min.	Max.	Unit
Supply Current*	—	—	30	mA
Power Dissipation	—	—	225	mW
Input Voltage High	—	0.7Vp	—	V
Input Voltage Low	—	—	0.3Vp	V
Input Current High	—	—	10	μA
Input Current Low	—	−10	—	μA
Output Voltage High	Ioh = −0.2mA	Vp-0.5	—	V
Output Voltage Low	Iol = +0.4mA	—	Vn+0.5	V

*with DTMF output disabled

DTMF Receiver
Electrical Characteristics

Parameter	Test Conditions	Min.	Typ	Max.	Unit
Frequency Detect Bandwidth	—	±(1.5+2Hz)	±2.3	±3.5	%Fo
Amplitude for Detection	Each Tone	−32	—	−2	dBm/tone
Twist Tolerance	—	−10	—	+10	dB
60Hz Tolerance	—	—	—	0.8	Vrms
Dial Tone Tolerance	Precise Dial Tone	—	—	0	dB*
Speech Immunity	MITEL Tape #CM7290	—	2	—	hits
Noise Tolerance	MITEL Tape #CM7290	—	—	−12	dB*
Input Impedance	—	100	—	—	kΩ

*Referenced to lowest amplitude tone

Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit
Tone Time for Detect	ton	40	—	ms
Tone Time for No Detect	ton	—	20	ms

Timing Characteristics (cont.)

Parameter	Symbol	Min.	Max.	Unit
Pause Time for Redetection	toff	40	—	ms
Pause Time for Bridging	toff	—	20	ms
Detect Time	td1	25	46	ms
Release Time	tr1	35	50	ms
Data Set Up Time	tsu1	7	—	μs
Data Hold Time	thd1	4.2	5.0	ms
Output Enable Time	—	—	200	ns
Output Disable Time	—	—	200	ns

DTMF Generator
Electrical Characteristics

Parameter	Test Conditions	Min.	Max.	Unit
Frequency Accuracy	—	−1.0	+1.0	%Fo
Output Amplitude	R1 = 100Ω to Vn, Vp − Vn = 5.0 V	—	—	—
Low Band	—	−9.2	−7.2	dBm
High Band	—	−6.6	−4.6	dBm
Output Distortion	DC to 50kHz	—	−20	dB

Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit
Start-Up Time	tstart	—	2.5	μs
Data Set-Up Time	tsu2	100	—	ns
Data Hold Time	thd2	50	—	ns
RESET Pulse Width	trp	100	—	ns
$\overline{\text{LATCH}}$ Pulse Width	tpw	100	—	ns

Call Progress Detector
Electrical Characteristics

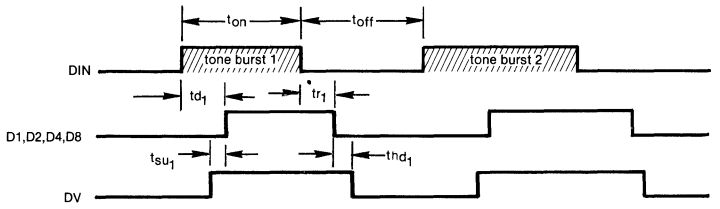
Parameter	Conditions	Min.	Max.	Unit
Amplitude for Detection	305 Hz − 640 Hz	−40	0	dBm
Amplitude for No Detection	305 Hz − 640 Hz	—	−50	dBm
	f > 2200Hz, < 160Hz	—	−25	dBm
Detect Output	Logic 0	—	.5	V
	Logic 1	4.5	—	V
"LIN" Input	Max Voltage	V_{DD} −10	V_{DD}	V
Input Impedance	500 Hz	100	—	kΩ

Timing Characteristics

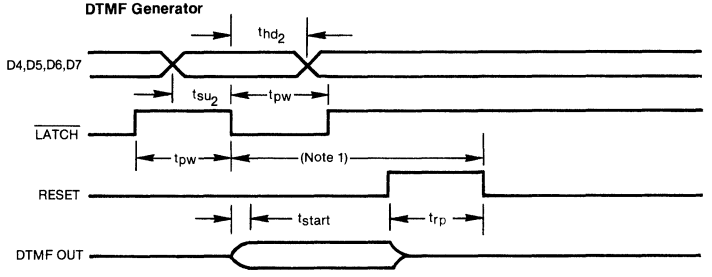
Parameter	Symbol	Min.	Max.	Unit
Signal Time for Detect	ton	40	—	ms
Signal Time for No Detect	ton	—	10	ms
Interval Time for Detect	toff	40	—	ms
Interval Time for No Detect	toff	—	20	ms
Detect Time	td2	—	40	ms
Release Time	tr2	—	40	ms

Timing Diagrams

DTMF Decoder

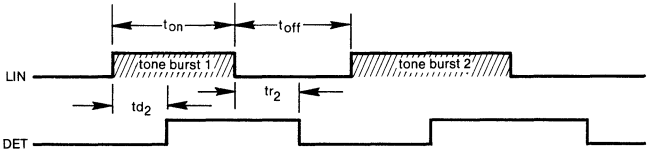


DTMF Generator

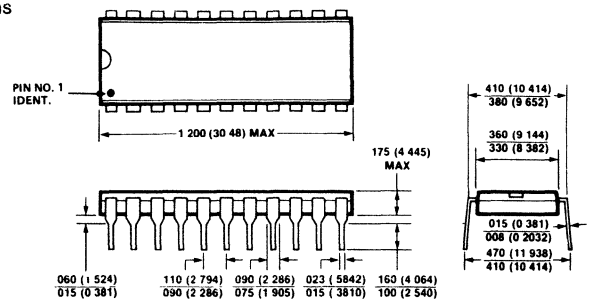


Note 1 The indicated time may be as small as 0 sec meaning that the $\overline{\text{LATCH}}$ and RESET lines may be tied together

Call Progress Detector



PLASTIC DIP
22 Pins



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SSI 957 DTMF Receiver with Dial Tone Reject Filter

Data Sheet

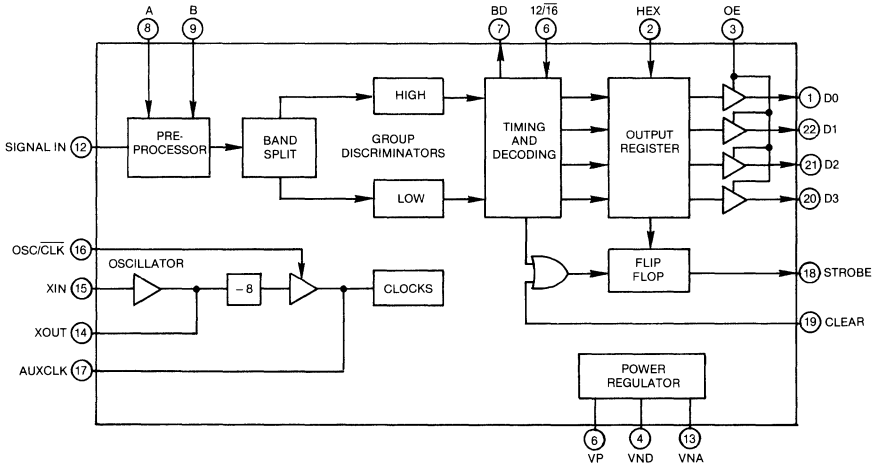
GENERAL DESCRIPTION

The SSI 957 combines switched-capacitor and digital frequency measuring techniques to decode Dual-Tone Multifrequency (DTMF) signals to four bit binary data. Dial tone rejection and 60 Hz noise rejection filters are built in. Fabricated as a monolithic integrated circuit using low power CMOS processing, the SSI 957 is packaged in a 22-pin DIP and operates from a single 5 through 12 volt DC supply. An inexpensive 3.58 MHz television crystal and a resistor are the only external components required. High system density may be achieved by using the clock output of one crystal connected receiver to drive the time bases of additional receivers.

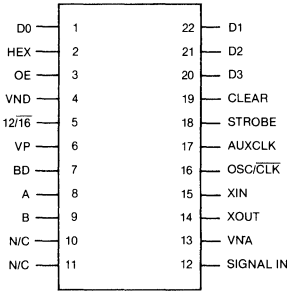
The SIGNAL IN input to the SSI 957 interfaces readily to telephone lines, radio receivers, tape players, and other DTMF signal sources. Inputs A and B control sensitivity to a maximum of −38 dBm, while the 12/$\overline{16}$ input determines the signals to be detected. The pre-processing stages of the SSI 957 filter out dial tone and noise, split the signal into its high frequency group and low frequency group components, and hard limit each component to provide automatic gain control. Four discriminators in each group then detect the individual tones. Post-processing stages of the SSI 957 time the tone durations and store binary data for outputting as determined by the HEX input. The STROBE output is activated by the presence of valid data in the output register and cleared by the detection of a valid end-of-signal pause or by the CLEAR input. An early signal presence indicator, BD, facilitates applications requiring tone blocking. The data outputs operate with simple logic circuits or microprocessors, and are tristate enabled to facilitate bus-oriented architectures.

FEATURES

- **Complete DTMF receiver in 22-pin DIP**
- **Decodes all 16 DTMF digits**
- **Excellent dial tone and speech immunity**
- **Meets telephone impulse noise immunity standards**
- **Digitally selectable sensitivity to −38 dBm**
- **Selectable 4-bit hexadecimal or binary-coded 2-of-8 output**
- **Fabricated using low-power CMOS technology**
- **Operates on single DC supply**
- **Uses inexpensive 3.58 MHz crystal**
- **Second source of Teltone M-957**



SSI 957 Block Diagram



Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

Table 1: Pin Functions

Pin	Function
SIGNAL IN	DTMF input. Timings are shown in Figure 1. Internally biased so that the input signal may be AC coupled. SIGNAL IN also permits DC coupling as long as the input voltage does not exceed the positive supply. Proper coupling is shown in Figure 3. See Table 3 for the frequency pairs associated with each DTMF signal.
12/$\overline{16}$	DTMF signal detection control. When 12/$\overline{16}$ is at logic "1", the SSI 957 detects the 12 most commonly used DTMF signals (1 through #). When 12/$\overline{16}$ is at logic "0", the SSI 957 detects all 16 DTMF signals (1 through D).
A, B	Binary DTMF signal sensitivity control inputs. A and B select the sensitivity of the SIGNAL IN input to a maximum of −38 dBm.
D3, D2, D1, D0	Data outputs. When enabled by the OE input, the data outputs provide the code corresponding to the detected digit in the format programmed by the HEX pin. See Table 3. The data outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. Timings are shown in Figure 1.
OE	Output enable. When OE is at logic "1", the data outputs are in the CMOS push/pull state and represent the contents of the output register. When OE is driven to logic "0", the data outputs are forced to the high-impedance or "third" state. Timings are shown in Figure 1.
HEX	Binary output format control. When HEX is at logic "1" the output of SSI 957 is full, 4-bit binary. When HEX is at logic "0", the output is binary coded 2-of-8. Table 3 shows the output codes.
STROBE	Valid data indication. STROBE goes to logic "1" after a valid tone pair is sensed and decoded at the data outputs. STROBE remains at logic "1" until a valid pause occurs or the CLEAR input is driven to logic "1", whichever is earlier. Once cleared, STROBE will not rise to a logic "1" until a new valid tone (preceded by a valid pause) is detected. Timings are shown in Figure 1.
CLEAR	STROBE control. Driving CLEAR to logic "1" forces the STROBE output to logic "0". When CLEAR is at logic "0", STROBE is forced to logic "0" only when a valid pause is detected. Tie to VNA or VND when not used.
BD	Button Down — A logic "1' BD indicates a signal has been detected and is being validated. BD precedes STROBE and Data outputs.
XIN, XOUT	Crystal connections. When an auxiliary clock is used, XIN should be tied to logic "1". See Figure 4.
OSC/$\overline{CLK}$	Time base control. WHen OSC/$\overline{CLK}$ is at logic "1", the output of the SSI 957's internal oscillator is selected as the time base. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1", the AUXCLK input is selected as the time base.
AUXCLK	Auxiliary clock input. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1", the AUXCLK input is selected as the SSI 957's time base. The auxiliary input must be 3.58 MHz divided by 8 for the SSI 957 to operate to specifications. If unused, AUXCLK should be left open.
VNA, VND	Negative analog and digital power supply connections. Separated on the chip for greater system flexibility, VNA and VND should be at equal potential.
VP	Positive power supply connection.
N/C	Not connected. These pins have no internal connection and may be left floating.

Table 2: Timing Parameters ($-40°C \le T_A \le +85°C$, $4.5V \le V_P \le 13.2V$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
TONE TIME: for detection	t_{ON}	40	—	—	ms
for rejection	t_{ON}	—	—	20	ms
PAUSE TIME. for detection	t_{OFF}	40	—	—	ms
for rejection	t_{OFF}	—	—	20	ms
DETECT TIME	t_D	25	—	46	ms
RELEASE TIME	t_R	35	—	50	ms
DATA SETUP TIME	t_{SU}	7	—	—	μs
DATA HOLD TIME	t_H	4.2	—	5.0	ms
STROBE CLEAR TIME	t_{CL}	—	160	250	ns
CLEAR PULSE WIDTH	t_{PW}	200	—	—	ns
BD DETECT TIME	BD	7	—	22	ms
BD RELEASE TIME	t_{ER}	2	—	18	ms
OUTPUT ENABLE TIME C_L = 50pF R_L = 1KΩ	—	—	200	300	ns
OUTPUT DISABLE TIME C_L = 35pF R_L = 500Ω	—	—	150	200	ns
OUTPUT RISE TIME C_L = 50pF	—	—	200	300	ns
OUTPUT FALL TIME C_L = 50pF	—	—	160	250	ns

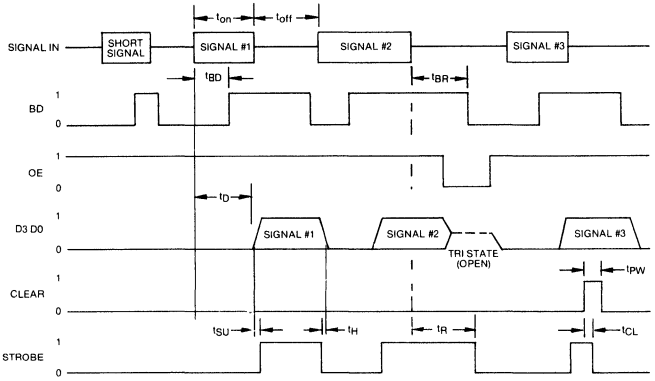


Figure 1. Timing Diagram

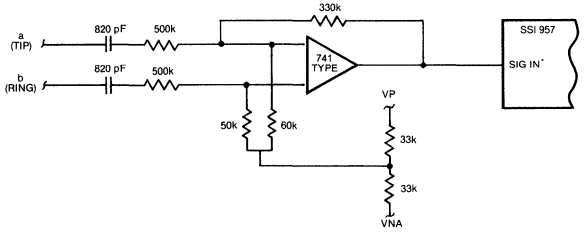


Figure 2. Telephone Line Differential Input Interface

Table 3: DTMF to Binary Decoding

DIGIT	LOW-FREQUENCY COMPONENT (Hz)	HIGH-FREQUENCY COMPONENT (Hz)	HEX OUTPUT	BINARY CODED 2 OF 8 OUTPUT
			D3 D2 D1 D0	D3 D2 D1 D0
1	697	1209	0001	0000
2	697	1336	0010	0001
3	697	1477	0011	0010
4	770	1209	0100	0100
5	770	1336	0101	0101
6	770	1477	0110	0110
7	852	1209	0111	1000
8	852	1336	1000	1001
9	852	1477	1001	1010
0	941	1336	1010	1101
*	941	1209	1011	1100
#	941	1477	1100	1110
A	697	1633	1101	0011
B	770	1633	1110	0111
C	852	1633	1111	1011
D	941	1633	0000	1111

Note: The SSI 957 detects signals A through D when the 12/$\overline{16}$ input is at logic "0"

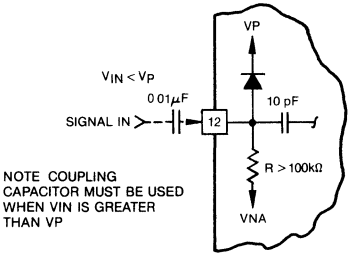


Figure 3. Input Signal Configuration

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (Note 2) ..... 16.0 V
Voltage on SIGNAL IN ..... (VP + 0.5V) to (V_P – 22 V)
Voltage on Any Pin Except
SIGNAL IN .....(VP + 0.5 V) to (VND – 0.5 V)
Storage Temperature Range ..... – 65° to 150°C
Operating Temperature Range ..... – 40° to 85°C
Lead Soldering Temperature .....260 °C for 5 seconds
Power Dissipation..... 1W

Notes
1 Exceeding these ratings may permanently damage the SSI 957
2 VP referenced to VND, VND should be a equal potential to VNA VND and VNA are normally grounded.

Table 4: Electrical Specifications ($-40°C \leq T_A \leq +85°C$)

Parameter		Conditions	Min	Typ	Max	Units	Notes
SIGNAL IN Input Requirements	Signal Level (per tone)	VP = 12V	—	—	—	—	—
		A = 0, B = 0	−24	—	+6	dBm	1
		A = 1, B = 0	−27	—	+3	dBm	1
		A = 0, B = 1	−30	—	0	dBm	1
		A = 1, B = 1	—	−32	—	dBm	1
		VP = 5V	—	—	—	—	—
		A = 0, B = 0	−32	—	−2	dBm	1
		A = 1, B = 0	−35	—	−5	dBm	1
		A = 0, B = 1	−38	—	−8	dBm	1
		A = 1, B = 1	—	−40	—	dBm	1
	Signal Frequency Deviation With Detection	—	—	±2.5%	±(1.5% + 2)	Hz	—
	Signal Frequency Deviation Without Detection	—	±3.5%	±3.0%	—	Hz	—
	Twist	—	—	—	±10	dB	2
	Gaussian Noise	—	—	12	A—7	dB	3
	Dial tone Level (per tone, F≤ 480 Hz)	—	—	—	A + 22	dB	4
Digital Input Requirements	Logic 0 Voltage	VP = 12V	0	—	3.6	V	5
		VP = 5V	0	—	1.5	V	5
	Logic 1 Voltage	VP = 12V	8.4	—	12.0	V	5
		VP = 5V	3.5	—	5.0	V	5
Digital Ouput Characteristics	Logic 0 Voltage	VP = 12V, I_O = 1.0mA	0	—	1.2	V	5
		VP = 5V, I_O = 0.4mA	0	—	0.5	V	5
	Logic 1 Voltage	VP = 12V, I_O = −0.5mA	10.8	—	12.0	V	5
		VP = 5V, I_O = −0.2mA	4.5	—	5.0	V	5
	Tri-State Leakage	—	—	—	10.0	μA	—
Miscellaneous Characteristics	CMOS Latch-up Voltage	—	20	—	—	V	7
	SIGNAL IN Input Impedance	F = 1kHz, paralleled with 15 pF	100k	—	—	Ω	—
Power Requirements	Supply Current	VP = 12V	—	20	40	mA	—
		VP = 5V	—	9	18	mA	—
	Power Dissipation (Outputs Open)	VP = 12V	—	204	480	mW	6
		VP = 5V	—	30	90	mW	6
	Power Supply Wide Band Noise (A = 0, B = 0)	VP = 12V	—	—	25	mVpp	—
		VP = 5V	—	—	10	mVpp	—

Notes

1 With an ambient temperature of 25°C, the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load (For example, −24 dBm equals 49 mVrms)

2 Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component

3 With an ambient temperature of 25°C, the signal level at A + 5, the signal frequency deviation and twist at 0, and the signal applied 50 ms off and 50 ms on The A level is the minimum detect level selected

4 With the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum The A level is the minimum detect level selected

5 Logic levels shown are referenced to VND

6 For an ambient temperature of 25°C

7 Power supply excursions above this value can cause device damage

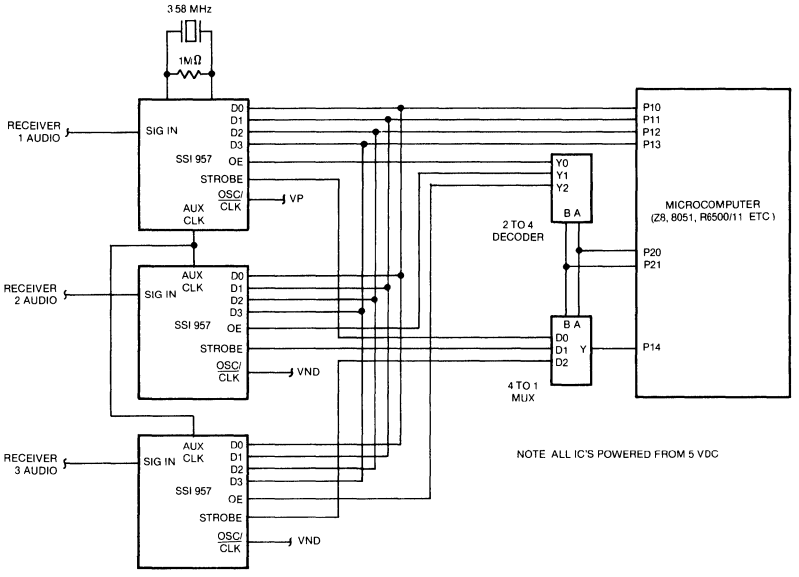
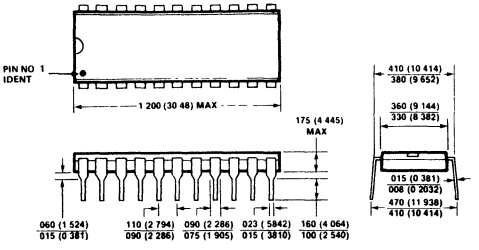


Figure 4. Multiple Receiver/Microprocessor Interface

PLASTIC DIP
22 Pins



CERDIP
22 Pins

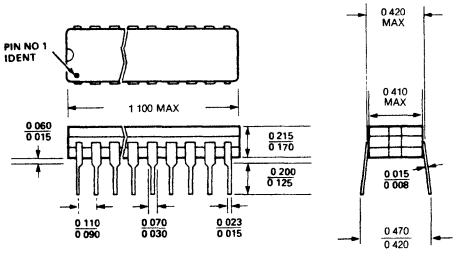


Figure 5. Package Dimensions

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SSI 980 Call Progress Tone Detector

Data Sheet

DESCRIPTION

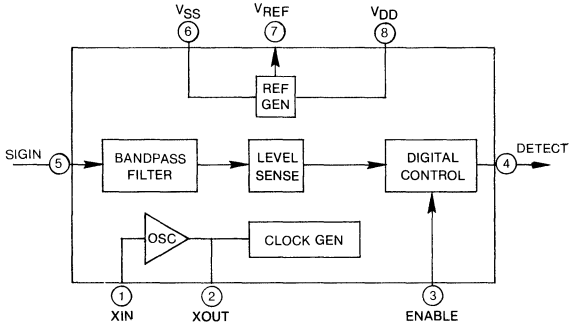
The SSI 980 Call Progress Tone Detector circuit allows automatic equipment to monitor tones in dial telephone systems that relate to the routing of calls. Such tones commonly include dial tone, circuits-busy tone, station-busy tone, audible ringing tones, and others. By sensing signals in the range of 305 to 640 Hz, the SSI 980 does not require the use of precision tones to function. This means that tones which vary with location or call destination can be detected regardless of their exact frequency. The SSI 980 is sensitive to signals from 0 dBm to – 40 dBm.

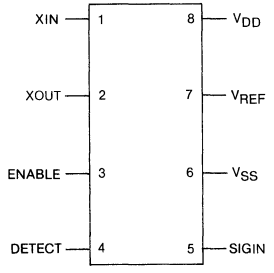
The low power CMOS switched capacitor filters used in the SSI 980 derive their accuracy from a 3.58 MHz clock, which in turn may be derived from other devices in the system being designed. The SSI 980 is available in plastic and ceramic DIP 8-pin packages.

FEATURES

- **Detects tones throughout the telephone progress supervision band (305 to 640 Hz)**
- **Sensitivity to – 40 dBm**
- **Dynamic range over 40 dB**
- **40 ms minimum detect (50 ms to output)**
- **Single supply CMOS (low power)**
- **Supply range 4.5 to 5.5 V DC**
- **Uses 3.58 MHz crystal or external clock**
- **8-pin DIP**
- **Second source of Teltone M-980.**

SSI 980 Block Diagram





Pin Out
(Top View)

Applications:
- Automatic Dialers
- Dialing Modems
- Billing Systems
- Service Supervision
- Test Equipment
- Traffic Measurement Equipment

CAUTION. Use handling procedures necessary for a static sensitive component

Table 1: Pin Functions

Pins	Function
SIGIN	Accepts analog input signal. Voltage levels given in Table 3, timing in Table 4.
DETECT	Call progress detect output. Goes to logic "1" when signal in 305-460 Hz band is sensed. See Table 4 for timing.
ENABLE	Application of logic "1" on this pin enables the output; logic "0" disables output.
V_{REF}	Supplies voltage at half V_{DD} for voltage reference of on-chip op amps.
XIN, XOUT	Crystal connections to on-chip oscillator circuit
V_{DD}	Positive power supply connection
V_{SS}	Negative power supply connection

Table 2:

Absolute Maximum Ratings*

DC Supply Voltage (V_{DD}-V_{SS}) . . . . . 16.0 V
Voltage on SIGNAL IN . . . . . V_{DD} + 0.5V to VSS – 22V
Voltage on Any Pin Except
SIGNAL IN . . . . . V_{DD} + 0.5V to V_{SS} – 0.5V
Storage Temperature Range . . . . . – 65 to 150 °C
Operating Temperature Range . . . . . 0 to 70 °C
Lead Soldering Temperature (for 5 sec) . . . . . 260 °C

*Exceeding these ratings may permanently damage the device

Table 3:

ELECTRICAL CHARACTERISTICS Ta = 25°C, $V_{DD} - V_{SS}$ = 4.5 to 5.5 V

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Current	$V_{dd} - V_{ss} = 5V$	—	4	10	mA
Signal level for Detection	305 – 640 Hz	– 40	—	0	dBm
Signal level for Rejection	305 – 640 Hz f > 1025 Hz, <190 Hz	— —	— —	– 50 0	dBm dBm
"Detect" output	Iout = + 1mA Logic 0 Logic 1	— — 4.5	— — —	— 0.5 —	— V V
"Enable", "XIN" input	Iin = 10μA Logic 0 Logic 1	— V_{SS} V_{DD} – 0.2	— — —	— V_{SS} + 0.2 V_{DD}	— V V
"XIN" Duty Cycle	—	40	—	60	%
"XIN", "XOUT" Loading	—	—	—	10	pF
"VREF" Output nominal = (V_{DD} + V_{SS})/2	Deviation Resistance	– 2 3.25	— —	+ 2 6.75	% kΩ
"SIGIN" input	Max Voltage Impedance (500 Hz)	V_{DD} – 10 80	— —	V_{DD} —	V kΩ

Note dBm is referenced to 600 Ω

Figure 1: Detect and Reject Regions

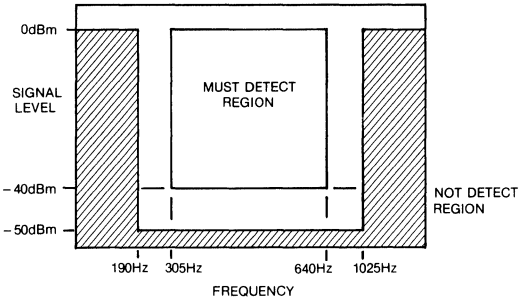


Table 4

TIMING CHARACTERISTICS Ta = 25°C, $V_{DD} - V_{SS} = 4.5$ to 5.5 V

Parameter	Conditions	Min.	Max.	Unit
Signal Duration for Detection (t_{MD})	305–640 Hz	40	—	ms
Signal Duration for Rejection (t_{ND})	305 – 640 Hz	—	20	ms
Interval Duration for Detection	Signal Dropping from: – 40 to – 50 dBm (t2) 0 to – 50 dBm (t1)	 40 90	 — —	 ms ms
Detect Time (t_D)	—	—	50	ms
Tone Dropout Bridging (t_B)	—	—	20	ms

Figure 2: Basic Timing

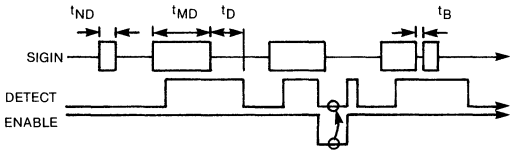


Figure 3: Effect of Amplitude on Timing

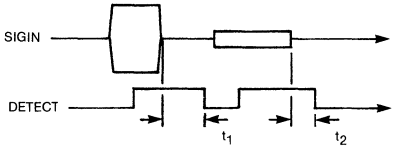


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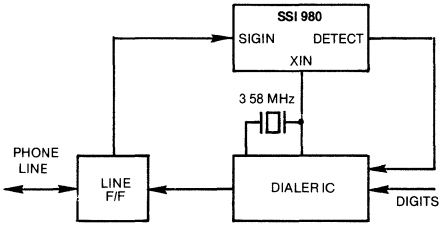
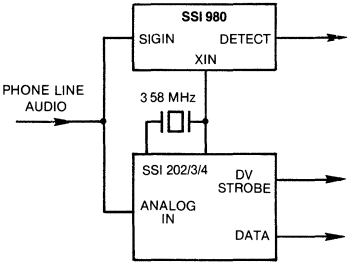
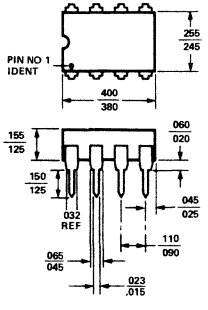
Figure 4: Applications Circuits



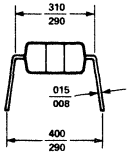
Dialer



DTMF Receiver



Plastic Dip 8-Pins



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SSI 981/982 Precise Call Progress Tone Detector

Data Sheet

DESCRIPTION

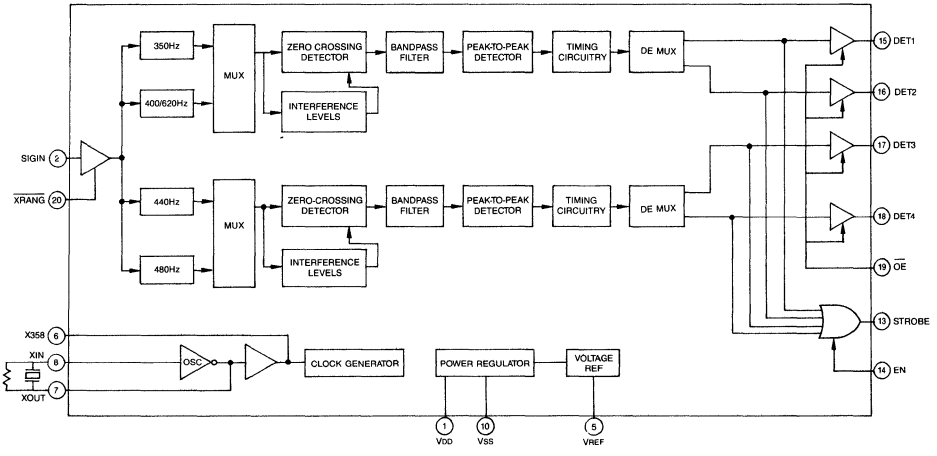
The SSI 981 and 982 Precise Call Progress Tone Detector circuits enable automatic monitoring of tones in dial telephone systems for the purpose of routing calls. Built using CMOS switched capacitor technology, each has four independent channels for detecting precise tones in the 305 to 640 Hz range. The outputs of the channels have a response related to the respective tone durations.

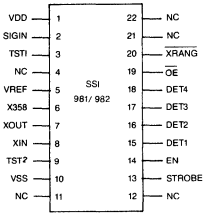
The SSI 981 and 982 are identical except for the tones detected. The SSI 981 will decode 350Hz, 400Hz, 440Hz and 480Hz. The SSI 982 will decode 350Hz, 440Hz, 480Hz and 620Hz tones.

FEATURES

- **Detects & decodes precise tones throughout 305-640Hz telephone progress band**
- **35dB dynamic range**
- **Single supply CMOS (low power)**
- **Adjustable gain sensitivity**
- **Supply range 4.5 to 5.5 VDC**
- **Uses 3.58 MHz crystal**
- **Three-state outputs**
- **Standard 22-pin DIP**
- **Second source to Teltone M981 and M982**

SSI 981/982 Block Diagram





Pin Out (Top View)

Figure 1

CAUTION: Use handling procedures necessary for a static sensitive component

CIRCUIT OPERATION

The functional block diagram is shown in figure 1. Channels 1 and 2, and 3 and 4 are multiplexed, respectively as shown. Each channel starts with a 4-pole band-pass filter that reduces the amplitude of out-of-band signals. The output of the front-end filter is fed into two circuits, one being a zero-crossing detector which functions as a limiter-AGC, and the other being a circuit that controls the level of the interference floor based on the level of the incoming signal. The output of the ZCD, an energy-limited signal, is fed into a peak-to-peak detector that determines if the precise frequency is present by checking the amplitude of the signal from the back-end filter. Pulses from the peak-to-peak detector, which indicate the presence of the precise tone, are counted to time the duration of the input pulsed-tone. If the criteria of the specifications are met, the appropiate detect output goes to the high state. As shown in figure 1, all circuitry after the front-end filters is multiplexed. A digital demultiplexer follows the P-P detector to provide the four distinct outputs.

SIGIN

The input signal is applied to the SIGIN pin and is AC-coupled into the front-end filters. The SSI 981 and 982 can amplify a low level signal by 10dB when the $\overline{\text{XRANG}}$ pin is held low.

DET OUTPUTS & OE

Outputs DET1-4 are CMOS push-pull when enabled (OE ="1") and high impedance when disabled (OE ="0"). A "1" on a Det pin indicates that the appropiate valid tone pulse was detected (see table 2). Detect timing is shown is figure 2.

STROBE & EN

The STROBE pin is the logical OR of the DETn outputs and will indicate when any one of the four call progress tones has been detected. STROBE is unaffected by OE but goes to a high impedance state when EN="0".

XIN, XOUT & X358

Internal timing and clocks are derived from the 3.58MHz clock. The SSI 981 and 982 contain an on-board inverter with sufficient gain to provide oscillation when connected to a low cost "colorburst" crystal. The crystal is connected between XIN an XOUT. A 1Mohm 10% resistor is also connected between these pins. In this mode, X358 is a clock frequency output available to drive other parts requiring the same frequency.

The part will also operate with an external digital clock (duty cycle 40% to 60%).

VREF

Internal analog signal reference voltage. Noise or interference coupled onto this pin may degrade chip functionality.

TST1 & TST2

Manufacturer's special test pins.

Table 1:
TIMING CHARACTERISTICS TA = 25°C, V_{DD} - V_{SS} = 4.5V to 5.5V

Parameter	Conditions	Min	Max	Units
Signal Duration for Detection t_{DD}	In band, see Table 1	200	—	ms
Time to Detect, t_{DD}		—	200	ms
Bridge Time, t_B		—	30	ms
Signal Duration for Rejection t_{ID}	Noise at SIGIN: −50dBm, 0.2–3.4 kHz	160	—	ms
Time to Release t_{RD}		—	200	ms
Interval Duration for Detection of both Signals	High to Low; High, 0 dBm Low, −25 dBm	1	—	s
DETn pin Enable Time, t_{EN} Z to Low or High	C_L = 50pF, R_L = 100kΩ	—	100	μs
DETn pin Disable Time, t_{DS} Low or High to Z		—	100	μs

Figure 2: TIMING CHARACTERISTICS

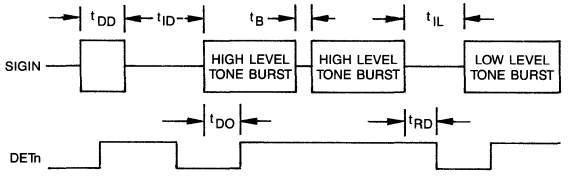


Table 2: FREQUENCY DETECTION

Signal Present (fo)		DET1	DET2	DET3	DET4	OE	STROBE	EN
981	982							
350Hz	350Hz	1	X	X	X	1	1	1
400Hz	620Hz	X	1	X	X	1	1	1
440Hz	440Hz	X	X	1	X	1	1	1
480Hz	480Hz	X	X	X	1	1	1	1
Other In-Band		0	0	0	0	1	0	1
Any		High Impedance				0	0	0

NOTE: Out of band tones may cause short detect pulses if at sufficient amplitude and pulsed duration.

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$)

Parameter	Test Conditions	Min	Max	Units
VDD		4.5	5.5	V
Oscillator Frequency Deviation (at XOUT) from 3.57959 MHz		−0.01	+0.01	%
Power Supply Noise (0.1 – 5) KHz		—	20	mVp-p
Current Drain (VDD = 5.5V, TA = 0°C)		—	30	mA
Must Detect Signal:				
Frequency Range	In Band, see Table 1	−1.0	+1.0	% of fo
Level (2)		−25	0	dBm
Must Reject Signal:	Noise at SIGIN	—	−50	dBm
Level	−50 dBm, 0.2 to 3.4 kHz			
Level Skew between (4) Adjacent In-Band Signals for Detection of Both		—	6	dB
Steady State Responser:	fo − 5% >f >fo + 5%	—	0	dBm
Must Reject Level (3)	See Table 1			
SIGN Pin:				
Voltage Range		VDD − 10	VDD	V
Input Impedance	f = 500 Hz	80		KΩ
			15	pF
Gain	$\overline{XRANG}$ = 0	9.9	10.1	dB
$\overline{XRANG}$ Pin:				
VIL		—	0.5	V
VIH		VDD − 2.0	—	V
Pullup Current	$\overline{XRANG}$ = VSS	—	−10	μA
Detect Pins, DETn:				
VOL	ISINK = −1mA	—	0.5	V
VOH	ISOURCE = 1mA	VDD − 0.5	—	V
IOZ	VO = VDD, VSS	—	1	μA
STROBE Pin:				
VOL	ISINK = −1mA	—	0.5	V
VOH	ISOURCE = 1mA	VDD − 0.5	—	V
OE, ENABLE Pin:				
VIL		—	0.5	V
VIH		VDD − 2.0	—	V
Pullup Current	OE, Enable = VSS	—	−10	μA
External Clock:	XOUT Open			
VIL		—	0.2	V
VIH		VDD − 0.2	—	V
Duty Cycle		40	60	%
XIN, XOUT Loading	Crystal Oscillator Active			
Capacitance		—	10	pF
Resistance		20	—	MΩ
X358 Pin:	CL = 20 pF			
VOL	ISINK = −10 μA	—	0.2	V
VOH	ISOURCE = 10 μA	VDD − 0.2	—	V
Duty Cycle		40	60	%

Notes

(1) All parameters are specified at VDD = 5 volts and $\overline{XRANG}$ at a logical "hi" state, which implies unity front-end gain Power levels in dBm are referenced to 600Ω

(2) A post-filter AGC is employed to enhance end-of-tone detection for high-level signals A drop in amplitude of the input tone may cause an end-of-tone (interval) indication

(3) Large input voltage transients may cause excessive ringing in the highly selective filter, causing spurious detection The detects are not considered as incorrect circuit operation

(4) Any tone 40Hz - 1% from fo must adhere to this specification, where fo is defined in Table 1

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Absolute Maxumum Ratings *

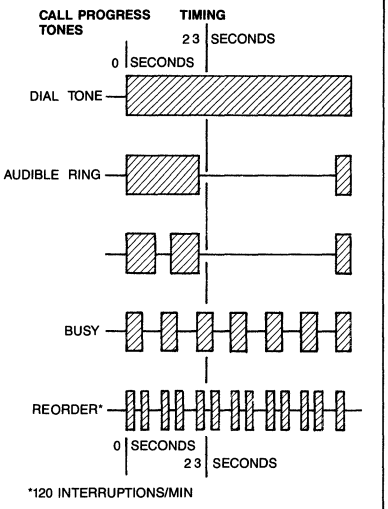
DC Supply Voltage (V_{DD} - V_{SS}) ..... +7V
Voltage on any pin except SIGIN V_{SS} −0.3V to V_{DD} +0.3V
Voltage on SIGIN ..... V_{DD} −18V to V_{DD} +0.3V

Storage Temperature Range ..... −65° C to 150° C
Operating Temperature Range ..... 0° C to 70° C
Lead Soldering Temperature ..... 260° C

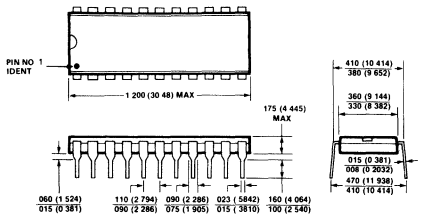
* Exceeding these ratings may permanently damage this device

Normal Call Progress Tones And Sequence

Tone	Frequency (Hz)	Cadence
Precision Dial Tone	350 +440	continuous
Old Dial Tones	600 +120 or 133. and other combinations	continuous
Precision Busy	480 +620	0.5 s on 0.5 s off
Old Busy	600 +120	0.5 s on 0.5 s off
Precision Reorder	480 +620	0.3 s on local 0.2 s off reorder
Old Reorder	600 +120	0.2 s on toll 0.3 s off reorder 0.25 s on toll 0.25 s off local
Precision Audible Ringback	440 +480	2 s on 4 s off
Old Audible Ringback	420 +40 and other combinations	2 s on 4 s off



PLASTIC DIP
22 Pins



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SSI K212 Single Chip Bell 212 Modem

Preliminary Data Sheet

INTRODUCTION

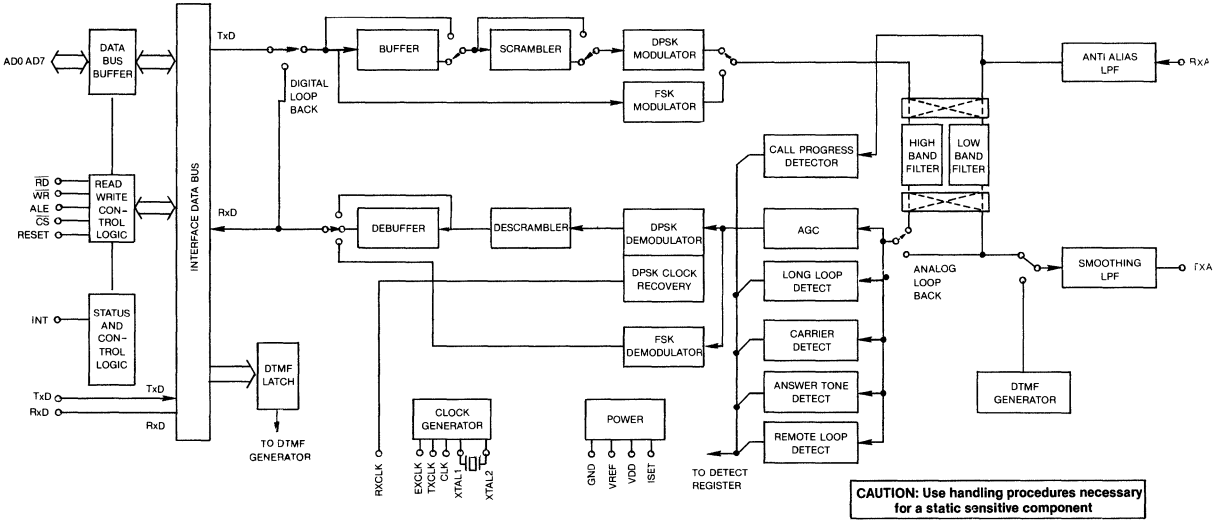
The SSI K212 is a true single-chip modem device that provides the functions needed to construct a typical Bell 212A standard full-duplex modem. Using an advanced CMOS process that integrates analog, digital, and switched-capacitor array functions on a single substrate, the SSI K212 offers excellent performance and a high level of functional integration in a single 28 pin DIP configuration. The K212 provides the basic PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes, and a DTMF dialer. This device supports all Bell 212A modes of operation, allowing both synchronous and asynchronous communication. The K212 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communication occurs through a separate serial port only.

The K212 is ideal for use in either freestanding or integral-system modem products where full-duplex 1200 BPS data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converters for a typical system The use of coherent demodulation techniques also assures the user of optimum performance when communicating over degraded lines.

FEATURES

- **One-chip fully Bell 103/212A compatible modem**
- **Full duplex operation at 0-300 and 1200 BPS**
- **FSK (300 BPS) or PSK (1200 BPS) encoding**
- **Compatible with standard microprocessors (8048, 80C51 typical)**
- **Serial (22 Pin DIP) or parallel microprocessor bus interface (28 Pin DIP)**
- **Maskable interrupts**
- **Serial port for data transfer**
- **Selectable asynch/synch and scrambler/descrambler functions**
- **Coherent demodulation technique provides optimal performance**
- **Call progress, carrier, and long-loop detect monitor**
- **DTMF tone generator**
- **Test modes available – ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Space efficient 22-pin DIP, 28-pin DIP and Quad packages**
- **CMOS technology for low power consumption (120 mW)**
- **Low power IDLE mode uses < 10mW**
- **Single +12 V supply**
- **TTL and CMOS compatible inputs and outputs**

BLOCK DIAGRAM



OPERATION

General

The SSI K212 was designed to be a complete Bell 212A compatible modem on a chip. As many functions as deemed economically feasible were included in order to simplify implementation into typical modem designs. In addition to the basic 1200 BPS PSK and 300 BPS FSK modulator/demodulator sections, the device also includes synch/asynch converters, scrambler/descrambler, call progress tone detect, and DTMF tone generator capabilities. All Bell 212A modes are supported (synchronous and asynchronous) and test modes are provided for diagnostics. Most functions are selectable as options and logical defaults are provided when override modes are selected. The device can be directly interfaced to a microprocessor via its 8-bit multiplexed address/data bus, or a serial command interface can be used (22-pin version) reducing the number of control lines required. Data communication takes place through a serial port.

PSK Modulator/Demodulator

The K212 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (Originate mode) or 2400 Hz carrier (Answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (Answer mode or ALB Originate mode) or a 2400 Hz carrier (Originate mode or ALB Answer mode) The K212 uses a phase-locked-loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers

FSK Modulator/Demodulator

The FSK modulator frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 Hz and 1070 Hz (originate mark and space) and 2225 and 2025 (answer mark and space) are used. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 mode.

Passband Filters and Equalizers

A high and low band filter is included to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out of band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering corresponds to a 75% square root of raised Cosine frequency response characteristic.

Asynchronous Mode

The asynchronous mode is used for communication with asynchronous terminals which may communicate at 1200 BPS +1%, −2.5% even though the modem's output is limited to 1200 BPS ± 0 01%. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is 1200 BPS ± 0.01%. This signal is then routed to a data scrambler (following the CCITT V.22 algorithm) and into the analog PSK modulator where dibit encoding results in a Bell 212A standard PSK output signal. Both the rate converter and scrambler can be bypassed for handshaking, FSK, and synchronous operation. The device recognizes a break signal and handles it in accordance with Bell 212A specifications. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than 1219 BPS. An incoming break signal will be passed through without incorrectly inserting a stop bit.

Synchronous Mode

The Bell 212A standard defines synchronous operation only at 1200 BPS. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TxD must be valid on the rising edge of TxCLK. Receive data at the RxD pin is clocked out on the falling edge of RxCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input

Parallel Bus Interface

Four 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the A0 and A1 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the DTMF register are read or write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

Serial Command Interface

The serial command mode allows access to the K212 control and status registers via a serial command port (22 pin version only). In this mode the A0 and A1 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of ExCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of ExCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

Special Detect Circuitry

The special detect circuit monitors carrier, call-progress tones, answer tone, long loop (weak received signal), and remote-digital-loopback-request bit pattern. The appropriate status bit is set when one of these conditions changes and an interrupt is generated.

DTMF Generator

The DTMF generator will output one of 16 standard dual-tones determined by the 4-bit binary value previously loaded into the DTMF register. Dialing is initiated when the DTMF mode is selected and the transmit enable bit is changed from a 1 to a 0.

HARDWARE INTERFACE **Pin No.**

	I/O	Signal Label	28 Pin	22 Pin	Description
POWER					
	I	GND	28	1	System ground.
	I	Vdd	15	11	Power supply input, +12 volt +10%, −20%
	O	Vref	26	21	An internally generated reference voltage for test use. Bypass with .1μF cap. to ground.
	I	ISET	24	19	Chip current reference. Sets bias current for op-amps. Programmed by connecting to Vcc through 2 Meg Ω resistor. Power dissipation/ performance tradeoff results from varying this value.
MICROPROCESSOR INTERFACE					
	I	ALE	12	–	Address latch enable. The falling edge of ALE latches the address on AD0-AD2.
	I/O	AD0-AD7	4-11	–	Address/data bus. This is a bidirectional, tri-state, multiplexed address and data bus.
	I	$\overline{CS}$	20	–	Chip select Allows access to device data and address bus. AD0-AD7 will be in a high impedance state unless $\overline{CS}$ is low. $\overline{CS}$ is latched on the falling edge of ALE.
	O	CLK	1	2	Clock output. This pin outputs either the crystal frequency (for use as a processor clock) or a 16x1200 Hz signal for use as a baud clock.
	O	$\overline{INT}$	17	13	Interrupt flag to processor When low, indicates that a detect condition has occurred. Reset when the detect register is read or a reset is performed.
	I	$\overline{RD}$	14	–	Read control When low puts addressed register into a read condition. $\overline{CS}$ must also be low.
	I	Reset	25	20	Resets device when in high state, setting all register bits to zero and CLK to Xtal frequency. An internal pulldown resistor allows power on reset by connecting a 1μf capacitor between reset and Vcc.
	I	$\overline{WR}$	13	–	Write control. A low indicates that data is available Data is latched on the rising edge of $\overline{WR}$. $\overline{CS}$ must be active.
RS-232 INTERFACE					
	I	ExCLK	19	15	External clock input. Used in synchronous modes when external timing is selected. ExCLK becomes the phase-lock reference for TxCLK.
	O	RxCLK	23	18	Receive clock output. Carrier derived synch clock. Falling edge coincides with received data output transitions. Rising edge can be used to latch valid output data. Active when carrier present.
	O	RxD	22	17	Received digital data output. In synchronous or asynchronous mode, data is valid on rising edge of RxCLK.
	O	TxCLK	18	14	Transmit clock output. Used in synchronous mode to latch input data on the TxD pin. Data must be valid on the rising edge of TxCLK. TxCLK is an internally generated 1200 Hz reference in internal mode, phase locked to ExCLK in external mode, and derived from RxCLK in slave mode. TxCLK is always active.
	I	TxD	21	16	Transmit digital data input. In synch modes the data must be valid on the rising edge of TxCLK. In Asynch modes no clocking is necessary. High speed data must be 1200 +1%, −2.5%.

HARDWARE INTERFACE **Pin No.**

	I/O	Signal Label	28 Pin	22 Pin	Description
ANALOG INTERFACE					
	I	RxA	27	22	Received modulated analog signal input.
	O	TxA	16	12	Transmit analog output.
	I	Xtal 1	2	3	Connection for external 11.0592 MHz crystal or CMOS level clock signal.
	I	Xtal 2	3	4	Connection for external 11.0592 MHz crystal
SERIAL INTERFACE					
	I	A0-A1	–	5-6	Register address selection. These lines should be valid during any read or write operation.
	I/O	Data	–	8	Serial control data. Data for a read/write operation is clocked in or out on the falling edge of the ExCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
	I	$\overline{RD}$	–	10	Read data control. A low enables a read operation from the addressed register. Data is clocked out on transitions of the ExCLK (LSB first) while the $\overline{RD}$ line is low. Eight cycles of ExCLK are needed to transfer the full 8 bits of data contained in one register.
	I	$\overline{WR}$	–	9	Write data control. A low to high transition on this line causes 8 bits of data previously shifted in (LSB first) to be transferred to the addressed register.

Operating Limits — Absolute Maximums — SSI K212

Parameter	Max	Unit
VDD supply voltage	14	V
Storage temperature	– 65 to 150	°C
Lead temperature (10 sec.)	260	°C
TTL compatible inputs	0 to V_{DD}	V
TTL compatible outputs	– 0.3 to V_{DD}	V
TTL compatible outputs	± 3	mA

Notes: 1. All inputs and outputs are protected from static charge using built-in industry standard protection devices.
2. All outputs are short-circuit protected.

BUS INTERFACE

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines (latched by ALE in parallel mode). Control and status bits are identified below:

A0	A1	Register	Function
0	0	CR0	Control register 1
0	1	CR1	Control register 2
1	0	DR	Detect register (read only)
1	1	DTMF	DTMF transmit tones

	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
CR0	00	SSI TEST	0	LOW SPEED	TX MODE BIT 2	TX MODE BIT 1	TX MODE BIT 0	TX ENABLE	ORG/ ANS
CR1	01	TX TEST BIT 1	TX TEST BIT 0	EN INT DETECT	BYPASS SCR	CLK SELECT	RESET	TEST MODE BIT 1	TEST MODE BIT 0
CR2	10	0	0	RCV DATA	RDL	CD	ANS TONE	CALL PROG	LONG LOOP
CR3	11	RXD OPEN	0	TX ANS TONE	TX DTMF	DTMF BIT 3	DTMF BIT 2	DTMF BIT 1	DTMF BIT 0

CONTROL REGISTER 0 – CR0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0	SSI TEST	0	LOW SPEED	TX MODE BIT 2	TX MODE BIT 1	TX MODE BIT 0	TX ENABLE	ORG/ANS

0 = NORMAL
1 = INVALID

1 = 300 BPS
0 = 1200 BPS

000 = PWR DOWN
001 = INT SYNCH
010 = EXT SYNCH
011 = SLAVE SYNCH
100 = ASYCH 8 BITS/CHAR
101 = ASYCH 9 BITS/CHAR
110 = ASYCH 10 BITS/CHAR
111 = ASYCH 11 BITS/CHAR

1 = TX
0 = TX OFF

1 = ORG
0 = ANS

CONTROL REGISTER – CR1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1	TX TEST BIT 1	TX TEST BIT 0	INT EN	SCR EN	CLK CONTROL	RESET	TEST MODE BIT 1	TEST MODE BIT 0

00 = TX DATA
01 = TX ALTERNATE
10 = TX MARK
11 = TX SPACE

ENABLE INTERRUPT
1 = ON
0 = OFF

0 = ON
1 = OFF

0 = XTAL
1 = 16X1200

RESET

00 = NORMAL
01 = ANALOG LOOPBACK
10 = REMOTE DIGITAL LOOPBACK
11 = LOCAL DIGITAL LOOPBACK

DETECT REGISTER – DR

	D7	D6	D5	D4	D3	D2	D1	D0
CR2	0	0	RCV DATA	RDL	CD	ANS TONE	CALL PROG	LONG LOOP

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
CR3	RXD OPEN	0	TX ANS TONE	TX DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

1 = TRI STATE
0 = NORMAL

1 = ON
0 = OFF

1 = TX DTMF
0 = DATA

–4-BIT CODE FOR 1 OF 16 DUAL-TONE COMBINATIONS–

Operating Conditions — SSI K212

Parameter	Test Conditions	Min	Nom	Max	Units
Power supply					
VDD supply voltage		9.6	12	13.2	V
VDD supply current	3.9 MΩ resistor ISET – V_{DD}	—	—	15	mA
VDD supply current	Power down mode	—	—	5	mA
External Components					
VREF bypass capacitor	External to ground	0.1	—	—	μF
Bias setting resistor	Between V_{DD} and ISET	—	2	—	MΩ
VDD bypass capacitor	External to ground	0.1	—	—	μF
Input Clock variation	11.0592MHz input xtal	– 0.01	—	+ 0.01	%
Environmental					
Ambient temperature	—	0	—	70	°C
Input/Output					
Input high voltage	Vih	2	—	—	V
Input low voltage	Vil	—	—	0.8	V
Input high current	Input voltage = 7 V	—	—	100	μA
Input low current	Input voltage = 0 V	– 200	—	—	μA
Input capacitance		—	—	10	pF
Output high voltage	Iout = – 0.4 mA	2.4	—	5	V
Output low voltage	Iout = 1.6 mA	—	—	0.4	V
Crystal Oscillator					
Load capacitance	XTAL 1, Xtal 2	10	—	30	pF
XTAL 1 input high	Vih	4.0	—	—	V
XTAL 1 input low	Vil	—	—	0.8	V
CLK output high level	Iout = – 0.1 mA	2.4	—	5	V
CLK output low level	Iout = 1.6 mA	—	—	0.4	V
Bus Interface					
Address before latch	tAL	30	—	—	ns
Address hold after latch	tLA	20	—	—	ns
Latch to RDB/WDB control	tLC	40	—	—	ns
Data out from RDB	tRD	140	—	—	ns
ALE width	tLL	60	—	—	ns
Data float after read	tRDF	0	—	80	ns
Read width	tRW	200	—	5000	ns
Write width	tWW	140	—	5000	ns
Data setup before write	tDW	150	—	—	ns
Data hold after write	tWD	20	—	—	ns
PSK Modulator					
Carrier suppression	measured at TXA	55	—	—	dB
Transmitter gain variation	measured at TXA	– 0.5	—	0.5	dB
Output Amplitude	TX scrambled marks ···	– 10.5	– 10.0	– 9.5	dBm0

Operating Conditions — SSI K212

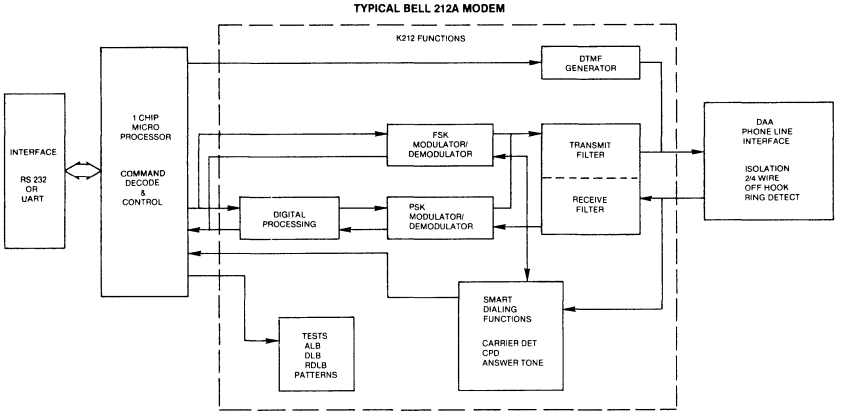
Parameter	Test Conditions	Min	Nom	Max	Units
FSK Mod/Demod					
Output frequency error	1070 Hz Txd = 0	−0.31	—	0.31	%
	1270 Hz Txd = 1	−0.32	—	0.32	%
	2025 Hz Txd = 0	−0.19	—	0.19	%
	2225 Hz Txd = 1	−0.43	—	0.43	%
Output amplitude	—	−10.5	−10.0	−9.5	dBm0
Output distortion	—	—	—	−20	dB
Output bias distortion	Alternate m/s input	−5	—	+5	%
Output jitter	Random input — varying duty cycle	−5	—	+5	%
DTMF Generator					
Output accuracy	697 Hz	−0.14	—	0.14	%
	770 Hz	−0.26	—	0.26	%
	852 Hz	−0.27	—	0.27	%
	941 Hz	−0.35	—	0.35	%
	1209 Hz	−0.30	—	0.30	%
	1336 Hz	−0.26	—	0.26	%
	1477 Hz	−0.00	—	0.00	%
	1633 Hz	−0.64	—	0.64	%
Output amplitude	Low band	−9.5	—	−8.5	dBm0
	High band	−7.5	—	−6.5	dBm0
Output distortion	—	—	—	−20	dB
Long loop detector					
Detect long loop	—	−37	—	−32.5	dBm0
Call Progress Detector					
Detect level	350 to 620 Hz band	−34	—	0	dBm0
Reject level		—	—	−40	dBm0
Delay time		—	—	20	ms
Hold time		—	—	10	ms
Hysterisis		2	—	—	dB
Carrier Detect					
Upper threshold	At RXA with 1200/2400 Hz input	—	—	−43	dBm0
Lower threshold	At RXA with 1200/2400 Hz input	−48	—	—	dBm0
Hysterisis	At RXA with 1200/2400 Hz input	2	—	—	dB
Delay time	1200/2400 Hz input	10	20	30	ms
Hold time	1200/2400 Hz input	5	10	15	ms
Answer Tone Detector					
Detect on	—	−43	—	—	dBm0
Detect off	—	—	—	−48	dBm0

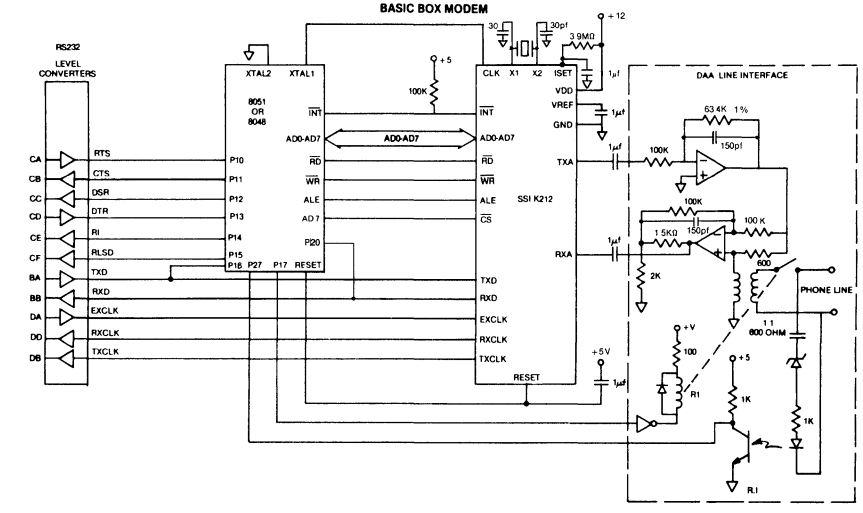
Note dBm0 refers to an output level of 0 dBm at the line side of the DAA specified in the following section The DAA introduces a +9 0 dB receive gain and a −10 0 dB loss on the transmit side The K212 transmits nominally at 0 0 dBm (775Vrms) at its TXA pin with −10 0 dBm0 output from the DAA to the phone line It receives a nominal +9 0 dBm signal (2 18Vrms) at its RXA pin with a 0 dBm0 signal input from the phone line

Application

The SSI K212 is designed to be used in conjunction with a microprocessor and RS-232 serial lines or parallel bus interface, and a DAA phone line interface to function as a typical intelligent modem. The K212 interfaces directly with 8048/8051 family microprocessors for this purpose. Figure 1 shows the components making up the typical intelligent modem and that portion of the system contained in the K212. Figure 2 shows a basic modem circuit for the stand-alone modem (self-contained box), which functions as described in the following section.

A typical intelligent modem consists of the mod/demod block, phone line and terminal interfaces, and a dedicated control microprocessor as shown in the block diagram. The SSI K212 has two busses — a parallel or serial bus for control or status monitoring, and a serial bus for data transfer. Either a serial or parallel interface can be used to transfer data (and commands) between the modem and terminal, but the actual data path is through the serial port. A dedicated microprocessor monitors the TXD line from the terminal, interprets commands in the data stream, and takes control action in response to these commands by using the K212's control bus to access its four internal registers. The received data path is monitored by passing received data through the control processor to allow sending messages back to the terminal for status indication. The mod/demod block performs the actual Bell 212A communications link, which includes asynchronous buffer/debuffer functions, scrambler/descramber, and 1200 and 0-300 BPS modulation/demodulation. DTMF dialing capability allows the modem to dial its own calls. Call progress detection expands this capability by giving the modem the ability to detect dial tone, busy signal, or ringback, and to change its calling action in response to these detected signals. An FCC approved DAA section completes the modem by providing a connection to the dial-up phone line.





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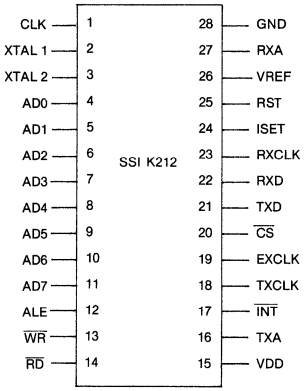

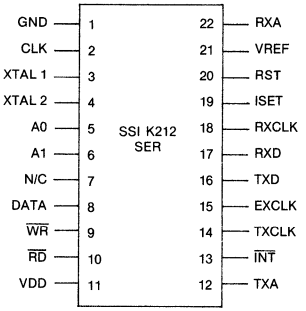

Pin Out
(Top View)

Telecommunications Circuits

Device	Circuit Function	Features	Power Supplies	Package
Tone Signaling Products				
SSI 201	Integrated DTMF Receiver	Binary or 2-of-8 output	12V	22 DIP
SSI 202	Integrated DTMF Receiver	Low-power, binary output	5V	18 DIP
SSI 203	Integrated DTMF Receiver	Binary output, Early Detect	5V	18 DIP
SSI 204	Integrated DTMF Receiver	Low-power, binary output	5V	14 DIP
SSI 207	Integrated MF Receiver	Detects central office tone signals	10V	20 DIP
SSI 957	Integrated DTMF Receiver	Early Detect, Dial Tone reject	5V	22 DIP
SSI 20C89	Integrated DTMF Transceiver	Generator and Receiver, µP interface	5V	22 DIP
SSI 20C90	Integrated DTMF Transceiver	Generator and Receiver, µP interface, Call Progress Detect	5V	22 DIP
SSI 980	Call Progress Detector	Detects supervision tones, Teltone second-source	5V	8 DIP
SSI 981	Precise Call Progress Detector	Detects supervision tones, Teltone second-source	5V	22 DIP
SSI 982	Precise Call Progress Detector	Detects supervision tones, Teltone second-source	5V	22 DIP
Modem Products				
SSI K212	1200/300 bps Modem	DPSK/FSK, single chip, autodial, Bell 212A	10V	28 DIP
SSI K214	2400 bps Analog Front End	Analog Processor for DSP V 22 bis Modems	10V	28 DIP
SSI K222	1200, 600, 300 bps Modem	DPSK, FSK, single chip, autodial, V 22	5V	28 DIP
SSI 223	1200 bps Modem	FSK, HDX/FDX	10V	16 DIP
SSI K224	2400 bps Modem	QAM, DPSK, FSK single chip V 22 bis	10V	28 DIP
SSI 291/213	1200 bps Modem	DPSK, two chips, low-power	10V	40/16 DIP
SSI 3522	1200 bps Modem Filter	Bell 212 compatible, AMI second-source	10V	16 DIP
Speech Synthesis Products				
SSI 263A	Speech Synthesizer	Phoneme-based, low data rate, VOTRAX second-source	5V	24 DIP
Switching Products				
SSI 80C50	T1 Transmitter	Bell D2, D3, D4, serial format and mux, low power	5V	28 DIP,Q
SSI 80C60	T1 Receiver	Bell D2, D3, serial synchron and demux, low power	5V	28 DIP,Q
SSI 22100	Cross-point Switch	4x4x1, control memory, RCA second-source	12V	16 DIP
SSI 22101/2	Cross-point Switch	4x4x2, control memory, RCA second-source	12V	24 DIP
SSI 22106	Cross-point Switch	8x8x1, control memory, RCA second-source	5V	28 DIP
SSI 22301	PCM Line Repeater	T1 carrier signal recondition	5V	18 DIP

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INNOVATORS IN INTEGRATION

SSI K214 Analog Processor for DSP-Based V.22 bis Modems

Preliminary Data Sheet

PRODUCT DESCRIPTION

The SSI K214 is a complete analog front end for digital signal processor based V.22 bis and Bell 212A compatible modems. The K214 provides bandsplit filters, fixed compromise equalization, signal path, programmable gains, and the clocks for transmit and receive activities. An 8-bit A/D convertor is available for receive signal processing, and on-chip modulators provide the QAM, PSK, and FSK transmit signals, making it unnecessary for the DSP to perform the transmit functions. A tone generator is used to produce DTMF, answer, and guard tones while an analog loopback mode allows system testing. Level detectors indicate carrier answer tone and call progress tone detection.

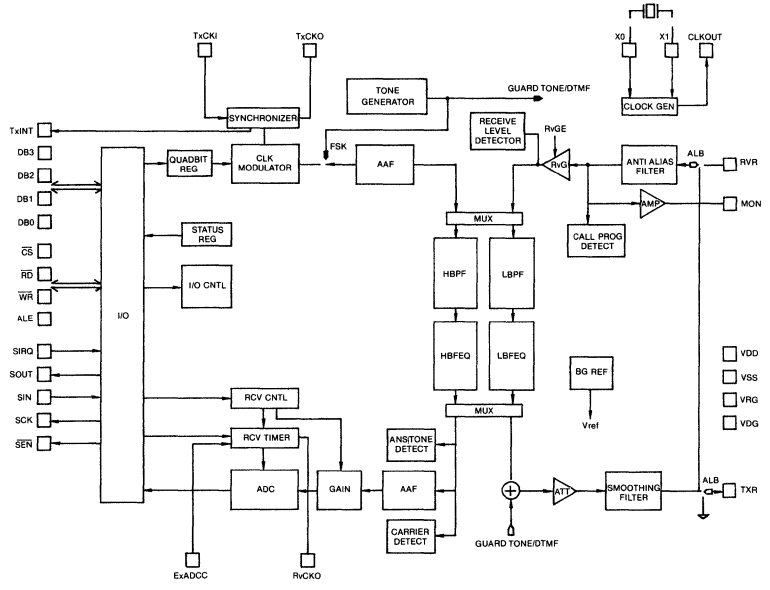
All functions on the device can be accessed easily using two control busses. A 4-bit parallel bus designed to work with standard micro-processors is used to pass transmit data, control, and status information to the K214. A serial bus which interfaces with popular DSP's (7720 typical) is used for the demodulator section.

The SSI K214 is ideal for use in self-contained or integral intelligent modem products requiring the benefits of 2400 BPS full duplex operation while maintaining compatibility with existing standards at speeds down to 300 BPS. By integrating the majority of functions needed on a single CMOS I.C., system complexity and cost is reduced without compromising performance or features.

FEATURES

- **Analog front end for DSP-based V.22 bis modems**
- **Complete modulators for QAM/DPSK (V.22 bis, V.22 Bell 212) and FSK (Bell 103)**
- **Programmable receive gain/transmit attenuation**
- **8 bit ADC with reference**
- **Band split filters with compromise equalization**
- **Analog loopback test mode**
- **Serial interface for receive processing**
- **Parallel 4-bit interface for transmitter and control**
- **Receive/transmit bit rate clocks**
- **Programmable timer for receiver data clock recovery**
- **Carrier, call progress, and answer tone detector**
- **DTMF, guard tone, and answer tone generation**
- **Crystal oscillator with echo**
- **Audio output for audible call monitoring**
- **Low power CMOS (± 5V @ 300 mW)**
- **28-pin plastic DIP or quad surface mount package**

SSI K214 Block Diagram



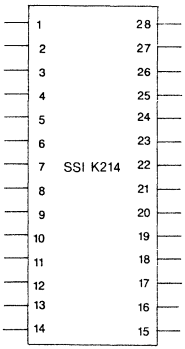


Figure 1-1

CAUTION: Use handling procedures necessary for a static sensitive component

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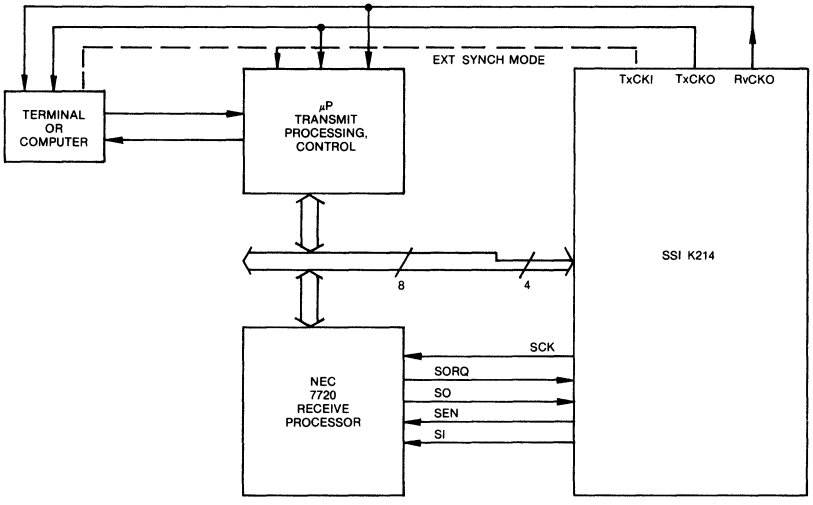
Typical 2400 BPS V.22 bis Modem Using SSI K214 Modem Analog Processor



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INNOVATORS IN INTEGRATION

SSI K222 Single Chip V.22 Modem

Preliminary Data Sheet

INTRODUCTION

The SSI K222 is a highly integrated single-chip modem I.C. which provides the functions needed to construct a V.22 compatible modem capable of 1200 BPS full-duplex operation over dial-up lines. The K222 is an enhancement of the SSI K212 single-chip modem with performance characteristics suitable for European telephone systems. The K222 also produces both 550 Hz and 1800 Hz guard tones, recognizes and generates a 2100 Hz answer tone, and allows V.21 fallback for 300 Hz FSK operation. The K222 integrates analog, digit, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28 pin DIP configuration.

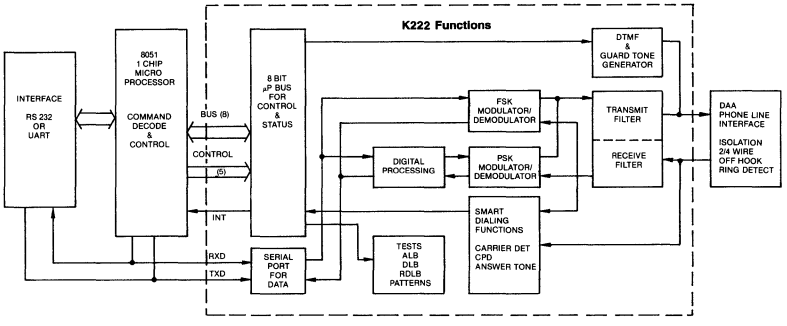
The K222 provides the PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes, and a tone generator capable of producing DTMF, answer, and simulataneous 550 and 1800 Hz guard tones required for European applications. This device supports all V.22 and V.21 modes of operation, allowing both synchronous and asychronous communication. The K222 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit mulitplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only. The K222 is pin and software compatible with the SSI K212 and K224 one-chip modem I.C.'s allowing systems to be configured for either U.S. or European operation with only a single component change.

The K222 is ideal for use in either free standing or integral system modem products where full-duplex 1200 BPS data communications over the 2-wire switched telephone network is desired. It's high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level convertors for a typical system. Coherent demodulation techniques and efficient switched-capacitor filters provide optimum performance over all line conditions when operating in the PSK mode.

FEATURES

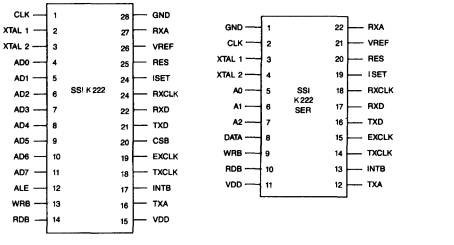
- **One-chip V.22 standard compatible modem**
- **Full duplex operation at 0-300, 600, and 1200 BPS**
- **FSK (300 BPS), or PSK (1200 BPS) encoding**
- **Pin and software compatible with SSI K212 and K224 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22 Pin DIP) or parallel microprocessor bus (28 pin DIP) for control**
- **Serial port for data transfer**
- **Maskable interrupts**
- **Selectable asynch/synch and scrambler/descrambler functions**
- **Both synchronous and asynchronous operating modes**
- **Notch filters for elimination of 550 Hz and 1800 Hz guard tones**
- **Call progress, carrier, answer tone, and long loop monitors**
- **DTMF and guard tone generators**
- **Test modes available — ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Space efficient 22 and 28 pin DIP packages**
- **CMOS technology for low power consumption (120 mW) with power down mode (30 mW)**
- **Single +5 volt supply**
- **TTL and CMOS compatible inputs and outputs**

SSI K222 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

Preliminary Pin Configuration



Pin Out (Top View)

HARDWARE INTERFACE **Pin No.**

	I/O	Signal Label	28 Pin	22 Pin	Description
POWER					
	I	GND	28	1	System ground
	I	Vdd	15	11	Power supply input, + 5 volt +10%, −10%
	O	Vref	26	21	An internally generated reference voltage for test use. Bypass with 0.1μF cap. to ground.
	I	ISET	24	19	Chip current reference Sets bias current for op-amps Programmed by connecting to Vcc through 2 MΩ resistor. Power dissipation/ performance tradeoff results from varying this value. Connecting I SET to ground selects the power down mode.
MICROPROCESSOR INTERFACE					
	I	ALE	12	–	Address latch enable. The falling edge of ALE latches the address on AD0-AD2.
	I/O	AD0-AD7	4-11	–	Address/data bus. This is a bidirectional, tri-state, multiplexed address and data bus.
	I	$\overline{CS}$	20	–	Chip select. Allows access to device data and address bus. AD0-AD7 will be in a high impedance state unless $\overline{CS}$ is low. $\overline{CS}$ is latched on the falling edge of ALE.
	O	CLK	1	2	Clock output This pin outputs either the crystal frequency (for use as a processor clock) or a 16x1200 Hz signal for use as a baud clock.
	O	$\overline{INT}$	17	13	Interrupt flag to processor. When low, indicates that a detect condition has occurred. Reset when the detect register is read or a reset is performed
	I	$\overline{RD}$	14	–	Read control. When low puts addressed register into a read condition. $\overline{CS}$ must also be low.
	I	Reset	25	20	Resets device when in high state, setting all register bits to zero and CLK to Xtal frequency. An internal pulldown resistor allows power on reset by connecting a 1μF capacitor between reset and Vcc.
	I	$\overline{WR}$	13	–	Write control. A low indicates that data is available. Data is latched on the rising edge of $\overline{WR}$. $\overline{CS}$ must be active
RS-232 INTERFACE					
	I	ExCLK	19	15	External clock input. Used in synchronous modes when external timing is selected. ExCLK becomes the phase-lock reference for TxCLK.
	O	RxCLK	23	18	Receive clock output. Carrier derived synch clock. Falling edge coincides with received data output transitions. Rising edge can be used to latch valid output data Active when carrier present
	O	RxD	22	17	Received digital data output. In synchronous or asynchronous mode, data is valid on rising edge of RxCLK.
	O	TxCLK	18	14	Transmit clock output. Used in synchronous mode to latch input data on the TxD pin. Data must be valid on the rising edge of TxCLK. TxCLK is an internally generated 1200 Hz reference in internal mode, phase locked to ExCLK in external mode, and derived from RxCLK in slave mode. TxCLK is always active.
	I	TxD	21	16	Transmit digital data input. In synch modes the data must be valid on the rising edge of TxCLK. In Asynch modes no clocking is necessary. High speed data must be 1200 +2.3%, −2.5%.

HARDWARE INTERFACE **Pin No.**

	I/O	Signal Label	28 Pin	22 Pin	Description
ANALOG INTERFACE					
	I	RxA	27	22	Received modulated analog signal input.
	O	TxA	16	12	Transmit analog output.
	I	Xtal 2	2	3	Connection for external 11.0592 MHz crystal or CMOS level clock signal.
	I	Xtal 1	3	4	Connection for external 11.0592 MHz crystal or CMOS level clock signal.
SERIAL INTERFACE					
	I	A0-A1	–	5 - 6	Register address selection. These lines should be valid during any read or write operation
	I/O	Data	–	8	Serial control data. Data for a read/write operation is clocked in or out on the falling edge of the ExCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
	I	$\overline{RD}$	–	10	Read data control. A low enables a read operation from the addressed register. Data is clocked out on transitions of the ExCLK (LSB first) while the $\overline{RD}$ line is low. Eight cycles of ExCLK are needed to transfer the full 8 bits of data contained in one register.
	I	$\overline{WR}$	–	9	Write data control. A low to high transition on this line causes 8 bits of data previously shifted in (LSB first) to be transferred to the addressed register.

Operating Limits — Absolute Maximums — SSI K222

Parameter	Max	Unit
VDD supply voltage	14	V
Storage temperature	– 65 to 150	°C
Lead temperature (10 sec.)	260	°C
TTL compatible inputs	0 to V_{DD}	V
TTL compatible outputs	– 0.3 to V_{DD}	V
TTL compatible outputs	± 3	mA

Notes: 1. All inputs and outputs are protected from static charge using built-in industry standard protection devices
2 All outputs are short-circuit protected

BUS INTERFACE

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines (latched by ALE in parallel mode) Control and status bits are identified below:

A0	A1	Register	Function
0	0	CR0	Control register 1
0	1	CR1	Control register 2
1	0	DR	Detect register (read only)
1	1	DTMF	DTMF transmit tones

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
00	SSI TEST	**HALF SPEED**	LOW SPEED	TX MODE BIT 2	TX MODE BIT 1	TX MODE BIT 0	TX ENABLE	ORG/ ANS
01	TX TEST BIT 1	TX TEST BIT 0	EN INT DETECT	BYPASS SCR	CLK SELECT	RESET	TEST MODE BIT 1	TEST MODE BIT 0
10	0	0	0	RDL	CD	ANS TONE	CALL PROG	LONG LOOP
11	0	0	TX ANS TONE	TX DTMF	DTMF BIT 3	DTMF BIT 2	DTMF BIT 1	DTMF BIT 0

CONTROL REGISTER 0 – CR0

D7	D6	D5	D4	D3	D2	D1	D0
SSI TEST	0	LOW SPEED	TX MODE BIT 2	TX MODE BIT 1	TX MODE BIT 0	TX ENABLE	ORG/ANS

0 = NORMAL
1 = INVALID

0=1200
1=600

1 = 300 BPS
0 = 1200 BPS

000 = PWR DOWN
001 = INT SYNCH
010 = EXT SYNCH
100 = SLAVE SYNCH
000 = ASYCH 8 BITS/CHAR
101 = ASYCH 9 BITS/CHAR
110 = ASYCH 10 BITS/CHAR
111 = ASYCH 11 BITS/CHAR

1 = TX
0 = TX OFF

1 = ORG
0 = ANS

CONTROL REGISTER – CR1

D7	D6	D5	D4	D3	D2	D1	D0
TX TEST BIT 1	TX TEST BIT 0	INT EN	SCR EN	CLK CONTROL	RESET	TEST MODE BIT 1	TEST MODE BIT 0

00 = TX DATA
01 = TX ALTERNATE
10 = TX MARK
11 = TX SPACE

ENABLE INTERRUPT
1 = ON
0 = OFF

0 = ON
1 = OFF

0 = XTAL
1 = 16X1200

RESET

00 = NORMAL
01 = ANALOG LOOPBACK
10 = REMOTE DIGITAL LOOPBACK
11 = LOCAL DIGITAL LOOPBACK

DETECT REGISTER – DR

D7	D6	D5	D4	D3	D2	D1	D0
RCV DATA	0	0	RDL	CD	ANS TONE	CALL PROG	LONG LOOP

TONE REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
RXD OPEN	**TX GUARD**	TX ANS TONE	TX DTMF	DTMF 3	DTMF 2	DTMF 1	**DTMF O/ GUARD**

1 = ON
0 = OFF

1 = TX DTMF
0 = DATA

– 4-BIT CODE FOR 1 OF 16 DUAL-TONE COMBINATIONS –

Operating Conditions — SSI K222

Parameter	Test Conditions	Min	Nom	Max	Units
Power supply					
VDD supply voltage		9.6	12	13.2	V
VDD supply current	2 MΩ resistor ISET — V_{DD}	—	—	15	mA
VDD supply current	Power down mode	—	—	5	mA
External Components					
VREF bypass capacitor	External to ground	0.1	—	—	μF
Bias setting resistor	Between V_{DD} and ISET	—	2	—	MΩ
VDD bypass capacitor	External to ground	0.1	—	—	μF
Input Clock variation	11.0592MHz input xtal	−0.01	—	+0.01	%
Environmental					
Ambient temperature	—	0	—	70	°C
Input/Output					
Input high voltage	Vih	2	—	—	V
Input low voltage	Vil	—	—	0.8	V
Input high current	Input voltage = 7 V	—	—	100	μA
Input low current	Input voltage = 0 V	−200	—	—	μA
Input capacitance		—	—	10	pF
Output high voltage	Iout = −0.4 mA	2.4	—	5	V
Output low voltage	Iout = 1.6 mA	—	—	0.4	V
Crystal Oscillator					
Load capacitance	XTAL 1, Xtal 2	10	—	30	pF
XTAL 1 input high	Vih	4.0	—	—	V
XTAL 1 input low	Vil	—	—	0.8	V
CLK output high level	Iout = −0.1 mA	2.4	—	5	V
CLK output low level	Iout = 1.6 mA	—	—	0.4	V
Bus Interface					
Address before latch	tAL	30	—	—	ns
Address hold after latch	tLA	20	—	—	ns
Latch to RDB/WDB control	tLC	40	—	—	ns
Data out from RDB	tRD	140	—	—	ns
ALE width	tLL	60	—	—	ns
Data float after read	tRDF	0	—	80	ns
Read width	tRW	200	—	5000	ns
Write width	tWW	140	—	5000	ns
Data setup before write	tDW	150	—	—	ns
Data hold after write	tWD	20	—	—	ns
PSK Modulator					
Carrier suppression	measured at TXA	55	—	—	dB
Transmitter gain variation	measured at TXA	−0.5	—	0.5	dB

Operating Conditions —

Parameter	Test Conditions	Min	Nom	Max	Units
FSK Mod/Demod					
Output frequency error	1070 Hz Txd = 0	−0.31	—	0.31	%
	1270 Hz Txd = 1	−0.32	—	0.32	%
	2025 Hz Txd = 0	−0.19	—	0.19	%
	2225 Hz Txd = 1	−0.43	—	0.43	%
Output amplitude	—	−10.5	−10.0	−9.5	dBm0
Output distortion	—	—	—	−20	dB
Output bias distortion	Alternate m/s input	−5	—	+5	%
Output jitter	Random input — varying duty cycle	−5	—	+5	%
DTMF Generator					
Output accuracy	697 Hz	−0.14	—	0.14	%
	770 Hz	−0.26	—	0.26	%
	852 Hz	−0.27	—	0.27	%
	941 Hz	−0.35	—	0.35	%
	1209 Hz	−0.30	—	0.30	%
	1336 Hz	−0.26	—	0.26	%
	1477 Hz	−0.00	—	0.00	%
	1633 Hz	−0.64	—	0.64	%
Output amplitude	Low band	−9.5	—	−8.5	dBm0
	High band	−7.5	—	−6.5	dBm0
Output distortion	—	—	—	−20	dB
Long loop detector					
Detect long loop	—	−37	—	−32.5	dBm0
Call Progress Detector					
Detect level	350 to 620 Hz band	−34	—	0	dBm0
Reject level		—	—	−40	dBm0
Delay time		—	—	20	ms
Hold time		—	—	10	ms
Hysterisis		2	—	—	dB
Carrier Detect					
Upper threshold	At RXA with 1200/2400 Hz input	—	—	−43	dBm0
Lower threshold	At RXA with 1200/2400 Hz input	−48	—	—	dBm0
Hysterisis	At RXA with 1200/2400 Hz input	2	—	—	dB
Delay time	1200/2400 Hz input	10	20	30	ms
Hold time	1200/2400 Hz input	5	10	15	ms
Answer Tone Detector					
Detect on	—	−43	—	—	dBm0
Detect off	—	—	—	−48	dBm0

Note dBm0 refers to an output level of 0 dBm at the line side of the DAA specified in the following section The DAA introduces a +9 0 dB receive gain and a −10 0 dB loss on the transmit side The K212 transmits nominally at 0 0 dBm (775Vrms) at its TXA pin with −10 0 dBm0 output from the DAA to the phone line It receives a nominal +9 0 dBm signal (2 18Vrms) at its RXA pin with a 0 dBm0 signal input from the phone line

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Telecommunications Circuits

Device	Circuit Function	Features	Power Supplies	Package
Tone Signaling Products				
SSI 201	Integrated DTMF Receiver	Binary or 2-of-8 output	12V	22 DIP
SSI 202	Integrated DTMF Receiver	Low-power, binary output	5V	18 DIP
SSI 203	Integrated DTMF Receiver	Binary output, Early Detect	5V	18 DIP
SSI 204	Integrated DTMF Receiver	Low-power, binary output	5V	14 DIP
SSI 207	Integrated MF Receiver	Detects central office tone signals	10V	20 DIP
SSI 957	Integrated DTMF Receiver	Early Detect, Dial Tone reject	5V	22 DIP
SSI 20C89	Integrated DTMF Transceiver	Generator and Receiver, μP interface	5V	22 DIP
SSI 20C90	Integrated DTMF Transceiver	Generator and Receiver, μP interface, Call Progress Detect	5V	22 DIP
SSI 980	Call Progress Detector	Detects supervision tones, Teltone second-source	5V	8 DIP
SSI 981	Precise Call Progress Detector	Detects supervision tones, Teltone second-source	5V	22 DIP
SSI 982	Precise Call Progress Detector	Detects supervision tones, Teltone second-source	5V	22 DIP
Modem Products				
SSI K212	1200/300 bps Modem	DPSK/FSK, single chip, autodial, Bell 212A	10V	28 DIP
SSI K214	2400 bps Analog Front End	Analog Processor for DSP V.22 bis Modems	10V	28 DIP
SSI K222	1200, 600, 300 bps Modem	DPSK, FSK, single chip, autodial, V.22	5V	28 DIP
SSI 223	1200 bps Modem	FSK, HDX/FDX	10V	16 DIP
SSI K224	2400 bps Modem	QAM, DPSK, FSK single chip V.22 bis	10V	28 DIP
SSI 291/213	1200 bps Modem	DPSK, two chips, low-power	10V	40/16 DIP
SSI 3522	1200 bps Modem Filter	Bell 212 compatible, AMI second-source	10V	16 DIP
Speech Synthesis Products				
SSI 263A	Speech Synthesizer	Phoneme-based, low data rate, VOTRAX second-source	5V	24 DIP
Switching Products				
SSI 80C50	T1 Transmitter	Bell D2, D3, D4, serial format and mux, low power	5V	28 DIP,Q
SSI 80C60	T1 Receiver	Bell D2, D3, serial synchron. and demux, low power	5V	28 DIP,Q
SSI 22100	Cross-point Switch	4x4x1, control memory, RCA second-source	12V	16 DIP
SSI 22101/2	Cross-point Switch	4x4x2, control memory, RCA second-source	12V	24 DIP
SSI 22106	Cross-point Switch	8x8x1, control memory, RCA second-source	5V	28 DIP
SSI 22301	PCM Line Repeater	T1 carrier signal recondition	5V	18 DIP

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SSI 223
1200 Baud FSK Modem

Preliminary Data Sheet

DESCRIPTION

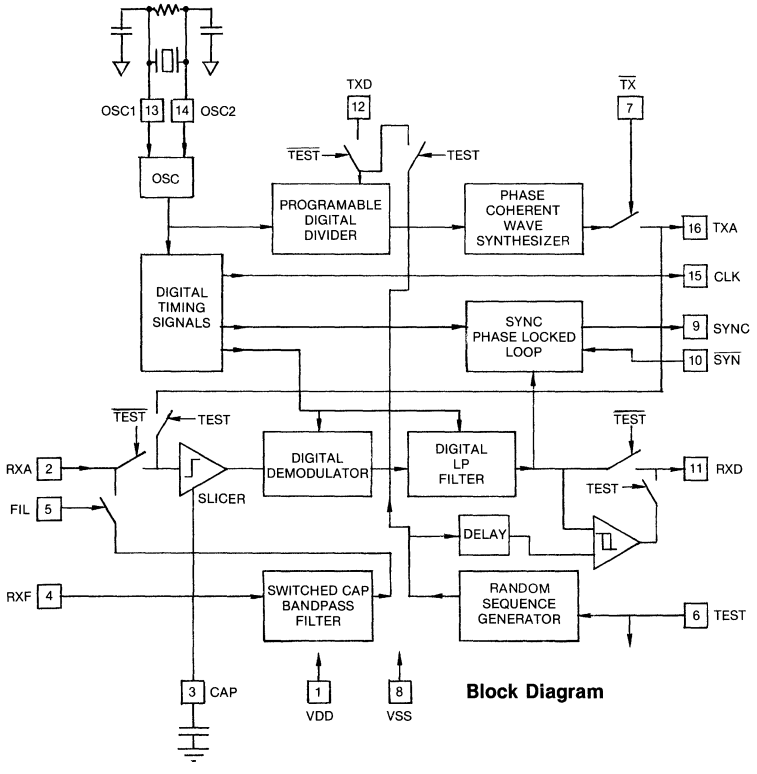
The SSI 223 modem device receives and transmits, serial, binary data over existing telephone networks using Frequency Shift Keying (FSK). It provides the filtering, modulation, and demodulation to implement a serial, asynchronous data communication channel. The SSI 223 employs the CCITT V.23 signaling frequencies of 1302 and 2097 Hz, operating at 1200 baud, and is intended for half duplex operation over a single line system or full duplex operation over a two line system.

The SSI 223 provides a cost effective alternative to existing modem solutions. It is ideally suited for R.F. data links, credit verification systems, point-of-sale terminals, and remote process control.

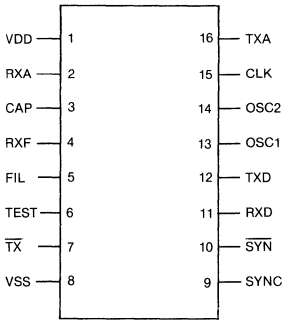
CMOS Technology ensures small size, low power consumption and enhanced reliability.

FEATURES

- **Low cost FSK Modem**
- **1200 Baud operation**
- **CMOS switched capacitor technology**
- **Simultaneous transmit and receive**
- **Built-in self-test feature**
- **On-chip filtering, Mod/Demod.**
- **Uses CCITT V.23 Frequencies**
- **On chip crystal oscillator**
- **Pin/function compatible with SSI 180**
- **Low power/High reliability**
- **16-pin plastic package**



Block Diagram



SSI 223 Pin Out (Top View)

Circuit Operation

The SSI 223 has four main functional sections: timing, transmit, receive, and test. Each section of the chip will be individually described below.

TIMING

The timing section contains the oscillator (OSC) and random logic which generates digital timing signals used throughout the chip. The time base can be derived from 3.18MHz crystal or an external digital input. The modem will operate with clock inputs from 330KHz to 3.3MHz. Back channel is supplied by selecting the lower frequency clock rate. The digital timing logic divides the oscillator frequency to give a 1200HZ output that can be used for system timing.

TRANSMITTER

The SSI 223 transmitter consists of a programmable divider that drives a programmable coherent phase frequency synthesizer. The programmable divider is digitally controlled via the Data Input pin (TXD). The output of the divider clocks a 16 segment phase coherent frequency synthesizer. A sine wave is constructed by eight weighted capacitors which are the inputs to a high pass filter. Proper matching of the capacitors is important in order to suppress the second thru fourteenth harmonics. The synthesized signal is output directly to the transmit pin TXA. The transmit signal can be disabled by using the digital control pin TX.

RECEIVER

The SSI 223's receiver is comprised of three sections: the input bandpass filter, the synchronization loop, and the demodulator.

The input bandpass filter is a four pole Butterworth filter, implemented using switched capacitor technology. This filter reduces wideband noise which significantly improves data error rates. the SSI 223 can be configured with the bandpass filter in series with the receiver by setting FIL = 1 and inserting the received signal at RXF, or the bandpass filter can be deleted from the system by setting FIL = 0 and inputting the received signal thru RXA.

The demodulator is used to detect a received mark or space.

The synchronization for sampling the digital output at RXD derived from a digital phase locked loop. The phase locked loop is clocked at 16 times the bit rate with a maximum lock period of 8 clocks and locks on the data output signal.

SELF TEST MODE

The SSI 223 features an autotest mode which provides easy field test capability of the chip's funtionality. The modem is placed in the test mode by taking the test pin high. In the test mode the Data Input pin is disconnected and the programmable divider is driven by a pseudo random PN sequence generator and the transmitter's output is connected to the receiver's input. The input data to the programmable divider is delayed by the system delay time and compared to the digital output on sync transitions. If the detected data matches the delayed input data from the PN sequence counter, the SSI 223 is properly functioning as indicated by RXD low. A high on the RXD pin indicates a functional problem on the SSI 223.

ABSOLUTE MAX RATINGS

Power Supply Voltage (V_{DD}-V_{SS}) . . . . . 14 V
Analog Input Voltage at RXA . . . . . −0.3 to V_{DD} V
Analog Input Voltage at RXF . . . . . −3 to V_{DD} V
Digital Input Voltage . . . . . V_{SS} − 0.3 to V_{DD} + 0.3 V
Storage Temperature Range . . . . . −65 to + 150 °C
Operating Temperature Range . . . . . −25 to + 70 °C
Lead Temperature (10 sec soldering) . . . . . 260 °C

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	V_{DD}	Positive Supply Voltage
2	RXA	Receive Analog Input — Analog input from the telephone network.
3	CAP	Capacitor — Connect a 0.1μf capacitor between Pin 3 and ground (VSS).
4	RXF	Filtered Receive Analog Input
5	FIL	Analog Input Control — A logical 1 selects the filtered input. A logical 0 selects the non-filtered input.
6	TEST	Self-Test Mode Control — Normal operation when a logical 0. A logical 1 places the device into the self-test mode. A Low appears at RXD, to indicate a property functioning device.
7	TX	Transmitter Control — A logical 0 selects transmit mode. A logical 1 selects a stand-by condition forcing TXA to $\frac{V_{DD}}{2}$ V_{DC}.
8	VSS	Ground
9	SYNC	Synchronized Output — Digital output synchronized with the received signal and used to sample the received eye pattern.

PIN DESCRIPTIONS

Pin No.	Symbol	Description
10	$\overline{SYN}$	Sync Disable — A logical 0 input disables the phase locked signal from the received data and locks it to the 1200Hz reference.
11	RXD	Receiver Digital Output
12	TXD	Transmitter Digital Input
13	OSC_1	Crystal Input (3.1872 MHz) or External Clock Input
14	OSC_2	Crystal Return
15	CLK	1200Hz Squarewave Output — Can drive up to 10 CMOS loads.
16	TXA	Transmitter Analog Output

ELECTRICAL CHARACTERISTICS Unless otherwise specified, $4.5 < V_{DD} < 13\ V_{DC}$, $V_{SS} = 0\ V_{DC}$, $-25°C < TA < 70°C$.

POWER SUPPLY

Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDD Voltage Supply Range		4.5	—	13	V
Supply Current	V_{DD} = 5V 25°C	—	2.0	—	mA
	V_{DD} = 12V 25°C	—	5.0	—	mA
Digital Inputs					
Input Low Voltage VIL		$V_{SS} - 0.3$	—	$V_{SS} + 1.5$	V
Input High Voltage VIH		$V_{DD} - 1.5$	—	$V_{DD} + 0.3$	V
Input Low Current IIL		−1	—	—	μA
Input High Current IIH		—	—	1	μA
Digital Outputs					
Output Low Voltage VOL	IOL < 1μA	—	—	0.05	V
Output High Voltage VOH	IOL < 1μA V_{DD} = 5V	4.95	—	—	V
Output Low Current IOL	VOL = 0.4V V_{DD} = 5V	0.5	—	—	mA
Output High Current IOH	VOH = 4.5V V_{DD} = 5V	−0.2	—	—	mA
Analog Input Level @ RXA	Centered at $V_{DD}/2$ + 0.5V	0.2	—	$V_{DD}/4$	Vpp
Analog Input Level @ RXF	*DC Level between V_{DD} & V_{SS}	0.2	—	$V_{DD}/2$	V_{DC}
Error Rate	S/N = 8dB Input @ RXF	—	—	5×10^{-3}	—
Analog Output Level @ TXA	RL ≥10K $\overline{TX} = 0$	—	$V_{DD}/4$	—	Vpp
Analog Output Level @ TXA	$\overline{TX} = 1$	—	$V_{DD}/2$	—	V_{DC}
Output Frequency @ TXA	XTAL = 3.1872MHz TXD = 1	—	1302	—	Hz
	TXD = 0	—	2097	—	Hz
Output Harmonics	2nd to 14th Harmonics	—	−60	−50	dB
	15th Harmonic	—	—	−20	dB
Input Filter (RXF)	*Input = 200 mVpp to $V_{DD}/2$ Vpp				
Lower 3dB Corner		—	760	—	Hz
Upper 3dB Corner		—	2625	—	Hz

*Note The SSI 223 RXF input is AC coupled internally, but the DC value of the input must be between the two supplies VDD & VSS

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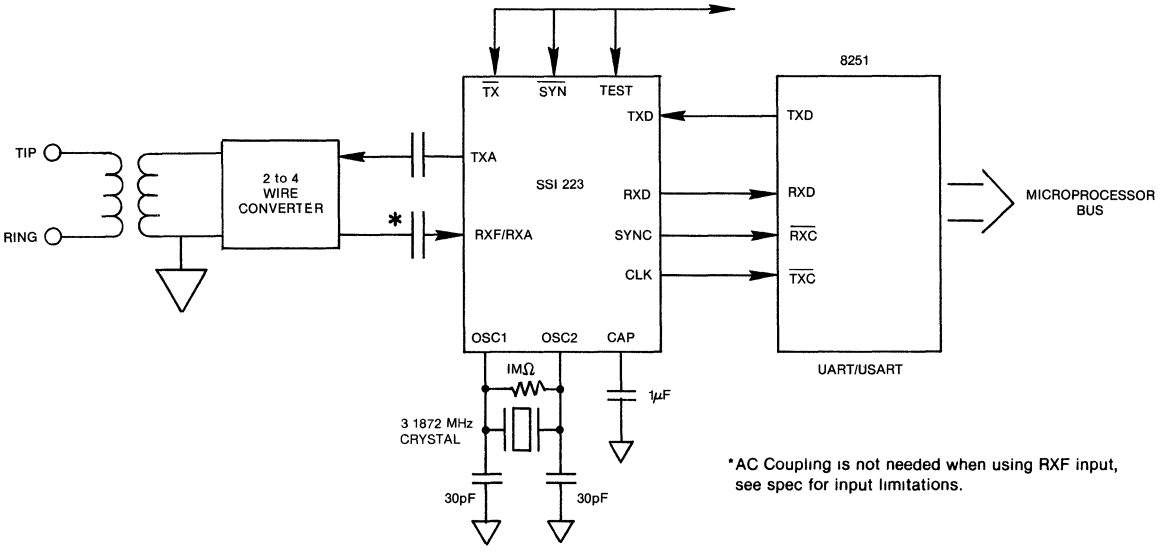
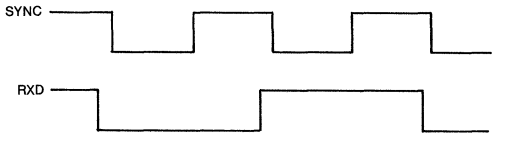
Typical Application

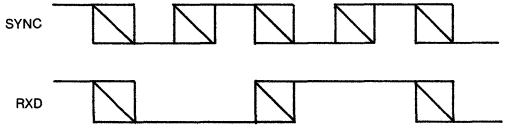


Note: A simple low speed back channel can be configured using a DTMF Encoder and Decoder (SSI202)

Received Output Waveforms



(a) High S/N Ratio Analog Input



(b) Low S/N Ratio Analog Input

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SSI K224 Single Chip V.22 bis Modem

(Availability: Fall 1986)

Preliminary Data Sheet

INTRODUCTION

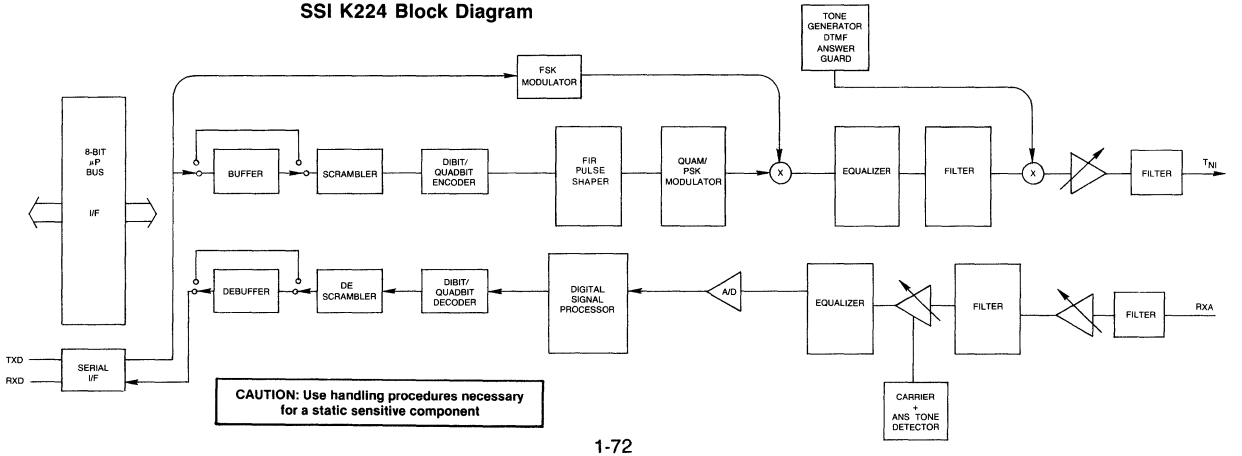
The SSI K224 is a highly integrated single-chip modem I.C. which provides the functions needed to construct a V.22 bis compatible modem, capable of 2400 BPS full-duplex operation over dial-up lines. Using an advanced CMOS process that integrates analog, digital signal processing, and switched-capacitor array functions on a single substrate, the SSI K224 offers excellent performance and a high level of functional integration in a single 28 pin DIP configuration. The K224 provides the QAM, PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes, and a tone generator capable of producing DTMF answer, and simultaneous 550 and 1800 Hz guard tones required for European applications. This device supports all V.22 bis, V.22, V.21, Bell 212A, and Bell 103 modes of operation, allowing both synchronous and asynchronous communication. The K224 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only. The K224 is pin and software compatible with the SSI K212 and K222 one-chip modem I.C.'s, allowing system upgrades with a single component change.

The K224 is ideal for use in either free standing or integral system modem products where full-duplex 2400 BPS data communications over the 2-wire switched telephone network is desired. It's high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level convertors for a typical system. Adaptive equalization assures the user of optimum performance over all line conditions when operating in the QAM and PSK modes.

FEATURES

- **One-chip multi-mode V.22 bis/Bell 212A compatible modem**
- **Full duplex operation at 0-300, 1200, and 2400 BPS**
- **FSK (300 BPS), PSK (1200 BPS), or QAM (2400 BPS) encoding**
- **Pin and software compatible with SSI K212 and K222 1-chip modems**
- **Interfaces directly with standard microprocessors (8048), 80C51 typical)**
- **Serial (22 Pin DIP) or parallel microprocessor bus (28 pin DIP) for control**
- **Serial port for data transfer**
- **Maskable interrupts**
- **Selectable asynch/synch and scrambler/descrambler functions**
- **All synchronous and asynchronous operating modes**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit gain (15dB, 1dB steps), selectable receive boost (+12dB)**
- **Call progress, carrier, answer tone, and signal quality monitors**
- **DTMF and guard tone generators**
- **Test modes available — ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Space efficient 22 and 28 pin DIP packages**
- **CMOS technology for low power consumption (120 MW) with power down mode (30 mW)**
- **Single +12 volt supply**
- **TTL and CMOS compatible inputs and outputs**

SSI K224 Block Diagram



OPERATION

General

The SSI K224 was designed to be a complete V.22 bis compatible modem on a chip. It requires only the addition of a control microprocessor, RS-232, and a phone line interface to design a complete modem. As many functions as possible were included in order to simplify implementation into typical modem designs. In addition to the basic 2400 BPS QAM, 1200 BPS PSK and 300 BPS FSK modulator/demodulator sections, the device also includes synch/asynch converters, scramber/descrambler, call progress tone detect, and DTMF tone generator capabilities. All V.22 bis and Bell 212A modes are supported (synchronous and asynchronous) and test modes are provided for diagnostics. Most functions are selectable as options and logical defaults are provided when override modes are chosen. The device can be directly interfaced to a microprocessor via its 8-bit multiplexed address/data bus for control and status monitoring. Datacommunication takes place through a separate serial port.

QAM Modulator/Demodulator

The SSI K224 encodes incoming data into quadbits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator reverses this procedure but also recovers a data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for those line characteristics.

PSK Modulator/Demodulator

The K224 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The K224 uses a phase locked loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers. Adaptive equalization is also used in PSK modes for optimum operation with slowly varying line conditions.

FSK Modulator/Demodulator

The FSK modulator frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 Hz and 1070 Hz (originate mark and space) and 2225 Hz and 2025 Hz (answer mark and space) are used when this mode is selected. V.21 frequencies are used when this mode is selected. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the FSK modes.

Passband Filters and Equalizers

A high and low band filter is included to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out of band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering corresponds to a 75% square root of raised Cosine frequency response characteristic.

Asynchronous Mode

The asynchronous mode is used for communication with asychronous terminals which may communicate at 1200 BPS +1%, −2.5% even though the modem's output is limited to 1200 BPS ±.01%. When transmitting in this mode the serial data on the TxD input is passed through a rate convertor which inserts or deletes stop bits in the serial bit stream in order to output a signal that is exactly 1200 BPS ±.01%. This signal is then routed to a data scrambler (following the CCITT V.22 algorithm) and into the analog PSK modulator where dibit encoding results in a V.22 bis or Bell 212A standard output signal. Both the rate convertor and scrambler can be bypassed for handshaking, FSK, and synchronous operation. The device recognizes a break signal and handles it in accordance with Bell 212A specifications. Received data is processed in a similar fashion except that the rate convertor now acts to reinsert any deleted stop bits and output data to the terminal at no greater than 1219 BPS. An incoming break signal will be passed through without incorrectly inserting a stop bit.

Synchronous Mode

Synchronous operation is possible only with the QAM or PSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TxD must be valid on the falling edge ot TxCLK. Receive data at the RxD pin is clocked out on the rising edge of RxCLK. The asynch/synch convertor is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

Parallel Bus Interface

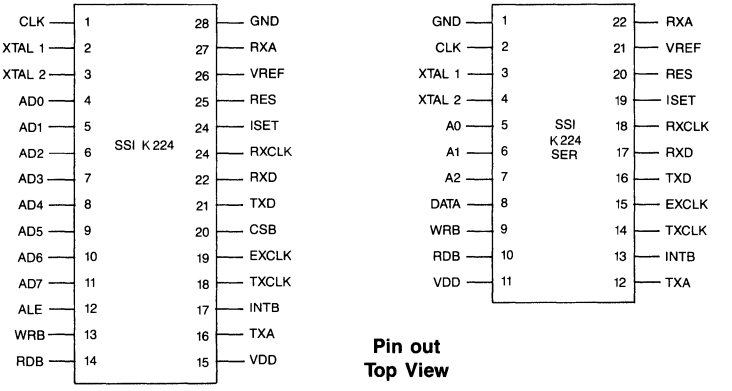
Six 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the A0, A1, and A2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as six consecutive memory locations. Five control registers are read or write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

Serial Command Interface

The serial command mode allows access to the K224 control and status registers via a serial command port (22 pin version only). In this mode the A0 and A1 lines provide register addresses for data passed through the data pin under control of the RD and WR lines. A read

operation is initiated when the RD line is taken low. The next eight cycles of ExCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of ExCLK. WR is then pulsed low and data transfer into the selected register occurs on the rising edge of WR.

Preliminary Pin Configuration



Pin out
Top View

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SSI 291/213 Modem 1200 BPS Full Duplex Modem Device Set

Preliminary Data Sheet

GENERAL DESCRIPTION

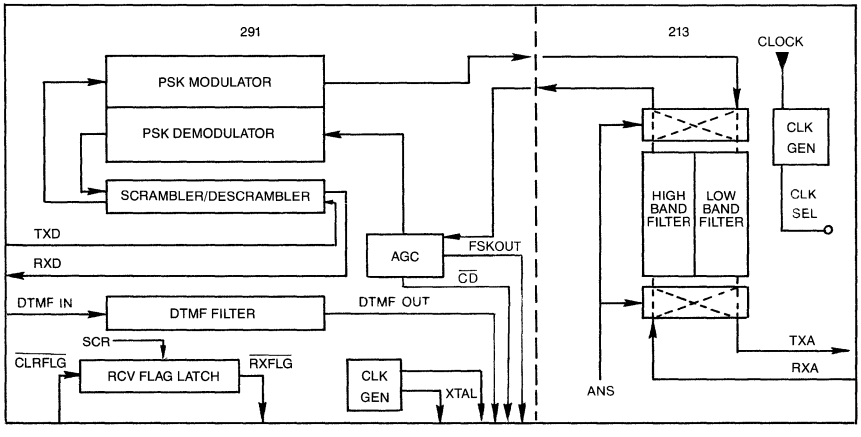
The SSI 291/213 is a CMOS I.C. device set that forms the basis for a 1200 bps Bell 212A compatible modem. The SSI 213 is a modem filter that provides the channel separation, equalization, and answer/originate steering logic needed for Bell 212A operation. The 291 contains the Bell 212 modulator and demodulator, AGC, scrambler/descrambler, and carrier detect monitor. Clock generator and undedicated low pass filter functions are also included to minimize the requirement for external components. Using TTL and CMOS compatible I/O, the device set is designed to provide a low-cost modem when integrated with a one-chip control microprocessor.

The 291/213 device set is ideal for use in either free standing, or integral system modem products, where full-duplex 1200 bps data communications over the 2-wire switched telephone network is desired. Its high functionality, reduced power consumption, and low-cost simplify design requirements and increase system reliability. A complete modem can be implemented by adding a phone line interface, a control microprocessor, and RS-232 level converters for a typical system. The use of coherent demodulation techniques assures the user of optimum performance when communicating over degraded lines.

FEATURES

- **Two-chip set compatible with 2-wire PSTN phone lines**
- **Available in 40- or 28-pin DIP (SSI 291) and 16-pin DIP (SSI 213)**
- **Full duplex operation at 1200 bps**
- **PSK encoding in Bell 212A format**
- **Will interface with standard microprocessors through serial control lines**
- **Serial port for data transfer**
- **Selectable answer/originate, clock frequencies**
- **Support functions on-chip: clock generator, low-pass filter, receive clock flag**
- **Coherent demodulation technique provides optimal performance**
- **CMOS technology for low power consumption (100 mW typical)**
- **± 5V supplies**
- **TTL and CMOS compatible inputs and outputs**

SSI 291/213 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

SSI 291/213 Modem 1200 BPS Full Duplex Modem Device Set

General

The SSI 291/213 is designed to serve as a low-cost 1200 bps full-duplex modem that offers Bell 212A 1200 bps compatibility when used with a control microprocessor. The modulator/demodulator, as well as various support functions needed to integrate the function with a microprocessor in a minimum cost system, were included in the device set. In addition to the basic 1200 bps PSK modulator/demodulator, the product also includes a carrier detect monitor, scrambler/descrambler, clock generator, and a DTMF low-pass filter for eliminating distortion from microprocessor-generated dual-tones. A zero-crossing detector simplifies the design of the 300 bps FSK demodulator function, and signal control logic is included to ease the addition of this operating mode to the device set. An included "receive signal flag" can be used as an interrupt, reducing the load on the system processor when operating in Bell 212A mode. The 1200 bps Bell 212A mode is supported (synchronous operation) and test modes are provided for chip diagnostics. The device set can be directly interfaced to a microprocessor using serial lines for data transfer, control, and status monitoring.

PSK Modulator/Demodulator

The 291/213 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (Orginiate mode) or 2400 Hz carrier (Answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream. Demodulation occurs using either a 1200 Hz (Answer mode) or a 2400 Hz carrier (Originate mode). The 291/213 uses a phase locked loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

Passband Filters and Equalizers

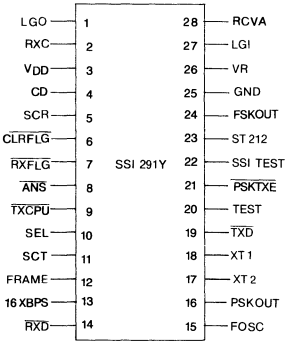
A high and low band filter is included in the SSI 213 to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out of band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal.

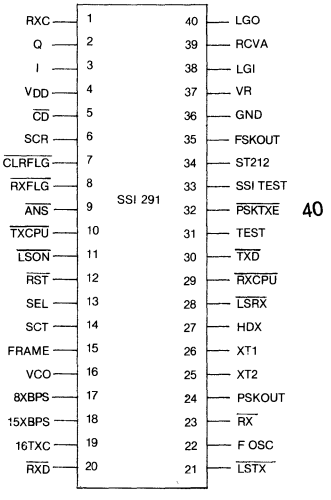
Signal Control Logic

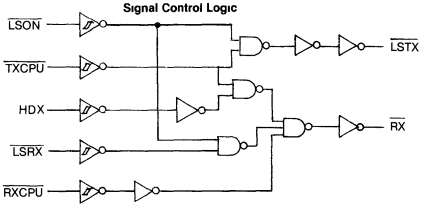
Signal control logic is provided that allows addition of the 300 bps mod/demod function to a system using the SSI 291/213 device set. This logic (see diagram) allows single pin routing of externally provided 300 bps digital signals to the $\overline{LSTX}$ and $\overline{RX}$ outputs for either full or half-duplex operation.

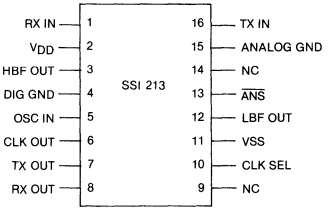
Synchronous Operation

The SSI 291/213 is designed to provide synchronous operation at the 1200 bps rate. In this mode, data is synchronized to a provided clock, and no variation in data transfer rate is allowable. Proper transmit action requires that serial input data appearing at TxD be valid on the falling edge of SCT. A receive data flag acts as a synchronization device for microprocessor interfacing. Received data at the RxD pin may be read after the RXFLG goes low, and this flag is reset after a read operation by externally setting CLRFLG.









Pin Descriptions — SSI 291

Pin Number 291Y	291	I/O	Type	Label	Description
Power					
25	36	I	—	GND	Power ground termination
3	4	I	—	VDD	+5V ±10% power input
26	37	I	—	VR	Analog voltage reference
Control Interface					
10	13	I	LSTTL	SEL	Selects output frequency for clocks as shown:
—	12	I	LSTTL	$\overline{RST}$	SEL RST 16TXC 16XBPS 8XBPS 1 1 4800Hz 4819Hz 2409Hz 1 0 4800Hz 4819Hz LOGIC 1 0 1 19200Hz 19505Hz 9752Hz 0 0 19200Hz 19505Hz LOGIC 1
8	9	I	LSTTL	$\overline{ANS}$	ANS/ORG mode. A logic "1" selects originate mode
21	32	I	LSTTL	$\overline{PSKTXE}$	PSK transmit enable — a "0" enables output "1" sets PSKOUT to "1"
15	22	O	LSTTL	FOSC	153.6KHz clock output
—	17	O	LSTTL	8XBPS	8 X 1219Hz clock output
13	18	O	LSTTL	16XBPS	16 X 1219Hz clock output
—	19	O	LSTTL	16TXC	16 X 1200Hz clock output
23	34	I	LSTTL	ST212	Self test: causes mod and demod to operate on the same frequency
7	8	O	LSTTL	$\overline{RXFLG}$	Receive data flag — reset to a low level in conjunction with latching of data at RXD on the rising edge of the SCR clock
6	7	I	LSTTL	$\overline{CLRFLG}$	Clear data flag — A low sets the RXFLG output to a high level
Analog Interface					
16	24	O	Analog	PSKOUT	PSK modulator output
1	40	O	Analog	LGO	Output for DTMF filter
28	39	I	Analog	RCVA	Receive analog (from bandsplit filter)
27	38	O	Analog	LGI	Input for two pole low pass DTMF filter
18	26	I	Analog	XT1	Connection for 2.4576MHz crystal
17	25	I	Analog	XT2	Connection for 2.4576MHz crystal
2	1	O	Analog	RXC	AGC analog output
RS-232 Signal Interface					
19	30	I	LSTTL	$\overline{TXD}$	Input for 1200 bps synchronous data
11	14	O	LSTTL	SCT	Derived synchronous transmit data clock — $\overline{TXD}$ data is latched on the rising edge of SCT
14	20	O	LSTTL	$\overline{RXD}$	Output for received 1200 bps synchronous data which is latched into the $\overline{RXD}$ output on the rising edge of SCR. $\overline{RXFLG}$ — the receive data flag is reset to a low level at the same time
5	6	O	LSTTL	SCR	Synchronous receive data clock
4	5	O	LSTTL	$\overline{CD}$	Carrier detect — a low level indicates carrier present

Pin Descriptions — SSI 291

Pin Number					
291Y	**291**	**I/O**	**Type**	**Label**	**Description**
Signal Control Logic					
—	11	I	LSTTL	$\overline{\text{LSON}}$	Low speed online enable
9	10	I	LSTTL	$\overline{\text{TXCPU}}$	Low speed transmit data input to logic
—	29	0	LSTTL	$\overline{\text{RXCPU}}$	Low speed receive data input to logic
—	27	I	LSTTL	HDX	Selects half duplex echo logic
—	28	I	LSTTL	$\overline{\text{LSRX}}$	Low speed receive data from an external FSK Demodulator
—	21	I	LSTTL	$\overline{\text{LSTX}}$	Low speed transmit data (to an external FSK modulator)
—	23	0	LSTTL	$\overline{\text{RX}}$	Low speed switched data output (to CPU)
Miscellaneous					
—	2	0	Analog	Q	PSK demodulator quadrature signal
—	3	0	Analog	I	PSK demodulator in-phase signal
12	15	0	LSTTL	FRAME	Derived synchronous baud clock — 600 Hz signal is low for the first half of the baud interval and high for the last half
24	35	0	LSTTL	FSKOUT	Receive analog zero crossing detector output
—	16	0	LSTTL	VCO	VCO output from demodulator circuit
20	31	I	LSTTL	TEST	A logic "1" forces the SCT output high
22	33	I	LSTTL	SSITEST	High level selects internal test mode

Operating Limits — SSI 291

Pin Number								
291Y	**291**	**Label**	**Parameter**	**Conditions**	**Min**	**Nom**	**Max**	**Units**
3	4	VDD	Supply voltage	—	4.5	5	5.5	V
			Supply current	—	—	—	—	mA
			Temperature range	—	0	—	70	°C
	All LSTTL	—	VIH	IIH $<10\mu$A	2.2	—	—	V
	inputs		VIL	IIL $<10\mu$A	—	—	0.7	V
	All LSTTL/	—	VOL	IOL = 1.6 mA	—	—	0.4	V
	CMOS			IOL = 10 μA	—	—	0.2	V
	OUTPUTS			IOH = 40 μA	2.6	—	—	V
				IOH = 10 μA	—	—	V_{DD}-0.2	V
			Rise time	CL $<$100 pF	—	—	300	ns
			Fall time	CL $<$100 pF	—	—	300	ns
1	40	RCVA	Zin	0 $<$VIN $<V_{DD}$	20	—	—	KΩ
26	37	VR	Zin	10μF bypass cap	1.25	—	5	KΩ
			Voltage	IL $<10\mu$A	0.45V_{DD}	—	0.55V_{DD}	V
28	39	LGI	Zin	—	20	—	—	KΩ
27	38	LGO	Zout	AC coupling	10	—	—	KΩ
			Capacitance	—	—	—	100	pF
2	3,2,1	I,Q,RXC	Zout	AC coupling	100	—	—	KΩ
			Capacitance	—	—	—	20	pF
7	26,25	XT1, XT2	duty cycle	—	40	—	60	%

Operating Limits — SSI 291

Pin Number 291Y	291	Label	Parameter	Conditions	Min	Nom	Max	Units
2	1	RXC	AGC level	RCVA = 2.2 – 45Mvp	–2	–1	0.6	dbV
			AGC threshold	RXC = 2 – 0.6dbV	34	45	60	mVp
			AGC attack	—	—	13	—	ms
			AGC release	—	—	107	—	ms
4	5	$\overline{CD}$	Low input level	—	34	45	60	mVp
			High input level	—	42	—	75	mVp
			Hysterisis	—	1.5	2	2.5	db
24	35	FSKOUT	Duty cycle	RCVA = 45 mVp	45	50	60	%

Pin Descriptions — SSI 213

Pin No.	I/O	Type	Label	Description
15	I	—	Analog Gnd	Analog ground pin—separate from digital ground
6	0	CMOS	CLK out	104.5 KHz SCF clock output. CMOS compatible
4	I	—	Digital Gnd	Digital ground pin—separate from analog ground
3	0	Analog	HBF out	High band filter output before equalization. Limited to 100KΩ drive capability.
12	0	Analog	LFB out	Low band filter output before equalizer. Limited to 100KΩ drive capability.
13	1	CMOS	$\overline{ANS}$	Channel steering control. Logic 0 selects the answer mode, with high-band transmit and low-band receive signal routing. A logic 1 selects the originate mode with the opposite channel orientation.
5	I	CMOS	Osc in	Accepts a CMOS level frequency reference at 2.304 or 3.5795 MHz as selected to generate the SCF 52.36 KHz clock used internally
16	I	Analog	Tx in	Transmit signal filter input
7	0	Analog	Tx out	Transmit signal output from equalizer
1	I	Analog	Rx in	Receive signal filter input
8	0	Analog	Rx out	Receive signal output from equalizer
2	I	—	V_{DD}	+5V –5%, +25% power input
11	I	—	VSS	–5V +5%, –25% power input
10	I	CMOS	Clk Sel	Clock select pin. Connecting pins 10 and 11 changes the internal divider ratio allowing use of a standard 3.5795 Mhz color burst crystal reference to generate the 52.36 KHz SCF clock. The 2.304 MHz clock input is selected when pin 10 is left open (has internal pull-up).

Operating Limits — SSI 213

Digital signals: pin 5, 6, 13

High level input voltage...VIH . . . . . 3.75V min
High level input voltage...IIH . . . . . 10μA max
Low level input voltage...VIL . . . . . 0.8V max
Low level input voltage...IIL . . . . . – 10μA max

Clock input: pin 5

Input clock frequency . . . . . 2.304 or 3.5795 MHz ± 0.01%
Input clock duty cycle . . . . . 20% min, 80% max

Analog signals: pins 1, 2, 3, 4, 7, 8, 11, 12, 15, 16

Supply voltage, V_{DD} . . . . . 4.75V min 6.25V max
Supply voltage, VSS . . . . . – 4.75V min – 6.25V max
Supply current, IDD...(V_{DD} = 5.0V) . . . . . 10mA max
Supply current, ISS...(VSS = – 5.0V) . . . . . – 10mA max
Input impedance, ZIn . . . . . 10 KΩ min
Output impedance, Zout (pins 3, 12) . . . . . 100KΩ typ
Output impedance, Zout (pins 7,8) . . . . . 1KΩ max
Output noise, C-message . . . . . 950μV RMS max
Channel separation . . . . . 50 dB min
Input signal level . . . . . V_{DD} – 2.0V P-P max
Supply imbalance, V_{DD} + VSS . . . . . 0.5V max
Operating temperature range . . . . . 0 to 70 °C
Storage temperature range . . . . . – 65 to 150 °C

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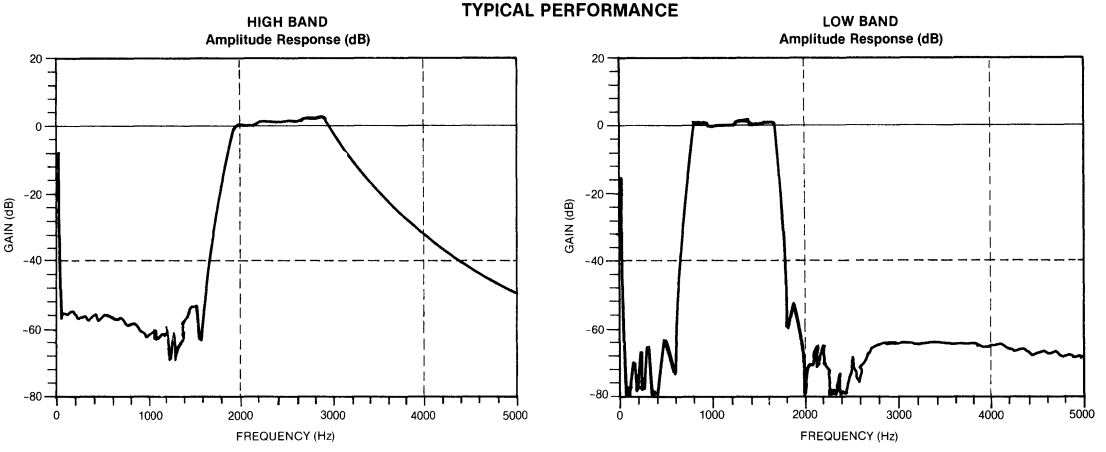
Design Considerations

The SSI 213 uses SCF sampled data techniques. To avoid signal aliasing problems the input signal should not contain significant energy within 3 KHz of any multiple of the 52.36 KHz sampling clock. An anti-aliasing filter may be needed to meet this requirement.

When the alternate clock input is selected, a rate multiplier is inserted in the normal clock divider circuit. This shifts the SCF clock frequency to 52.30 KHz and the CLK out pin output to 104.6 KHz. In addition, a low level modulation tone at approximately 23 KHz will be generated with a typical amplitude of less than 600 μV RMS. Normal applications will not be affected by these changes.

TYPICAL PERFORMANCE



Application

The SSI 291/213 chip set is typically used in conjunction with a microprocessor and supporting external components to form a cost-effective intelligent modem system. This type of modem communicates asynchronously by interpreting ASCII commands passed through the serial data stream, and controls the modem functions accordingly by using serial port lines to switch various control lines on the 291/213. A basic version of this design would include 1200 bps communications capability, answer/originate logic to answer incoming calls, and an auto dial function using pulse dialing. The 291/213 provides the mod/demod function, while the microprocessor performs the command interpretation, control, and the handshaking needed to originate and answer calls. The microprocessor must also perform the asynch to synch conversion needed to generate a synchronous data stream using the variable data rate coming from a terminal or processor bus.

A more elaborate system uses the additional features of the 291 I.C. to form a complete low-cost system, providing 1200 bps PSK and 300 bps FSK communication, smart calling functions with DTMF or pulse dialing, and call progress detection. In this system, the microprocessor performs the 300 bps mod/demod function using the partial demod block (zero crossing detector) on the 291 and an external D/A for waveform generation and DTMF tones.

A third version provides higher quality DTMF generation, call progress detection, and 300 bps operation by using external components. While not as economical as the basic 291/213 only design, the advantage of this approach is a reduction in the software requirement for the processor, making code available for providing more sophisticated features or multiple command sets.

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SSI 3522
Bell 212A/V.22
Modem Filter

Data Sheet

GENERAL DESCRIPTION

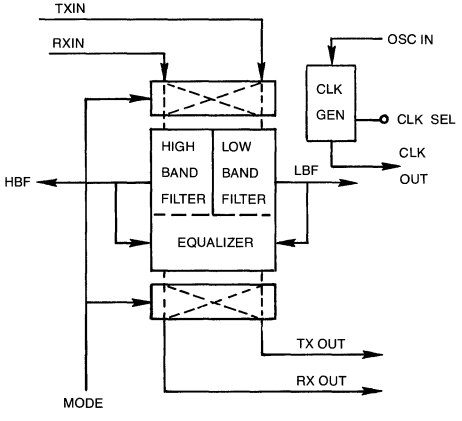
The SSI 3522 is a 16 pin CMOS integrated circuit that provides the channel filtering and equalization functions required for Bell 212A and C.C.I.T.T. V.22 modem applications. Employing switched capacitor filter techniques, the 3522 includes channel separation filters optimized for 1200 and 2400 Hz operation, while maintaining the bandshape necessary to reject 550 and 1800 Hz guard tones typical for V.22 standard modems. Fixed compromise equalization and group delay correction is distributed between the two channels as prescribed by V.22 recommendations. Dual multiplexers provide channel steering action for answer/orginate control using a single pin.

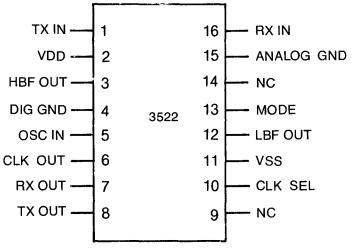
The 3522 is designed to provide the front end for a Bell 212A or V.22 modulator/demodulator I C such as the SSI 291. Optimized for PSTN lines, the 3522 offers an economical solution to the filter requirements of medium speed modem designs.

FEATURES

- **Performs Bell 212A/V.22 channel filter functions**
- **High performance/low cost filter for medium speed modems**
- **Compromise equalization**
- **Single pin originate/answer steering logic**
- **Selectable clock divider—2.304 MHz or 3.5795 MHz color burst frequency**
- **+− 5V operation at 50 mW typical power consumption**
- **CMOS technology and I/O compatibility**
- **16 pin DIP configuration**
- **CMOS latch-up protected**

SSI 3522 Block Diagram





CAUTION: Use handling procedures necessary for a static sensitive component

SSI 3522
Bell 212A/V.22
Modem Filter

CIRCUIT OPERATION

GENERAL:

The SSI 3522 is designed to act as a low cost filter for use in conjunction with Bell 212A or V.22 modem I C 's such as the SSI 291. The device consists of a high and low band filters, split compromise equalizers for the two channels, and dual multiplexer logic for originate/answer channel steering. The unbuffered filter outputs are brought out to pins LBF and HBF before the signals have been processed by the equalizer section, and may be used for test purposes or in applications where the equalizer must be bypassed. Output impedance of these pins is 100 kΩ, requiring buffering if significant loads are to be driven. A clock generator provides the switched capacitor clock sampling frequency of 52.36 kHz from a 2.304 MHz buffered input signal. Tying pins 10 and 11 together changes the internal scaling rate to allow use of a 3.5795 MHz input, which can be generated from a standard color burst crystal. Filter response is essentially flat for a passband centered around the 1200 and 2400 Hz center frequencies, while notch filters located at 550 and 1800 Hz insure excellent rejection of C.C.I.T.T. guard tones.

DESIGN CONSIDERATIONS

The SSI 3522 uses SCF sampled data techniques. To avoid signal aliasing problems the input signal should not contain significant energy within 3 kHz of any multiple of the 52.36 kHz sampling clock. An anti-aliasing filter may be needed to meet this requirement.

When the alternate clock input is selected, a rate multiplier is inserted in the normal clock divider circuit. This shifts the SCF clock frequency to 52.30 kHz and the CLK out pin output to 104.6 kHz. In addition, a low level modulation tone at approximately 23 kHz will be generated with a typical amplitude of less than 600 μV RMS. Normal applications will not be affected by these changes.

TABLE 1: PIN DESCRIPTIONS

PIN NO.	I/O	NAME	NAME—DESCRIPTION
15	I	Analog Gnd	Analog ground pin—separate from digital ground
6	O	CLK out	104.5 Khz SCF clock output, CMOS compatible
4	I	Digital Gnd	Digital ground pin—separate from analog ground
3	O	HBF out	High band filter output before equalization. Limited to 100 Kohm drive capability
12	O	LBF out	Low band filter output before equalizer. Limited to 100Kohm drive capability.
13	I	Mode	Channel steering control. Logic 1 selects the answer mode, with high-band transmit and low-band receive signal routing. A logic 0 selects the originate mode with the opposite channel orientation.
5	I	Osc in	Accepts a CMOS level frequency reference at 2.304 or 3.5795 MHz as selected to generate the SCF 52.36 KHz clock used internally
16	I	Rx in	Receive signal filter input
7	O	Rx out	Receive signal output from equalizer
1	I	Tx in	Transmit signal filter input
8	O	Tx out	Transmit signal output from equalizer
2	I	VDD	+5V −5%, +25% power input
11	I	VSS	−5V +5%, −25% power input
10	I	Clk Sel	Clock select pin. Connecting pins 10 and 11 changes the internal divider ratio to allow use of a standard 3.5795 Mhz color burst crystal reference to generate the 52.36 KHz SCF clock The 2 304 MHz clock input is selected when pin 10 is left open. (has internal pull-up)

ELECTRICAL: SPECIFICATIONS

Digital signals: pins 5,6,10,13

High level input voltage...VIH ..... 3.75V Minimum
High level input current...IIH ..... 10μA Maximum
Low level input voltage...VIL ..... 0.8V Maximum
Low level input current...IIL ..... −10μA Maximum

Clock input: pin 5

Input clock frequency ..... 2.304 or 3.5795 MHz ± 0 01%
Input clock duty cycle ..... 20% minimum, 80% maximum

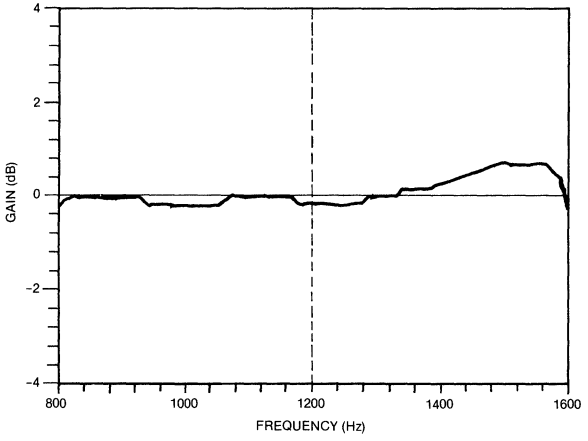
Analog signals: pins 1,2,3,4,7,8,11,12,15,16

Supply voltage, VDD... 4.75V minimum 6.25V maximum
Supply voltage, VSS... −4.75V minimum −6.25V maximum
Supply current, IDD...(VDD = 5.0V) .. 10 mA maximum
Supply current, ISS...(VSS = − 5.0V) .. −10 mA maximum
Input impedance, Zin ..... 10 kΩ minimum
Output impedance, Zout (pins 3, 12)..... 100 kΩ typical
Output impedance, Zout (pins 7, 8)..... 1 kΩ maximum
Output noise, C-message ..... 950 μV RMS maximum
Channel separation ..... 50 dB minimum
Input signal level ..... VDD-2.0V P-P maximum
Supply imbalance, VDD + VSS ..... 0.5V maximum
Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... −55 to 125 °C

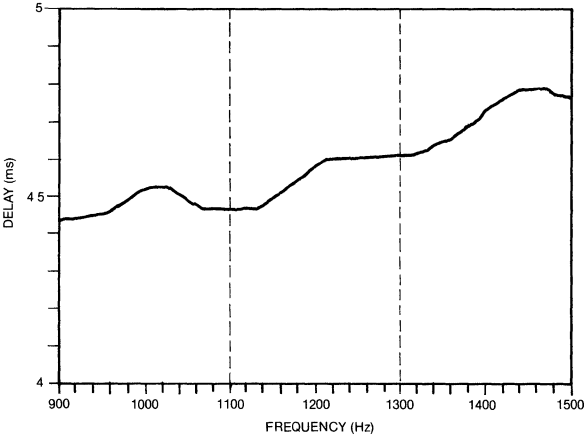
TYPICAL FREQUENCY RESPONSE

(Ta = 25°C, V_{DD} = 5.0V, V_{SS} = −5.0V)

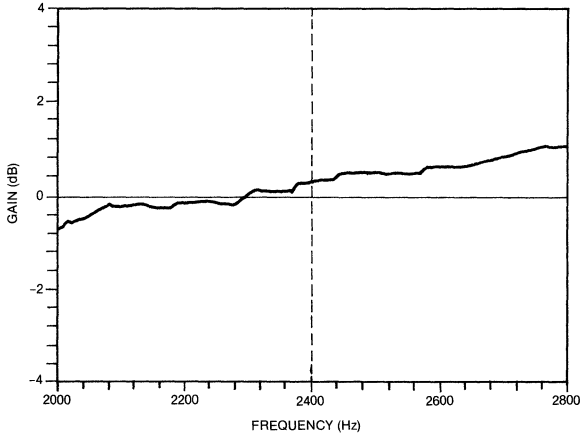
LOW BAND
Amplitude Response (dB)



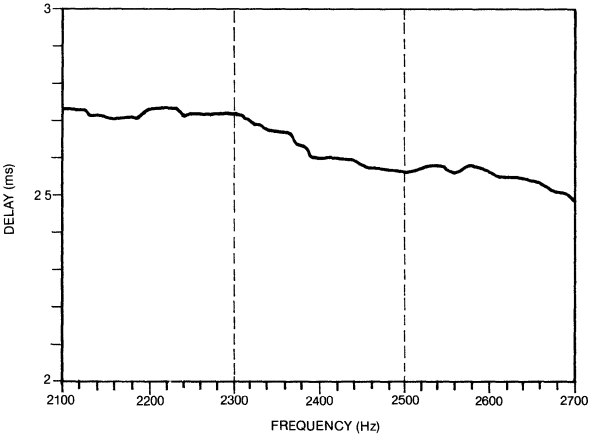
LOW BAND
Group Delay (ms)



HIGH BAND
Amplitude Response (dB)



HIGH BAND
Group Delay (ms)



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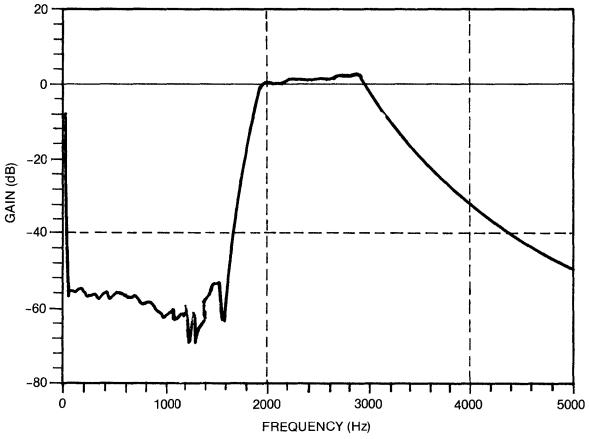
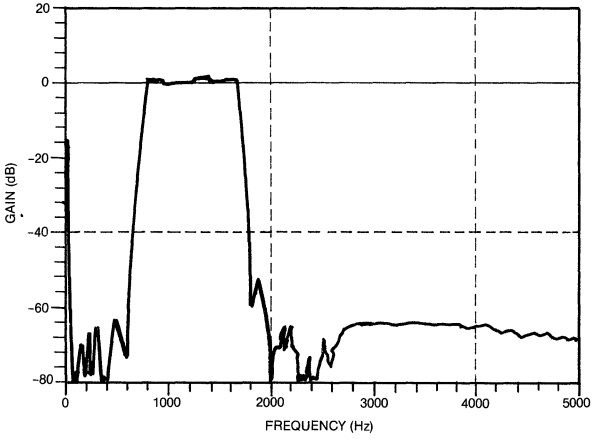
TYPICAL PERFORMANCE

(T_A = 25°C, V_{DD} = 5.0V, V_{SS} = – 5.0V)

HIGH BAND
Amplitude Response (dB)



LOW BAND
Amplitude Response (dB)



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SSI 263A Phoneme Speech Synthesizer

Data Sheet

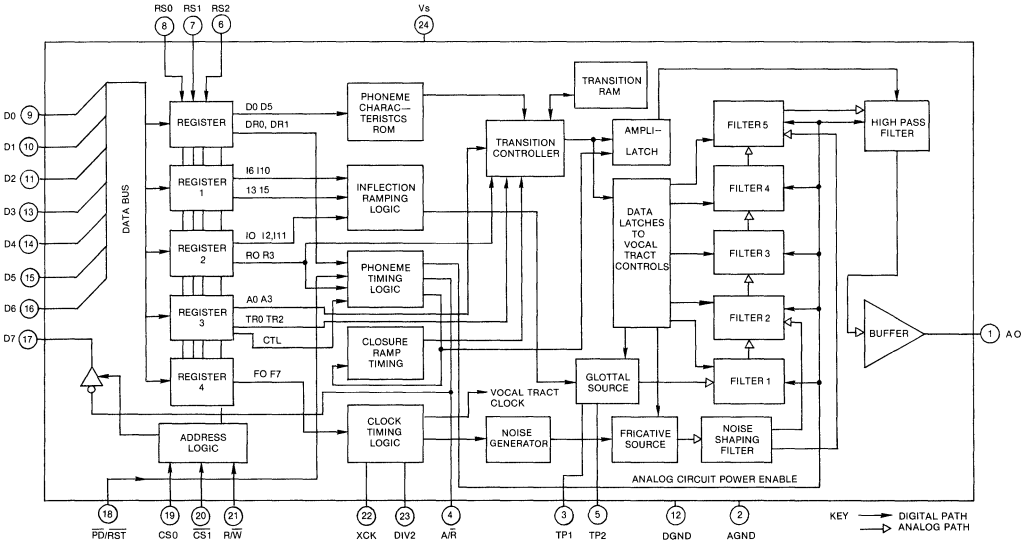
DESCRIPTION

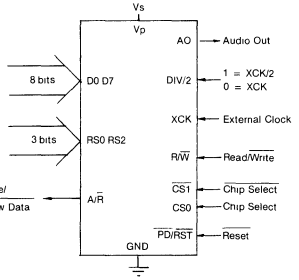
The SSI 263A is a versatile, high-quality, phoneme-based speech synthesizer circuit contained in a single monolithic CMOS integrated circuit. It is designed to produce an audio output of unlimited vocabulary, music and sound effects at an extremely low data input rate.

Speech is synthesized by combining phonemes, the building blocks of speech, in an appropriate sequence. The SSI 263A contains five eight-bit registers that allow software control of speech rate, pitch, pitch movement rate, amplitude, articulation rate, vocal tract filter response, and phoneme selection and duration.

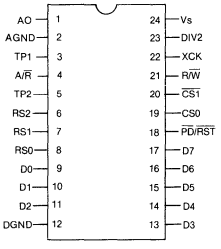
FEATURES

- **Single low-power CMOS integrated circuit**
- **5 Volt supply**
- **Extremely low data rate**
- **8-bit bus compatible with selectable handshaking modes**
- **Non-dedicated speech, ideal for text-to-speech programming**
- **Programmable and hard powerdown/reset mode**
- **Switched-capacitor-filter technology**





Signal Diagram



SSI 263A Pin Out
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

SSI 263A Operation Description

This short description is intended to provide SSI 263A feature and capability information only. Refer to the SSI 263A USERS GUIDE for complete information on application and phonetic programming.

The Production of Speech

To produce different speech phonemes (sounds) the SSI 263A uses a model of the human vocal tract. Within the device this analog tract is modeled with five cascaded programmable low pass filter sections. The filter sections are programmed internally by a digital controller. Either a glottal (pitch) or a pseudo-random noise source is used to excite the vocal tract, depending on whether a voiced or non-voiced phoneme is selected. During speech production the phonemes will typically last between 25 and 100 mS.

The Speech Attribute Registers

Speech is produced by programming speech attribute (characteristic) data into five eight-bit registers. These internal registers allow selection of phonemes and speech characteristics. Refer to the Register Input Formats for the functional allocations.

Device Response to Attribute Register Data

The SSI 263A has two general classes of attribute data: "control" data (speech rate, filter frequency, phoneme articulation rate, phoneme duration, immediate inflection setting, and inflection movement rate) and "target" data (phoneme selection, audio amplitude, and transitioned inflection). The SSI 263A responds immediately upon loading "control" data; upon loading "target" data the device will begin to move towards that target at the prescribed transition rates. This fully internal linear transitioning between target values, done in a manner as is found in normal speech, is a key factor in reducing control data rate without sacrificing speech quality.

Attribute Register Writing

The eight bit data bus D7-D0 loads the particular attribute register selected by the three bit address bus RS2-RS0. To write the data, R/$\overline{W}$ (Read/Write), CS0 (Chip Select 0), and $\overline{CS1}$ pins must first be in the 0,1,0 state, respectively. The data is then written when at least one of these pins changes state. Refer to the Write Timing Diagram. Writing is accomplished by changing preferably CS0 or $\overline{CS1}$. Following device power up, nominal values should be loaded into the attribute registers as described below.

Approximate Data Transfer Rate

For speech production using the SSI 263A, the actual data rate depends on the amount of speech attribute manipulation. For example, the production of monotonic speech, where phoneme and duration are the only attribute manipulations, requires a data rate less than 100 bits-per-second. A higher data rate of about 500 bits-per-second is required for high quality speech due to the associated full attribute manipulation.

Selectable Operation Modes

The state of the Duration/Phoeme Register bits DR1 and DR0 determine the operating mode of the device when the Control bit (CTL) is changed from a logic one to a logic zero. The four modes of operation include choice of timing response between "frame" or "phoneme" timing (as explained below), transitioned or immediate inflection response, and setting the A/$\overline{R}$ (Acknowledge/Request Not) pin active or disabled. Refer to the Mode Selection Chart.

Phoneme Selection

The SSI 263A can produce the 64 phonemes listed on the Phoneme Chart. Bits P5-P0 are used for phoneme selection. The relative phoneme duration is set by bits DR1 and DR0.

Phoneme Articulation Adjustment

A particular phoneme is produced by the combination of vocal-tract low-pass filter settings, excitation source type, and source amplitude. When a new phoneme is selected, the device performs a linear transition to the new set of characteristics. The rate of this transition is controlled by the articulation setting, bits TR2-TR0. This rate is relative in that articulation is not affected by speech rate bits R3-R0. A typical articulation register setting is "5".

Programming Inflection (Pitch)

When the SSI 263A is in the mode of immediate inflection, bits I11-I0 provide immediate adjustment with seven octaves of pitch on an even tempered scale. With the device in the transitioned inflection mode, bits I10-I6 select the target pitch and bits I5-I3 determine the inflection rate of change. Bits I11, I2, I1, and I0 always provide immediate adjustment. A typical value used for speech production is 90Hz where:

$$\text{Inflection Frequency} = \frac{\text{XCK frequency}}{8 \times (4096 - I)}$$

I = decimal equivalent of Inflection Register setting

Filter Frequency Setting

Data bits FF7-FF0 set the clock frequency for the switched-capacitor vocal tract filters. This determines overall filter frequency response. Inflection pitch is not affected by these bits. Typically this is set to give a clock frequency of about 20KHz (see formula below), but may be manipulated to fine-tune speech quality or to change "voice type"; bass, baritone, etc.

$$\text{Filter Frequency} = \frac{\text{XCK frequency}}{2\,(256 - FF)}$$

FF = decimal equivalent to the Filter Frequency Register setting.

Speech Rate

Rate of speech is controlled by bits R3-R0, the Speech

Rate Register. In Frame Timing Mode new attribute data is requested at the end of a "frame" where:

$$\text{Frame Duration} = \frac{4096 \times (16\text{-}R)}{\text{XCK frequency}}$$

R = decimal equivalent of Rate Register setting

In the Phoneme Timing Mode the frame duration is modified by the phoneme duration bits DR1 and DR0 where:

Phoneme Duration = (Frame Duration) X (4-D)

D = decimal equivalent of Duration Register setting

All internal attribute transitioning is performed relative to the Speech Rate Register setting. Speech rate does not effect inflection or filter frequency. A typical rate setting is hexadecimal "A".

Amplitude Adjustment

The overall Audio Output level is set with register bits A3-A0. Since each phoneme has a preset amplitude relative to other phonemes, it is not necessary to program the amplitude of each phoneme; however, amplitude changes may be used to enhance the speech quality and add emphasis. Amplitude is transitioned linearly at rate dependent on the phoneme duration setting. A typical amplitude setting is hexadecimal "C".

Control Bit and Power Down Mode

Setting the Control bit (CTL) to a logic one puts the device into Power Down mode, a sort of "standby". This bit is also set high when the $\overline{PD}/\overline{RST}$ pin is brought low and also upon power up. The Power Down mode turns off the excitation sources and analog circuits to reduce power consumption, but maintains the present register settings. Upon a Control bit logic one-to-zero transition, the present settings of DR1 and DR0 determine the operation mode as described above.

Register Reading

Device pin D7 becomes an output, as the inverted state of A/$\overline{R}$, when the device is put into Read (R/$\overline{W}$ is a logic 1 and the chip is selected, $\overline{CS1} = 0$, CS0 = 1). Refer to the Read Timing Diagram. The register address bits are ignored.

Time Base

Many different time bases may be utilized (see external clock input specifications). It is desirable to establish a stable crystal controlled time base from 800 to 1000KHz when DIV2 is set low, or twice the frequency when DIV2 is set high. A good time base can be easily accomplished with an inexpensive colorburst 3.5795 MHz crystal in conjunction with a divide-by-two circuit. The actual device timing and output frequencies are directly related to the time base frequency used.

Microprocessor Interfacing

Either the A/$\overline{R}$ line, or D7 as an output, are used as an interrupt to indicate when the duration of a frame or phoneme has been exceeded. No detectable degradation to speech quality results when several milliseconds occur between data request and load.

PHONEME CHART

Hex Code*	Phoneme Symbol	Example Word (or Usage)
00	PA	(pause)
01	E	MEET
02	E1	BENT
03	Y	BEFORE
04	YI	YEAR
05	AY	PLEASE
06	IE	ANY
07	I	SIX
08	A	MADE
09	AI	CARE
0A	EH	NEST
0B	EH1	BELT
0C	AE	DAD
0D	AE1	AFTER
0E	AH	GOT
0F	AH1	FATHER
10	AW	OFFICE
11	O	STORE
12	OU	BOAT
13	OO	LOOK
14	IU	YOU
15	IU1	COULD
16	U	TUNE
17	U1	CARTOON
18	UH	WONDER
19	UH1	LOVE
1A	UH2	WHAT
1B	UH3	NUT
1C	ER	BIRD
1D	R	ROOF
1E	R1	RUG
1F	R2	MUTTER (German)
20	L	LIFT
21	L1	PLAY
22	LF	FALL (final)
23	W	WATER
24	B	BAG
25	D	PAID
26	KV	TAG (glottal stop)
27	P	PEN
28	T	TART
29	K	KIT
2A	HV	(hold vocal)
2B	HVC	(hold vocal closure)
2C	HF	HEART
2D	HFC	(hold fricative closure)
2E	HN	(hold nasal)
2F	Z	ZERO
30	S	SAME
31	J	MEASURE
32	SCH	SHIP
33	V	VERY
34	F	FOUR
35	THV	THERE
36	TH	WITH
37	M	MORE
38	N	NINE
39	NG	RANG
3A	·A	MARCHEN (German)
3B	.OH	LOWE (French)
3C	U	FUNF (German)
3D	·UH	MENU (French)
3E	E2	BITTE (German)
3F	LB	LUBE

*Note — Hex codes shown with DR0, DR1 = 0 (longest Duration)

PIN ASSIGNMENT DESCRIPTIONS

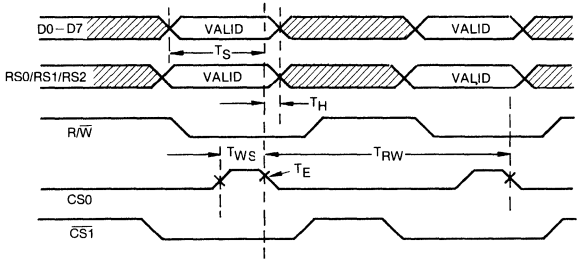
Pin No.	Symbol	Active Level	Description
1	AO		Analog Audio Output biased @ $V_{DD}/2$ requires an external audio amp for speaker drive
2	AGND		Analog Ground
3	TP1		Do not use
4	A/$\overline{R}$		Acknowledge/Request Not — open collector output changes from high to low level after phoneme is generated. May be used as an interrupt request for new phoneme data. (See Pin 17 also.)
5	TP2		Do not use
6	RS2		Register Select Input – used to select one of five internal registers in conjunction with RS1 and RS0
7	RS1		Register Select (See pin 6)
8	RS0		Register Select (See pin 6)
9	D0		LSB of 8-bit data bus — input only
10	D1		Data Input (only)
11	D2		Data Input (only)
12	DGND		Digital Ground
13	D3		Data Input (only)
14	D4		Data Input (only)
15	D5		Data Input (only)
16	D6		Data Input (only)
17	D7		MSB of 8-bit data bus. Bi-directional, inverse of pin 4 when read is high
18	$\overline{PD}/\overline{RST}$	Low	Power Down Control Input — Silences audio output and retains DC bias without disturbing register contents. Disables A/$\overline{R}$ output.
19	CS0	High	Chip Select Input
20	$\overline{CS1}$	Low	Chip Select Input
21	R/$\overline{W}$		Read/Write Control Input — Write is active low for loading internal registers. Read is active high but enables D7 only.
22	XCK		Clock Input ($\simeq$11 or 2 MHz)
23	DIV2	High	Clock Divide by Two — used when external clock is $\simeq$ 2 MHz
24	VDD		Positive Voltage Supply

REGISTER INPUT FORMATS

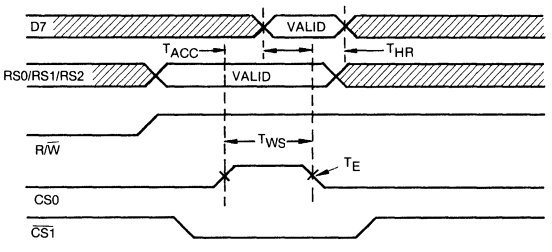
Register Address			Register Name	Bus Input Bit Position							
RS2	RS1	RS0		D7	D6	D5	D4	D3	D2	D1	D0
LO	LO	LO	Duration/Phoneme (DR/P)	DR1	DR0	P5	P4	P3	P2	P1	P0
LO	LO	HI	Inflection (I)	I10	I9	I8	I7	I6	I5	I4	I3
LO	HI	LO	Rate/Inflection (R/I)	R3	R2	R1	R0	I11	I2	I1	I0
LO	HI	HI	Control/Articulation/Amplitude (C/A/A)	CTL	T2	T1	T0	A3	A2	A1	A0
HI	X	X	Filter Frequency (F)	F7	F6	F5	F4	F3	F2	F1	F0

DR1, DR0 . . Define the phoneme duration.
P5 → P0 . . Address the phoneme required.
I11 → I0 . . . . Define inflection target frequencies and rate of change.
R3 → R0 . . . Define the rate or speed of speech.
CTL . . . . . Define the mode of A/$\overline{R}$ response in conjunction with DR1 and DR0. Also directly set by PD/$\overline{RST}$.
T2 → T0 . . . . Define the rate of movement of the formant position for articulation purposes.
A3 → A0 . . . Define the amplitude of the output audio.
F7 → F0 . . . Define the frequency of all vocal tract filters.

WRITE TIMING DIAGRAM



READ TIMING DIAGRAM



*Valid data latched on first rise or fall of R/W, CS0 or CS1 into inactive

Timing Characteristics (V_{DD} = 4.5 to 5.5 Volts, TA = -40 to +85 deg. C)

Item	Symbol	Limits		Units.
		Min.	Max.	
Data Setup Time	TS	120**		nsec
Data Hold Time	TH	10**		nsec
Strobe Width	TWS	200		nsec
Read/Write Cycle Time	TRW	2.25*		μsec
Rise/Fall Time	TE		100	nsec
D7 Output Access Time	TACC		180	nsec
D7 Output Hold Time	THR		180	nsec

Notes. * Based on color burst frequency

** Timing relative to deselect by either CS0, CS1, or R/W changing

MODE SELECTION CHART

DR1	DR0	'CTL' BIT	Function
HI	HI	HI→LO	A/$\overline{R}$ active; phoneme timing response; transitioned inflection (most commonly used mode)
HI	LO	HI→LO	A/$\overline{R}$ active; phoneme timing response; immediate inflection
LO	HI	HI→LO	A/$\overline{R}$ active; frame timing response; immediate inflection
LO	LO	HI→LO	Disables A/$\overline{R}$ output only; does not change previous A/$\overline{R}$ response

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Limit	Units
Supply Voltage	V_{DD}—V_{SS}	7.0	V
Input Voltage	V_{IN}	–0.5 to V_{DD} + 0.5	V
D.C. Current at Inputs	I_{INM}	± 1.0	mA
Storage Temperature	TS	–55 to + 125	°C
Operating Temperature	TA	–40 to + 85	°C
Power Dissipation	Pd	500	mW

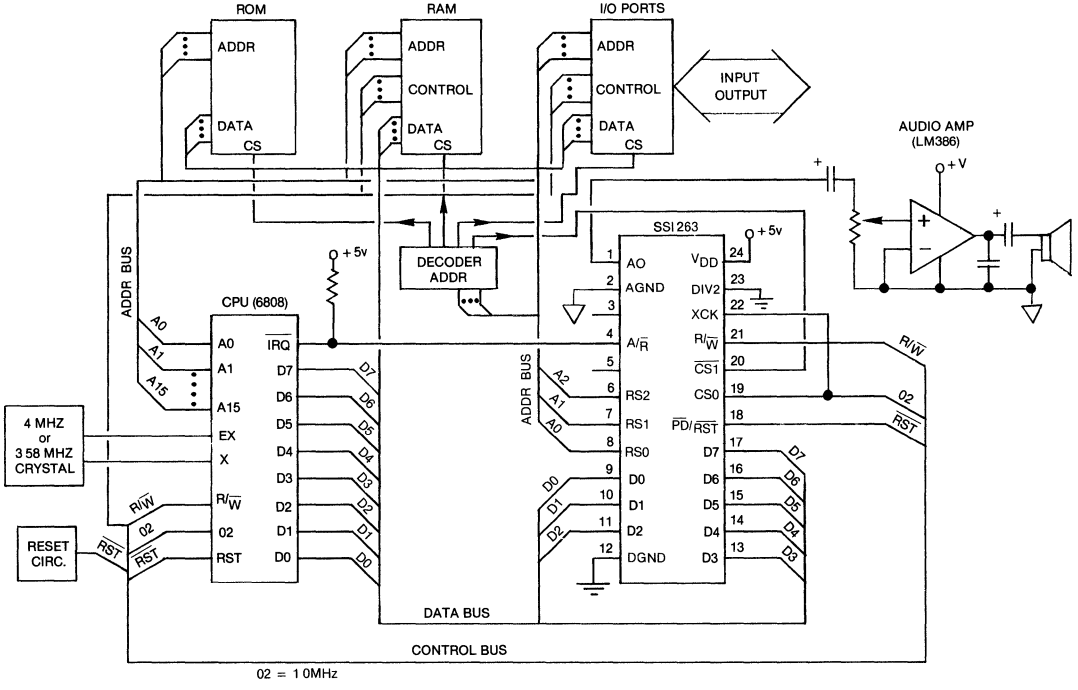
Electrical Characteristics Unless otherwise specified, 4.5 ≤ V_{DD} ≤ 5.5; —40 deg. C ≤ TA ≤ 85 deg. C;
1.50MHz ≤ XCK frequency ≤ 2.0MHz, when XCK/2 = logic 1 or
0.75MHz ≤ XCK frequency ≤ 1.0MHz, when XCK/2 = logic 0

Description	Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY					
Supply Current	$\overline{PD}/\overline{RST}$ = 1, CTL = 0		8	20	mA
Supply Current	$\overline{PD}/\overline{RST}$ = 0, CTL = 1		7	18	mA
AUDIO OUTPUT					
Output Level	AW phoneme RL = 50Kohm to GND through 1μF cap.	0.28VDD	0.37VDD	0.50VDD	Vpp
DC Output Offset		0.5VDD	0.6VDD	0.7VDD	V
Resistive Loading	AC coupled to AO to GND	10			Kohm
Capacitive Loading	To GND to ensure Stable A			100	pF

Description	Conditions	Symbol	Min	Typ	Max	Units
BUS CONTROL INPUTS, DATA INPUTS (RS0, RS1, RS2, CS0, CS1, D0-D7 PD/RST)						
Input High Voltage		V_{IH}	V_{SS} + 2.4		V_{DD} + 0.3	VDC
Input Low Voltage		V_{IL}	—0.3		+ 0.8	VDC
Input Leakage Current	V_{IN} = 0 to V_{DD}	I_{IN}			5	μA
Input Capacitance	V_{IN} = 0 T_A = 25 °C measured at f = 1.0MHz	C_{IN}			10	pF
Input Capacitance, D7 Input		$C_{IN(D7)}$			20	pF
Input Current, D7 in TRI-State "OFF" State	V_{IN} = 0.4 to 2.4 V	$I_{IN(TS)}$		2.0	5.0	μA
D7 OUTPUT						
D7 Output Low Voltage	I_{Load} = 0.4 mA into D7	$V_{OL(D7)}$			0.4	VDC
D7 Output High Voltage	I_{Load} = 205 μA out of D7	$V_{OH(D7)}$		V_{DD}-2.0		VDC
A/$\overline{R}$ OUTPUT						
Output Low Voltage	I_L = 3.2 mA into A/$\overline{R}$	$I_{OL(A/\overline{R})}$			0.4	VDC
Output High Leakage Current	V_{Out} = 0.0 to V_{DD}	$I_{L(A/\overline{R})}$			10	μA
Output Capacitance	V_{Out} = 0 VDC T_{AMB} = 25 °C f = 1.0 MHz	$C_{Out(A/\overline{R})}$		15	pF	
DIV2 INPUT						
Input Low Voltage		$V_{IL(DIV2)}$	-0.3		.2 V_{DD}	V
Input High Voltage		$V_{IH(DIV2)}$	.8V_{DD}		V_{DD} + 0.3	V
Input Leakage	V_{IN} = 0 to V_{DD}				5	μA

Description	Conditions	Symbol	Min.	Typ.	Max.	Units.
XCLK						
Input Low Voltage		$V_{IH(IC)}$	−0.3		+0.8	V
Input High Voltage		$V_{IH(IC)}$	2.4		V_{DD} + 0.3	V
Input Current	V_{IN} = 0.0 to V_{DD}	$I_{IN(C)}$			5	μA
Input Capacitance		$C_{IN(C)}$			10	pF
Duty Cycle		D(XCLK)	0.4		0.6	—

TYPICAL MICROPROCESSOR IMPLEMENTATION



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User's Guide for Phonetic Programming Using the SSI 263A

Phonetics

Every speech sound (phoneme) in any language may be represented by a special symbol (phonetic symbol). These symbols are used in WRITING precisely the sound sequence (phonetic transcription) of a word according to the way it is pronounced. There are many different phonetic symbol sets (phonetic alphabets). Each would contain a minimum number of symbols to represent the basic sounds (phonemes) required to pronounce any word in the language. Additional symbols are usually included which represent sounds with slight to great variations in the basic sounds (allophones). These symbols are used to assist in the transcription of words that reflect a regional, dialectic, or foreign pronunciation.

The process of transcribing a spoken word into its phonetic components begins with identifying the number of sounds in the word, then tagging each with a label to specify its type. Consonants and vowels are the most familiar labels but these may be broken down into subtypes (e.g., stop consonants, back vowels, etc.) as the need for more specificity arises. Once the sounds have been identified, their symbols are selected, then written in sequence. The resulting transcription should allow another person to identify the pronunciation without having heard the word spoken.

Note that when using a phonetic alphabet to transcribe words into their sound sequences, there is not a one-to-one correspondence between the alphabet characters (orthographics) used to spell words and the phonetic symbols (phonetics) used to represent their pronunciations. For example, in the word "phones" there are 6 letters but only 4 sounds. Conversely, the word "I" has 1 letter but 2 sounds. It may be of some assistance to keep a dictionary handy for reference. Dictionaries use their own phonetic system to describe the pronunciations of every word entry. It will be necessary to learn at least one phonetic alphabet in order to engage in phonetic transcription. The SSI 263A Phonetic Alphabet is the referent used in this manual. However, if another system is already known, it is easily translated into the referent.

When transcribing vocabulary from orthography (standard alphabet spelling) to phonetics, it is common to place the phonetic sequence between right slash marks when the transcription appears in running text. The word "phones," for example, would be transcribed as /F O N Z/ when using SSI 263A phonetic symbols. This allows the reader easier identification of phonetic segments.

SSI 263A Phonetic Alphabet

The phonetic alphabet used to represent the SSI 263A phonemes is the SSI 263A PHONETIC ALPHABET. Refer to the Phoneme Chart for a complete listing of the phoneme symbols.

Of the 64 alphanumeric symbols in the SSI 263A Phonetic Alphabet, 34 represent sound BASIC to the pronunciation of American English. The remaining 30 symbols fall into 2 groups: the ALLOPHONE group and the NO-SOUND group. The BASIC sound symbols are:

A, AE, AH, AW, B, D, E, EH, ER, F, HF, I, J, K, KV, L, M, N, NG, O, OO, P, R, S, SCH, T, TH, THV, U, UH, V, W, Y, Z.

Symbols in the ALLOPHONE group represent speech sounds that vary in pronunciation from one of the basic sounds. They may be used in transcribing words or word segments (syllables or morphemes) whose pronunciations are not satisfied by the basic phonemes alone (words rooted in a foreign language, words adapted by a regional dialect, etc.). The ALLOPHONE symbols are:

A1, AE1, AH1, AY, E1, E2, EH1, HN, HV, IE, IU, IU1, L1, LB, LF, OU, R1, R2, U1, UH1, UH2, UH3, YI,:A, :OH, :U, :UH.

The NO-SOUND symbols represent silent states. One of these symbols represents a "pause" state. It is used to separate phoneme sequences into phrase-like segments which assist in more closely imitating the natural pausing in human speech for breathing or for delayed emphasis. The "pause" is treated as a phoneme when it is selected for a transcription and will be subject to phoneme parameter programming. It has the ability to maintain the parametric levels of duration, inflection, amplitude, etc., during its silence, thus audibly affecting the movement of the preceding and following phonemes. Other NO-SOUND symbols represent "hold" states. They are used in combination with BASIC phonemes or ALLOPHONEs to generate articulation variations on their pronunciations. The NO-SOUND symbols are.

HFC, HVC, PA.

Now that there is a tool to use for writing the sounds that are heard, the next stage is to identify the sounds that are produced by the SSI 263A speech synthesizer

SSI 263A Phoneme Review

Thus far in this program, it has been established that: (1) spoken words are made up of a series of sounds; (2) each speech sound in a language may be represented by an identifying symbol; and (3) the spoken word may be written according to its sound sequence using these special symbols. Before a word may be written phonetically, however, users may wish to study further the SSI 263A speech sounds. What makes one sound different from another and how these differences may be helpful to phonetic programming will be essential information for phonetic programmers.

The sound that is represented by each phonetic symbol in the SSI 263A Phonetic Alphabet must be audibly learned. The easiest way to approach this task is to start with the sounds already known and associate a symbol with them. For example, from spelling we have already learned that vowels may be "long" or "short" and are often differentiated by their particular spelling formats. Every time a word with a "short a" sound is heard (sat, fat, cat, bat, happy, plaster, ankle, Saturday, amplify, contaminate, etc.) the symbol /AE/ should come to mind. A "long a" sound (fate, state, bait, lace, maybe, stable, arrangement, etc.) is actually a diphthong (two sounds combined into a single unit) and may be represented by the symbols /A AY/.

In standard orthography, there are only 5 vowel letters to represent 17 vowel sounds. In phonetics, each vowel sound will be represented by its own symbol or symbol combination.

Again, from spelling, we have learned that the letter "c" may have a hard sound as in "cat" or a soft sound as in "city." The hard sound is actually a /K/ as in "kite" and the soft sound is an /S/ as in "sing." Users must identify which sound (/K/ or /S/) is used in the transcription of a "c." You will not find a symbol C in a phonetic alphabet. Like "C," the letters "Q" and "X" will not be found in phonetic alphabets. They are transcribed into the sound sequences /K W/ and /K PA S/. Refer to the Phoneme Chart during this learning period. It provides example words to describe the pronunciations corresponding to each symbol.

Users may add more words to the examples above to continue identifying the symbol-sound relationship for /AE/ and /A AY/. Follow this technique for each symbol in the alphabet. For auditory verification, enter the sound that is being reviewed into the device. Speak aloud your example word for the SSI 263A

sound in an attempt to match that which the synthesizer is emitting.

Example: /E/ = "long e" vowel sound
= meat, read, need, repair, before, phoneme, erase, brief, people, timeliness, seniority, receive, catastrophe.

Example: /F/ = "voiceless fricative" consonant
= farm, false, aft, feet, finger, phrase, phone, Africa, alphabet, cough.

Once you have reviewed auditorily the sounds you already have a familiarity with from spelling, proceed to the BASIC sound list in the above text and continue the review. Be aware that several consonant sounds will not provide output unless they have another sound following. This is the case with /B/, /D/, /P/, /T/, and /K/. When one of these sounds is entered into the SSI 263A, follow it by a vowel and listen to both in sequence.

Users who already have a familiarity with phonetics and SSI 263A synthetic sounds, may wish to follow the sound review procedures in order to auditorily determine the difference between two sounds or identify new ones. For example, enter the /UH/ phoneme into the device. Then enter /UH1/, /UH2/, and /UH3/. Listen to each sound noting the pronunciation variations. Be aware that there are no duplicate sounds resident on the SSI 263A chip.

Whenever a SSI 263A sound is audited that cannot be readily identified as to its appropriate usage, do not be concerned. The review is designed only to provide a method for establishing an auditory memory for each sound and a visual memory for its symbol. Phonetic programming may begin anytime after the initial review. Return to the review later as your familiarity with the BASIC sounds increases and as your need for sound alternatives to those BASIC sounds becomes more apparent.

If there is a question as to which symbols should be chosen to transcribe a word into its sound sequence, make a written note of the word by circling the letter(s) that present the problem. Later, when phonetic programming has begun, a phoneme sequence may be created for the word and users may verify auditorily which phonetic selection produces the most appropriate translation.

SSI 263A Phoneme Discussion

The SSI 263A Phonetic Alphabet is divided into 3 groups for the purpose of differentiating between phonemes and allophones. Another way of dividing the Alphabet is according to usage. The most familiar division is a two sections split: CONSONANT sounds and VOWEL sounds. Within each of these sections, sounds may be further subdivided according to the distinctive features that best describe the sounds phonetically or acoustically. The more that is known about a sound, the easier it is to determine how it may be used in transcribing and phonetically programming a word.

Consonant Sounds

There are 22 Consonant Phonemes, subdivided according to their manner of production in the human speech mechanism. Some are characterized by the noise emitted when the articulators obstruct the air flow (Fricatives like /S/). Vowel-like consonants have the least amount of obstruction and may occasionally be used as a vowel substitute. Stop consonants are obstructed completely, release of air flow occuring at the onset of the next sound. Notice that Affricates are a sequence of 2 sounds (a Stop followed by a Fricative) spoken as a single unit. Unlike vowels, which always have a vocal source during production, consonants may be voiced (V) or unvoiced (U) (no vocal source during air flow). When listening to the manner in which a consonant is produced during speech, note its special characteristics that distinguish it from all other consonants. The figure below displays all of the consonant sounds within their production groups.

	Stops	Fricatives	Affricates
Voiced	B, D, KV	Z, V, J, THV	(D, J)
Voiceless	P, T, K	S, F, SCH, TH, HF	(T, SCH)

	Semi-vowels	Glides	Nasals
Voiced	R, L	W, Y	M, N, NG
Voiceless			

Consonant Chart

Voiced and voiceless consonants are subdivided into 6 categories according to the manner in which they are produced in the human vocal tract: i.e., how the air flow is obstructed by the articulators to make each sound different.

Consonant sounds are selected for a sequence in much the same manner as an alphabet character would be selected for the spelling of a word. Users must be alert, however, to identify the exceptions. Occasionally, a consonant appears in the spelling of a word but not in its sound sequence: the "b" in "comb" is not pronounced and the sound sequence reflects the absence of the "b": /K OU M/. Some exceptions have grammatical rules that may be used in determining the appropriate sound. For example, a consonant may have 2 pronunciations according to its sound environment. The "s" used to pluralize the two words that follow are pronounced differently based on whether the sound that precedes it is voiced or unvoiced. An "s" pronunciation will match the voicing characteristics of the sound it follows.

Examples: tips = /T I P S/
tabs = /T AE B Z/

There are other types of consonantal exceptions. For example, the "t" in a word like "nation" is pronounced /SH/ and the program might look like this: nation = /N A AY SH UH3 N/. Users must listen to each word's pronunciation to determine the appropriate phoneme selection.

There are 7 Consonant Allophones, each noted in the table below. The /L/ consonant is used in the initial position of a sequence for words beginning with "L", while the /LF/ allophone will occupy a medial or final position in a sequence: e.g., lull = /L UH LF/. The /LB/ and the /LI/ allophones would be used when a most constricted pronunciation of an "L" was required, as would occur for some words of foreign languages.

Consonant Phoneme	Consonant Allophones	Consonant Phoneme	Vowel Allophone
L	L1, LB, LF	R	ER
R	R1, R2	Y	YI

Allophone Listing for /L/, /R/, & /Y/

The /R/ is an initial position phoneme. Both /R1/ and /R2/ have more constricted pronunciations than /R/ and may be used in sequence with soundless interrupts to create a trilled /R/. Often when the /R/ is required in a medial or final position, it is vowelized and the /ER/ is used. Listening to the production of all four of these sounds will auditorily show that they may, occasionally, be used interchangeably.

Examples: red = /R EH D/
bird = /B ER D/
motor = /M OU T ER/

The /Y/ consonant, used as the final sound in words ending with "y," has a vowel allophone that may be used as the initial sound of words starting with "y." Note that both /Y/ and /YI/ are auditorily very close to the /E/ and the /IE/ vowels and may be considered interchangeable.

Vowel Sounds

There are 12 BASIC Vowel Phonemes. Vowels are subdivided according to the manner in which they are produced. All vowels are voiced sounds but each has a different output based on the degree of obstruction created by the opening of the mouth and the tongue position. Lip positions, another obstructing articulator, may range from spread flat to round. While the lips are in any of these positions, the jaw may be simultaneously dropped from a closed to an open position.

	Front Vowels	Medial Vowels	Back Vowels
	Spread	——→	Rounded
Closed	E		U
	I		OO
	A	UH	O
	EH	(ER)	AW
Open	AE		AH

Vowel Quadrilateral

Vowels begin their production with the same voiced energy. Changes in the position of the tongue (front or back), the shape of the lips (from spread flat to rounded), and the position of the lower jaw (from closed to open) determine the final characteristics that allow listeners to distinguish between vowel sounds.

Refer to the SSI 263A Phoneme Chart for the pronunciation reference on each BASIC vowel sound. Utilize the sound review techniques on the previous pages to practice identifying the vowel sounds in words and associating them with their phonetic symbols.

The allophonic variations of vowels, 20 in number, are used in a phonetic program to enhance the pronunciation of a word. There are some cases where the allophone is required for articulate pronunciations. This is true for /AY/, /YI/ and /IU/, which are integral components in the phonetic sequences for the "long a" and the varied "long u."

Examples: same = /S A AY M/
you = /YI IU U/

The table below places each allophone into the vowel quadrilateral to demonstrate approximately how they might relate to the BASIC vowels. Users are in no way restricted to traditional phonetic transcriptions that use only the BASIC vowel phonemes. Be encouraged to experiment with allophones. Place them in different positions in a sequence to auditorily check how they effect the overall pronunciation of a word.

	Front Vowels	Medial Vowels	Back Vowels
	Spread	——→	Rounded
Closed	YI E1 IE		U1
	AY	E2	IU IU1
	A1	UH1	OU
	EH1	UH2	
Open	AE1	UH3	AH1

Allophone Placement in Vowel Quadrilateral

Vowel allophones are placed in the vowel quadrilateral according to their production features. The sounds they emit vary slightly from the BASIC vowels that occupy the same positions.

Four vowel allophones—/:A/, /:OH/, /:U/, and /:UH/ — are adapted pronunciations of four of the BASIC vowels. These sounds are most commonly used for phonetically programming a foreign word. They may also be used as transitory sounds to link phonemes with opposite production features such as a round, open vowel with a very constricted, narrow consonant.

There are five vowels that require two or more vowel sounds in sequence in order to achieve their pronunciations. These are generally referred to as diphthongs. Refer to the Diphthong Conversion Chart.

The vowel quadrilateral is a handy tool to use for selecting vowel phonemes for diphthongs and other multi-phoneme units. For example, the diphthong in the word "I" starts with an /AH/ and ends with an /E/. In order to move smoothly from the first sound to the second (transition), another vowel may be inserted between these two sounds in sequence. The most likely choice would be a vowel that falls somewhere between /AH/ and /E/ in the quadrilateral: e.g., /UH/, /EH/, /I/, etc. The sequence may look like this: /AH EH E/ or /AH1 UH3 IE/ or /AH1 EH3 AY/. In their fullest durations, a three-sound sequence would over articulate the diphthong. Shortening the first and last sounds by 1 duration and the medial sound by 2 durations will produce a more acceptable pronunciation (see SSI 263A Phoneme Parameters).

SS1 263A Phoneme Parameters (Attributes)

To achieve an accurate pronunciation of a word produced by the SSI 263A synthesizer requires more than a selection of the appropriate phonemes. Like human speech sounds, synthesized sounds are further defined by the rate at which they are emitted (duration), the level of pitch at which they are emitted (inflection or frequency), and the intensity with which they are produced (amplitude). These are considered the three major speech parameters which give the overall production of a word its linguistic character, transforming simple speech into more complex language. Inflection, amplitude, and duration are only three of the parameters that users have control of during the programming process. The rate at which one sound moves into another (articulation) is also a controllable parameter. Other parameters are: the slope of the inflection (slope), the rate of each selected duration (rate), and the extended inflection frequencies (extension). Users may also select the base frequency at which speech may be produced (filter frequency). Refer to SSI 263A Phoneme Parameters, for the range of each and typical default values selected.

Every phoneme selected for a sequence must be accompanied by assignments for each of the eight parameters. As users become more aware of their need to create different language effects with their synthesized speech output, they will require the flexibility and choice that comes with programmable parameters. For example, with 4 selectable durations per phoneme, each actual pronunciation of each sound may be changed. Thus, every sound has four possible outputs increasing the users' choice from 64 phonemes and allophones to 256. Each of the 256 may be effected differently by each of the 32 possible inflection assignments. Add to these possibilities 16 variations in amplitude and 16 variations in rate. The possible combinations are not limitless, of course, but they are very great and users are encouraged to experiment with as many as possible.

Several of the parameters effect synthetic speech output as a whole. These are articulation, pitch extension, and filter frequency. Users may select a single level at which to set the filter frequency, for example, and maintain that level throughout the programming process.

Phonetic Programming Methodology

Due to the great variety of phonemes and parameter choices, as well as the different effects the parameter selections have on the speech sounds, a systematic approach to selecting the variables is advised. The approach described below is only one of several that might be used. It may be adjusted to accommodate the user's special programming style or to accommodate later implementation of automatic control techniques.

The first step is to transcribe the target word, phrase, etc., into its basic phonetic components. Next, enter these sounds into the SSI 263A and auditorily check the output. Use the default values suggested in the Nominal Phoneme Parameter Table. The results should be a bit stilted if not misarticulated for the first trial program. Phoneme adjustment is next. Continue to make changes in the phoneme sequence, auditorily monitoring the changes, until an adequate pronunciation of the target is established.

Begin parameter adjustments. First, maintain articulation, pitch extension and filter frequency at nominal values. The device should be kept in the transitioned inflection mode. Make adjustments in the levels of only one of the remaining 4 parameters at a time, beginning with the duration and moving on to the inflection, rate, and amplitude (in that order) once the specific effect that the parameter can make has been made. Return to a previously adjusted parameter at any time based on need.

PHONEME CHART

Hex Code*	Phoneme Symbol	Example Word (or Usage)
00	PA	(pause)
01	E	MEET
02	E1	BENT
03	Y	BEFORE
04	YI	YEAR
05	AY	PLEASE
06	IE	ANY
07	I	SIX
08	A	MADE
09	AI	CARE
0A	EH	NEST
0B	EH1	BELT
0C	AE	DAD
0D	AE1	AFTER
0E	AH	GOT
0F	AH1	FATHER
10	AW	OFFICE
11	O	STORE
12	OU	BOAT
13	OO	LOOK
14	IU	YOU
15	IU1	COULD
16	U	TUNE
17	U1	CARTOON
18	UH	WONDER
19	UH1	LOVE
1A	UH2	WHAT
1B	UH3	NUT
1C	ER	BIRD
1D	R	ROOF
1E	R1	RUG
1F	R2	MUTTER (German)
20	L	LIFT
21	L1	PLAY
22	LF	FALL (final)
23	W	WATER
24	B	BAG
25	D	PAID
26	KV	TAG (glottal stop)
27	P	PEN
28	T	TART
29	K	KIT
2A	HV	(hold vocal)
2B	HVC	(hold vocal closure)
2C	HF	HEART
2D	HFC	(hold fricative closure)
2E	HN	(hold nasal)
2F	Z	ZERO
30	S	SAME
31	J	MEASURE
32	SCH	SHIP
33	V	VERY
34	F	FOUR
35	THV	THERE
36	TH	WITH
37	M	MORE
38	N	NINE
39	NG	RANG
3A	:A	MARCHEN (German)
3B	:OH	LOWE (French)
3C	:U	FUNF (German)
3D	:UH	MENU (French)
3E	E2	BITTE (German)
3F	LB	LUBE

*Note — Hex codes shown with DR0, DR1 = 0 (longest Duration)

SSI 263A Diphthong Conversion Chart

Phoneme Sequence	Example Words
A AY Y	rain, became, stay
A IE EH1 UH3 LF	mail, hale, avail
AH1 AE1 EH1 Y	time, rhyme, sky
AH1 EH1 IE AW UH3 LF	smile, style, while
AH1 EH1 IE UH3 ER	fire, liar, inspire
UH3 AH1 Y	mice, right, sniper
O U	road, stone, lower
OU O O	tore, four, floor
AH1 AW O U	loud, flower, hour
UH3 AH1 O U	house, about, ouch
O UH1 AH1 I IE	boy, noise, annoy
O UH3 EH1 I OO LF	boil, spoil, doily
IU U U	tune, spoon, do
YI IU U U	you, few, music

SSI 263A Multi-Unit Conversion Chart

Phoneme Sequence	Example Words
T HFC SCH	church, latch
KV HVC HF	good, lag, angry
D J	just, ledge, wage
KV HF HFC	lake, corn, check
P HF	pipe, pay, poor
K HF W	quest, quick, aqua
T HF	top, trip, strain
HFC K HF HVC S	six, exit, taxi

Nominal Phoneme Parameter Table (Suggested Default Values for Speech Development)

Amplitude (A3 → A0)
Range—0 to F (softest to loudest, 0 = silent)
Default—C
Exceptions—KV = 0, B = D = 6

Duration (DR1, DR0)
Range— 3 to 0 (shortest to longest)
Default—0

Filter Frequency Range (F7 → F0)
Range—00 to FF (lowest to highest)
Default—E9

Inflection (Pitch) (I10 → I6, Transitioned Inflection Mode Only)
Range—0 to 1F (lowest to highest, 0 = silent)
Default—04

Extension and Range of Pitch (I11, 12 → I0)
Range—0 to 7 (low); 8 to F (high)
Default Value—8

Rate of Speech (R3 → R0)
Range—0 to F (slowest to fastest)
Default—A

Slope of Inflection (I6 → I3, Transitioned Inflection Mode Only)
Range—0 to 7
Default—0

Articulation (Rate of) (A3 → A0)
Range—0 to 7 (slow to fast)
Default — 5

Example of Using Phonetic Programming Methodology:

Developing "Hello"

Phoneme Parameters							SSI 263 Register Data				
Pho.	D	T	In—S	A	R	E	FF	DP	IS	RE	TA	FF

KEY:
- Pho = Phoneme
- D = Duration
- T = Articulation
- In = Inflection
- S = Slope of Inflection
- A = Amplitude
- R = Rate
- E = Extension and Range of Pitch
- FF = Filter Frequency

DP	= Duration/Phoneme Register	Address 000
IS	= Inflection/Slope Register	001
RE	= Rate/Extension Register	010
TA	= Articulation/Amplitude Register	011
FF	= Filter Frequency Register	1XX

1. Original Phoneme Entry:

Pho.	D	T	In—S	A	R	E	FF	DP	IS	RE	TA	FF
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
HF	.0	5	0A-0	C	A	8	E9	2C	50	A8	5C	E9
EH	.0	5	0A-0	C	A	8	E9	0A	50	A8	5C	E9
L	.0	5	0A-0	C	A	8	E9	20	50	A8	5C	E9
O	.0	5	0A-0	C	A	8	E9	11	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9

2. Phoneme Selection Refinement

Pho.	D	T	In—S	A	R	E	FF	DP	IS	RE	TA	FF
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
HF	.0	5	0A-0	C	A	8	E9	2C	50	A8	5C	E9
EH	.0	5	0A-0	C	A	8	E9	0A	50	A8	5C	E9
UH3	.0	5	0A-0	C	A	8	E9	1B	50	A8	5C	E9
LF	.0	5	0A-0	C	A	8	E9	22	50	A8	5C	E9
UH3	.0	5	0A-0	C	A	8	E9	1B	50	A8	5C	E9
O	.0	5	0A-0	C	A	8	E9	11	50	A8	5C	E9
OU	.0	5	0A-0	C	A	8	E9	12	50	A8	5C	E9
U	.0	5	0A-0	C	A	8	E9	16	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9

3. Duration Adjustment

Pho.	D	T	In—S	A	R	E	FF	DP	IS	RE	TA	FF
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
HF	.1	5	0A-0	C	A	8	E9	6C	50	A8	5C	E9
EH	.0	5	0A-0	C	A	8	E9	0A	50	A8	5C	E9
UH3	.2	5	0A-0	C	A	8	E9	9B	50	A8	5C	E9
LF	.0	5	0A-0	C	A	8	E9	22	50	A8	5C	E9
UH3	.2	5	0A-0	C	A	8	E9	9B	50	A8	5C	E9
O	.2	5	0A-0	C	A	8	E9	91	50	A8	5C	E9
OU	.0	5	0A-0	C	A	8	E9	12	50	A8	5C	E9
U	.3	5	0A-0	C	A	8	E9	D6	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9

4. Phoneme and Duration Adjustment

Pho.	D	T	In—S	A	R	E	FF	DP	IS	RE	TA	FF
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
HF	.1	5	0A-0	C	A	8	E9	6C	50	A8	5C	E9
EH1	.1	5	0A-0	C	A	8	E9	4B	50	A8	5C	E9
UH3	.2	5	0A-0	C	A	8	E9	9B	50	A8	5C	E9
LF	.0	5	0A-0	C	A	8	E9	22	50	A8	5C	E9
UH3	.2	5	0A-0	C	A	8	E9	9B	50	A8	5C	E9
O	.2	5	0A-0	C	A	8	E9	91	50	A8	5C	E9
OU	.0	5	0A-0	C	A	8	E9	12	50	A8	5C	E9
U	.2	5	0A-0	C	A	8	E9	96	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9

5. Inflection Adjustment

Pho.	D	T	In—S	A	R	E	FF	DP	IS	RE	TA	FF
PA	.0	5	0B-0	C	A	8	E9	00	58	A8	5C	E9
PA	.0	5	0B-0	C	A	8	E9	00	58	A8	5C	E9
HF	.1	5	0A-0	C	A	8	E9	6C	50	A8	5C	E9
EH1	.1	5	08-0	C	A	8	E9	4B	40	A8	5C	E9
UH3	.2	5	09-0	C	A	8	E9	9B	48	A8	5C	E9
LF	.0	5	08-0	C	A	8	E9	22	40	A8	5C	E9
UH3	.2	5	05-0	C	A	8	E9	9B	28	A8	5C	E9
O	.2	5	05-0	C	A	8	E9	91	28	A8	5C	E9
OU	.0	5	06-0	C	A	8	E9	12	30	A8	5C	E9
U	.2	5	07-0	C	A	8	E9	96	38	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9
PA	.0	5	0B-0	C	A	8	E9	00	58	A8	5C	E9

6. Phoneme, Duration, Inflection, and Rate Adjustment

Pho.	D	T	In—S	A	R	E	FF	DP	IS	RE	TA	FF
PA	.0	5	0B-0	C	A	8	E9	00	58	A8	5C	E9
PA	.0	5	0B-0	C	A	8	E9	00	58	A8	5C	E9
HF	.1	5	0A-0	C	7	8	E9	6C	50	78	5C	E9
EH1	.1	5	08-0	C	D	8	E9	4B	40	D8	5C	E9
UH3	.2	5	09-0	C	C	8	E9	9B	48	C8	5C	E9
LF	.0	5	08-0	C	C	8	E9	22	40	C8	5C	E9
UH3	.2	5	05-0	C	9	8	E9	9B	28	98	5C	E9
O	.2	5	05-0	C	9	8	E9	91	28	98	5C	E9
OU	.0	5	06-0	C	A	8	E9	12	30	A8	5C	E9
U	.2	5	07-0	C	C	8	E9	96	38	C8	5C	E9
U	.3	5	0A-0	C	7	8	E9	D6	50	78	5C	E9
PA	.0	5	0B-0	C	A	8	E9	00	58	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9

7. Phoneme, Duration, Inflection, Rate, and Amplitude Adjustment

Pho.	D	T	In—S	A	R	E	FF	DP	IS	RE	TA	FF
PA	.0	5	0B-0	C	A	8	E9	00	58	A8	5C	E9
PA	.0	5	0B-0	C	A	8	E9	00	58	A8	5C	E9
EH	.0	5	07-0	0	D	8	E9	0A	38	D8	50	E9
HF	.1	5	0A-0	4	7	8	E9	6C	50	78	54	E9
EH1	.1	5	08-0	C	D	8	E9	4B	40	D8	5C	E9
UH3	.2	5	09-0	A	C	8	E9	9B	48	C8	5A	E9
LF	.0	5	08-0	A	C	8	E9	22	40	C8	5A	E9
UH3	.2	5	05-0	C	9	8	E9	9B	28	98	5C	E9
O	.2	5	05-0	C	9	8	E9	91	28	98	5C	E9
OU	.0	5	06-0	C	A	8	E9	12	30	A8	5C	E9
U	.2	5	07-0	A	C	8	E9	96	38	C8	5A	E9
U	.3	5	0A-0	0	7	8	E9	D6	50	78	50	E9
PA	.0	5	0B-0	C	A	8	E9	00	58	A8	5C	E9
PA	.0	5	0A-0	C	A	8	E9	00	50	A8	5C	E9

8. Further Adjustment (depending on personal preference)

Pho.	D	T	In—S	A	R	E	FF	DP	IS	RE	TA	FF
PA	.0	5	0D-0	C	A	8	E9	00	68	A8	5C	E9
PA	.0	5	0D-0	C	A	8	E9	00	68	A8	5C	E9
EH	.0	5	0D-0	0	D	8	E9	0A	68	D8	50	E9
HF	.1	5	07-0	2	8	8	E9	6C	38	88	52	E9
EH1	.1	5	09-2	C	D	8	E9	4B	4A	D8	5C	E9
UH3	.2	5	09-4	A	C	8	E9	9B	4C	C8	5A	E9
LF	.0	5	09-0	A	C	8	E9	22	48	C8	5A	E9
UH3	.2	5	07-7	C	9	8	E9	9B	3F	98	5C	E9
O	.2	5	06-4	C	9	8	E9	91	34	98	5C	E9
OU	.1	5	05-2	C	A	8	E9	52	2A	A8	5C	E9
U	.2	5	06-3	3	5	8	E9	96	33	58	53	E9
U	.3	5	07-4	0	C	8	E9	D6	3C	C8	50	E9
PA	.0	5	05-4	C	C	8	E9	00	2C	C8	5C	E9
PA	.0	5	01-4	C	C	8	E9	00	0C	C8	5C	E9

silicon systems™
INNOVATORS IN INTEGRATION

SSI 80C50
CMOS Digital IC
T-1 Transmitter

Data Sheet

DESCRIPTION

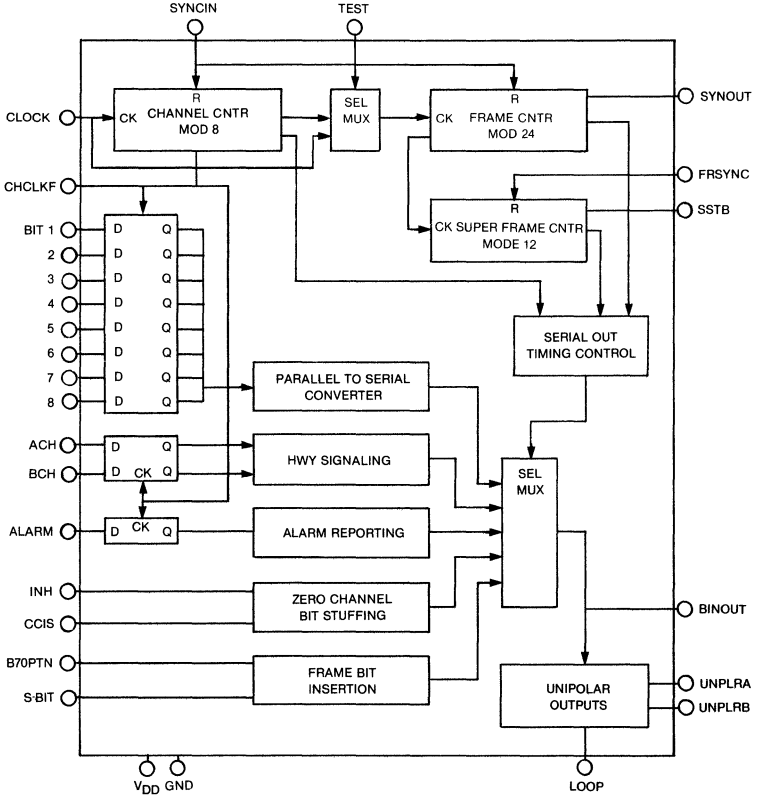
The SSI 80C50 is a CMOS digital IC that provides all the formatting to T-1, D2 or T-1, D3 specifications. The IC is functionally identical and pin compatible with the Rockwell R8050, but offers reduced power consumption and provides greater output current drive (fully TTL). The data rate is 1.544 MHz.

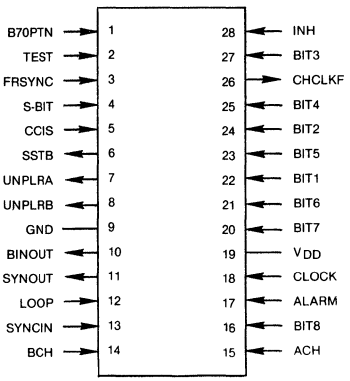
The IC performs 8-bit parallel to serial conversion — channel data is received and then serially transmitted in two formats: binary and as a pair of unipolar outputs. Inputs control the formatting features available — alarm reporting, highway signalling, zero data suppression, and framing. Several timing signal outputs are provided to indicate channel, frame, and multiframe boundaries.

FEATURES

- **Second source, Rockwell R8050**
- **TTL compatible**
- **CMOS low power dissipation**
- **Single 5V supply**
- **Provides formatting, timing and control for T-1, D2 or T1, D3**
- **Provides timing signals to synchronize channel and framing data**

SSI 80C50 Block Diagram





Pin Out
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

Pin Description

Pin No.	Name	Description
1	B70PTN	Provides bit 7 as an alternate bit position for "1" stuffing
2	TEST	Used only for device testing, otherwise this pin should be grounded or open (on chip pulldown resistor to ground). In test mode (TEST = 1) the bit/channel counters count 13, not 193 bits per frame — shortening test throughout time.
3	FRSYNC	Frame sync allows external synchronization of the transmitter's frame counter. When FRSYNC becomes "1", the frame counter is set to frame 1. If FRSYNC is held high and does not return to "0" before the rising edge of CLOCK, BINOUT will "1" and UNPLRA & UNPLRB will toggle each CLOCK cycle.
4	S-BIT	In conjunction with CCIS, provides an alternate way to control the multiframe signalling bit (FS) transmission. The S-BIT input is transmitted at the multiframe signalling bit (FS) if CCIS is "1".
5	CCIS	Common Channel Interoffice Signalling strap. Provides optional control for replacing the automatic FS bit pattern with a 4-kilobit common channel signalling path. When CCIS is high, the S-BIT input replaces the FS pattern and the insertion of ACH and BCH is suspended. The CCIS input may also be used to provide the alternate method of alarm reporting.
6	SSTB	4kHz multiframe strobe. SSTB is the least significant bit of the frame counter. Unless it is directly set by FRSYNC, SSTB will be "1" as each FT bit is serially transmitted, and will be "0" as each multiframe alignment signal FS is transmited.
7 8	UNPLRA UNPLRB	Serial data unipolar outputs. Two paired unipolar outputs are provided for the purpose of creating a single serial data transmission in bipolar format.
9	GROUND	Ground
10	BINOUT	Serial data output, binary formatted.
11	SYNOUT	Channel sync output. Provides a means to synchronize to the internal bit/channel (mod 193) counters. SYNOUT is high one bit time, beginning just prior to the first data bit of a frame being serially transmitted. SYNOUT is the only output determined by the falling edge of CLOCK.
12	LOOP	Loop strap. Intended Used for user testing, otherwise this pin should be grounded or open (on chip pulldown resistor to ground). When enabled to "1", LOOP forces the unipolar outputs to transmit, alternating ones and zeros, regardless of input conditions, while BINOUT still provides normal data outputs.
13	SYNCIN	SYNCIN allows external sychronization of the bit/channel counters (modulo 193). When SYNCIN becomes "1", the counters are set to the state corresponding to the output of the framing (FT or FS) bit. The first bit of channel one will be output on BINOUT (and UNPLRA or UNPLRB) as a result of the first rising edge of CLOCK following the return of SYNCIN to "0".
14	BCH	"B" channel highway signalling allows the user to transmit one bit of signalling per channel data sample in frame 12 only.
15	ACH	"A" channel highway signalling allows the user to transmit one bit of signalling per channel data sample in frame 6 only.
16 20-25 27	BITS 1-8	Bit 1, the sign bit, will be serially transmitted first, followed by bits 2 through 8. The falling edge of CHCLKF indicates input channel data has been clocked into the input register and always occurs during the final bit (bit 8) of each sample.
17	ALARM	Used for reporting alarm conditions. If the ALARM signal is "1", bit 2 of every channel is transmitted as "0".
18	CLOCK	1.544MHz clock.
19	VDD	Power.
26	CHCLKF	Channel clock false. The falling edge of CHCLKF, occurring as bit 8 of any channel is being serially transmitted, indicates input data has been clocked into the input register. With the exception of an extra bit period extending the low level duration at frame bit time, CHCLKF is a divide-by-eight of CLOCK.
28	INH	Inhibit zero channel monitor.

Counters —
Channel data (BIT1-BIT8) is parallel loaded into an input register and is then serially transmitted out at BINOUT at the clock rate of 1.544 MHz. Bit1 is the sign bit, bit 2 the MSB and bit 8 the LSB. When the last bit (bit 8) is being transmitted, the next channel is loaded into the register, latched by CHCLKF. Three counters control the transmission of data. The bit counter (modulo 8) decodes which bit is being transmitted, generates CHCLKF, and increments the channel counter at the end of each channel. The channel counter (modulo 24) outputs a pulse for frame synchronization which is one clock period wide (SYNOUT), and increments the frame counter. The frame counter (modulo 12) signals odd or even frames (SSTB). External synchronization is available with pins SYNCIN, which initializes the bit and channel counters, and FRSYNC which initializes the frame counter.

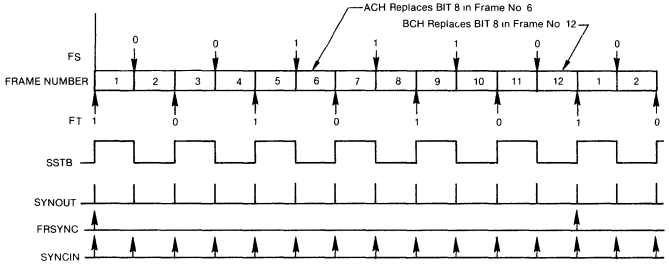
Transmit Ouputs —
The device provides two types of transmit formats a binary ouput (BINOUT) and a pair of unipolar outputs (UNPLRA and UNPLRB). BINOUT is the binary formatted serial conversion of the parallel input channel data. The unipolar outputs toggle for each "1" to be serially transmitted, and are complements of each other. For example, if the current BINOUT is "1", UNPLRA is "1" and UNPLRB is "O", the next output of "1" on BINOUT will toggle UNPLRA to "O" and UNPLRB to "1". Whenever BINOUT is "O", both unipolar outputs are forced to "O".

Alarm reporting and Signalling —
The device provides control for alarm reporting and highway signalling with inputs ALARM, ACH and BCH — all three are latched in by CHCLKF. In remote alarm signalling bit2 of every channel is transmitted as "O". Alternate remote alarm signalling may be used with signals CCIS and S-BIT. In highway signalling ACH replaces bit 8 of every channel in frame 6 only; likewise BCH replaces bit 8 in frame 12.

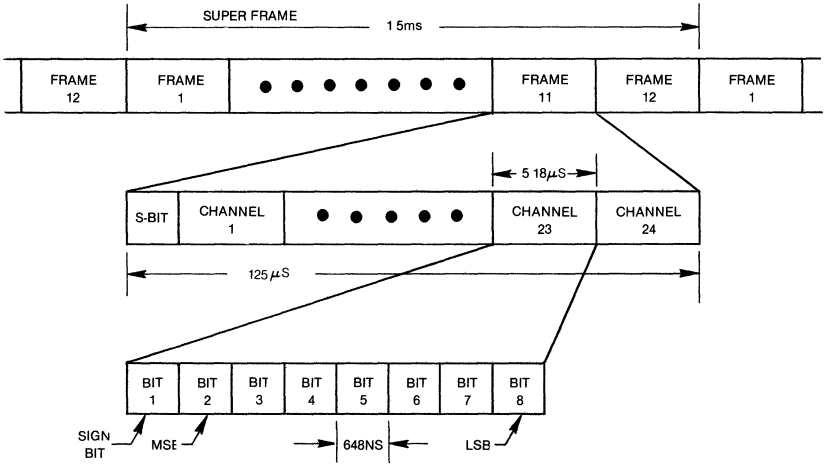
Bit Stuffing —
The device provides for automatic bit stuffing for all zero channel samples. Input INH inhibits the zero channel monitor (zcm) while input B70PTN controls whether bit 7 or bit 8 is stuffed. If INH is high, bits 7 and 8 are transmitted as normal, i.e., bits 7 and 8 are transmitted as received unless the frame is a signalling frame (6 or 12) — in which case the highway signalls replace bit 8 as previously described. If INH is low, the zcm is enabled and the following applies. For signalling frames, if the first seven channel bits and the signalling highway are all "O", bit 7 will be forced to "1". For the other frames, if all the channel bits are "O", then bit 7 will be "1" if B70PTN is "1", otherwise bit 8 will be forced to "1" if B70PTN is "0".

MODE		CONTROLS INH	B70PTN	ALARM	CCIS	FRAME #	HIGHWAY SIGNALING A	B	INPUT 8 BITS CHANNEL DATA 1	2	3	4	5	6	7	8	SERIAL BINOUT CHANNEL BIT POSITION 1	2	3	4	5	6	7	8
1) Normal parallel to serial transmission						‡ 6, 12	A	B	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8
						6	A	B	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_1	B_2	B_3	B_4	B_5	B_6	B_7	A
						12	A	B	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B
2) Alarm report (bit 2 of All channels)				ON		‡ 6,12	A	B	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_1	O	B_3	B_4	B_5	B_6	B_7	B_8
				ON		6	A	B	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_1	O	B_3	B_4	B_5	B_6	B_7	A
				ON		12	A	B	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_1	O	B_3	B_4	B_5	B_6	B_7	B
3) Alternate signalling — ignore A & B					ON	1-12	A	B	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8
4) Zero Data Suppression	a) Alternate signalling – ignore A & B	ON			ON	1-12	A	B	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	1
	b) bit 7 option	ON	ON			‡ 6, 12	A	B	O	O	O	O	O	O	O	O	O	O	O	O	O	O	1	O
	c) stuff bit 8	ON				‡ 6, 12	A	B	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	1
	stuff bit 7	ON				6	O	B	O	O	O	O	O	O	O	B_8	O	O	O	O	O	O	1	O
	stuff bit 7	ON				12	A	O	O	O	O	O	O	O	O	B_8	O	O	O	O	O	O	1	O

Framing —
The device automatically inserts frame information at the beginning of each frame. An FT bit is inserted before the sign bit (bit1) of channel 1 in odd frames, stretching the channel to 9 bits, an FS bit likewise is inserted in even frames. Alternatively, the FS bit insertion can be externally controlled by pins CCIS and S-BIT.



FRAME NUMBER	FT	FS		BIT NUMBERS IN CHANNELS		SIGNALLING CHANNEL
	FRAME ALIGNMENT SIGNAL	MULTIFRAME ALIGNMENT SIGNAL		CHARACTER BITS	SIGNALLING BIT	
		CCIS = 0	CCIS = 1			
1	1			1-8		
2		0	S-BIT	1-8		
3	0			1-8		
4		0	S-BIT	1-8		
5	1			1-8		
6		1	S-BIT	1-7	8	A
7	0			1-8		
8		1	S-BIT	1-8		
9	1			1-8		
10		1	S-BIT	1-8		
11	0			1-8		
12		0	S-BIT	1-7	8	B



T-1 formatting: 8 bits to a channel
24 channels to a frame
12 frames to a super-frame
193 bits to a frame
FT insertion at beginning of odd frames
FS insertion at beginning of even frames

Absolute Maximum Ratings

Positive 5.0 V Supply Voltage, V_{DD} ..... 7 V
Storage Temperature ..... −65 to 150 °C
Lead Temperature (Soldering 10 sec.) ..... 260 °C

Input Pins ..... −0.3V to VDD + 0.3V
Output Pins ..... −0.3 V to V_{DD} + 0.3V or 15 mA

Inputs and outputs are protected against static discharge with industry standard protection devices

Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Unit
IDD	V_{DD} Supply Current	Clock active, Ouputs open, Inputs to rail	—	10	mA
—	CLOCK Frequency	—	10	1600	kHz
VDD	V_{DD}	—	4.75	5.25	V
—	Temperature	—	O	70	°C

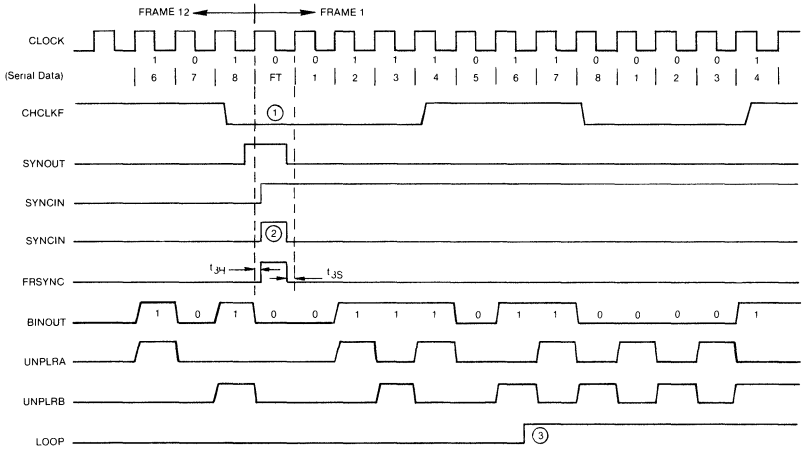
DC Requirements

VIH	Input Hi Voltage	—	2.0	—	V
VIL	Input Lo Voltage	—	—	0.8	V
VOH	Output Hi Voltage	Isource = −1.0mA	2.4	—	V
VOL	Output Lo Voltage	Isync = 2.0mA	—	0.4	V

Timing Characteristics

t1s	Latched Setup Time	(1)	20	—	ns
t1h	Latched Hold Time	(1)	250	—	ns
t2s	Setup Time	(2)	350	—	ns
t2h	Hold Time	(2)	20	—	ns
t3s	Setup Time	(3)	200	—	ns
t3h	Hold Time	(3)	20	—	ns
t3pw	Pulse Width	(3)	100	—	ns
t4s	FRSYNC Setup Time	NRTZ	525	—	ns
t4h	FRSYNC Hold Time	NRTZ	20	—	ns
C	Capacitive Load	Outputs	—	25	pF
tr, tf	Output Rise, Fall Time	50% in, to 90% or 10% out	—	100	ns
td1	Output Prop Delay	(4) From Rising Edge of CLOCK	—	350	ns
td2	SYNOUT Prop Delay	From Falling Edge of CLOCK	—	350	ns

(1) BIT1, BIT2, BIT3, BIT4, BIT5, BIT6, BIT7, BIT8, ACH, BCH, ALARM
(2) S-BIT, CCIS, LOOP, INH, B70PTN
(3) SYNCIN, FRSYNC
(4) BINOUT, UNPLRA, UNPLRB, CHCLKF, SSTB



Notes ① Extended count for frame bit insertion
② Timing for external synchronization of SYNCIN and FRSYNC
③ Loop mode

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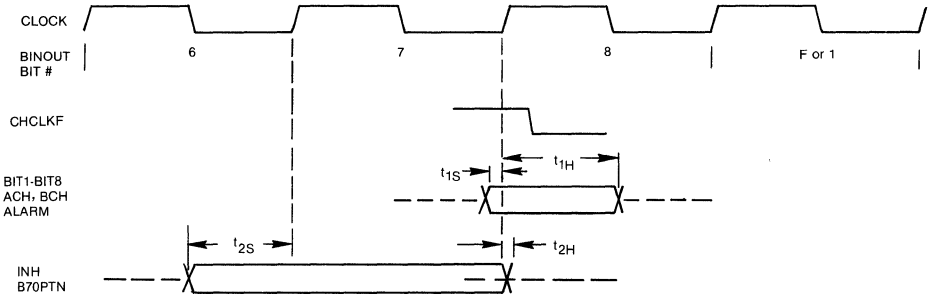
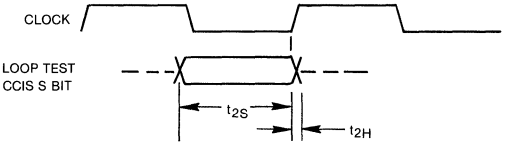
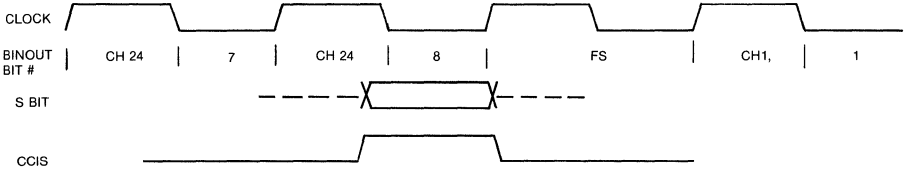
Timing For: BIT1-BIT8, ACH, BCH, ALARM, INH, B70PTN



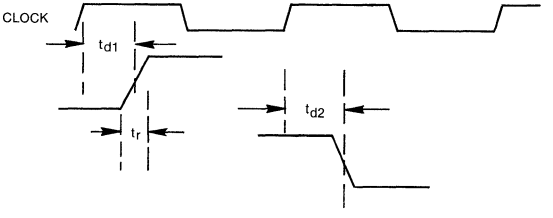
Timing For: Loop, Test, SBIT, CCIS



Timing For: Alternate Remote Alarm Reporting



Output Timing



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SSI 80C60
CMOS Digital IC
T-1 Receiver

Data Sheet

GENERAL DESCRIPTION

The SSI 80C60 is a CMOS digital IC that receives and deserializes serial unipolar data in a T-1, D2 or T-1, D3 format. The IC is functionally identical and pin compatible with the R8060 but offers reduced power consumption and provides greater output current drive (fully TTL).

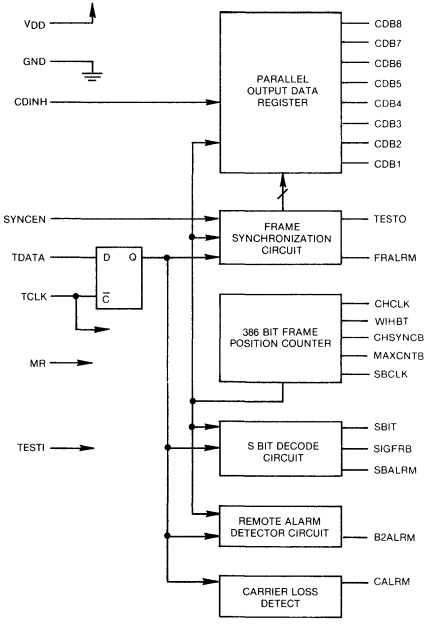
The IC receives 1.544 MBit/s unipolar data and an extracted clock. The data pattern is in 193 bit frames, each frame consisting of a frame bit (FT) or a signaling bit (FS) followed by 192 bits of data representing 24 channels of 8 bit words. F frames and S frames alternate. The receiver synchronizes by locking to (FT) which occurs every 386 bits and which continually alters between 1 and 0, and deserializes the data stream into 24 eight bit wide channels which are clocked out of the 8 data bit pins at a 192,000 channel/s rate with each channel repeated at a 8000 frame/s rate. Signaling bits (FS), which are positioned 193 bits behind the frame bit, are outputed at the SBIT pin.

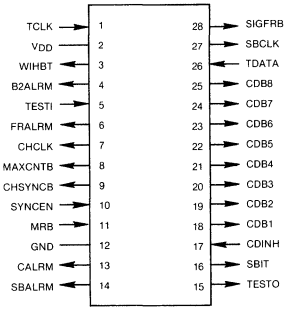
Remote alarm reporting is monitored and an alarm is indicated at the B2ALRM pin if 255 consecutive bit 2 zeros are received. The incoming data is monitored for loss of carrier and an alarm is indicated at the CALRM pin if 31 consecutive zero bits are received.

FEATURES

- **Second source, Rockwell R8060**
- **TTL compatible**
- **CMOS low power dissipation**
- **Single 5V supply**
- **Locks onto and deserializes incoming T-1, D2 and T-1, D3 data in 5ms**
- **Generates timing signals to synchronize channel and frame information**
- **Monitors and detects**
  - **— FS bit**
  - **— Frame sync**
  - **— Carrier**
  - **— Remote alarm reporting**

Block Diagram





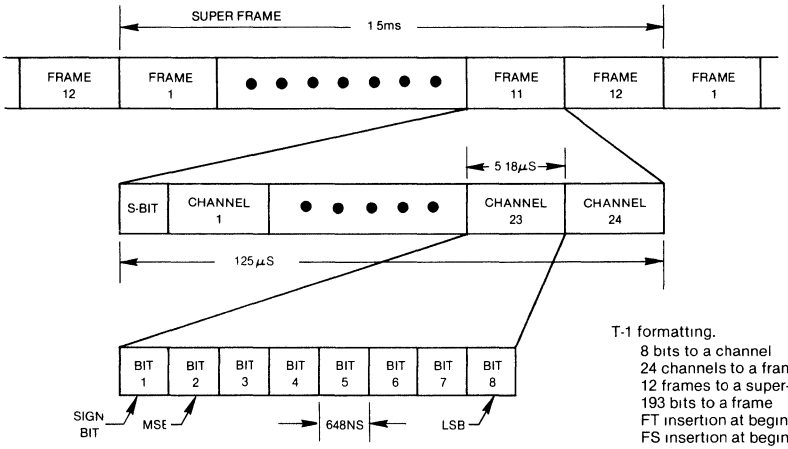
Pin Out
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

Pin	Name	Description
1	TCLK	Data clock. Nominal clock frequency is 1.544 MHz. Data bits are clocked into the chip on the falling edge of the clock.
2	V_{DD}	Power
3	WIHBT	Write inhibit clock. Strobes high once every channel for two TCLK periods and is used to load the 8-bit parallel channel output data into external circuitry.
4	B2ALRM	Bit 2 alarm signal, active high. Goes high indicating a remote alarm when 255 consecutive 0's are received in the bit 2 position. Resets low after bit 2 becomes 1.
5	TESTI	Test input, when low puts the circuit in its test mode. Must be high or left open during normal operation.
6	FRALRM	Frame alarm, active high. Goes high when frame sync is lost.
7	CHCLK	Output data channel clock, going high signals new parallel data output.
8	MAXCNTB	Strobes low once every two frames for one TCLK period during the expected input of FT.
9	CHSYNCB	Channel sync clock, strobes low once every frame for six TCLK periods during channel 1.
10	SYNCEN	Frame synchronization enable. When low, disables the automatic resync search initiated by a frame alarm condition.
11	MRB	Master Reset, active low resets the circuit.
12	GND	Ground
13	CALRM	Carrier alarm signal, active high. Goes high if 31 consecutive zeros are received in the TDATA input. Resets low when TDATA becomes 1.
14	SBALRM	FS alarm signal, active high. Signals an FS alarm when the previous FS bits have been a 0 followed by 1111. SBALRM is reset low when the FS bit pattern 10001 occurs. The SBALRM transition occurs during channel 1 of FS frame.
15	TESTO	Test mode output.
16	SBIT	Signaling bit, outputs the FS received 2 frames before the current FS.
17	CDINH	Channel data inhibit, when high forces CDB1 through CDB7 pins high. CDB8 is not affected.
18-25	CDB1-8	Bit 1, the sign bit, will be serially received first, followed by bits 2 (MSB) through bit 8 (LSB). The rising edge of CHCLK indicates output channel data has been clocked out and occurs as the final bit (bit 8) is received.
26	TDATA	Serial data input.
27	SBCLK	4 kHz signal that is low during even frames and high during odd frames.
28	SIGFRB	Signal frame clock, strobes low during frame 6 and 12.

Timing — Timing signals for channel and frame synchronization.
WIHBT
CHCLK
MAXCNTB
SIGFRB
CHSYNCB
SBCLK
SBIT

Alarms — Alarm conditions reported.
SBALRM
B2ALRM
CALRM
FRALRM



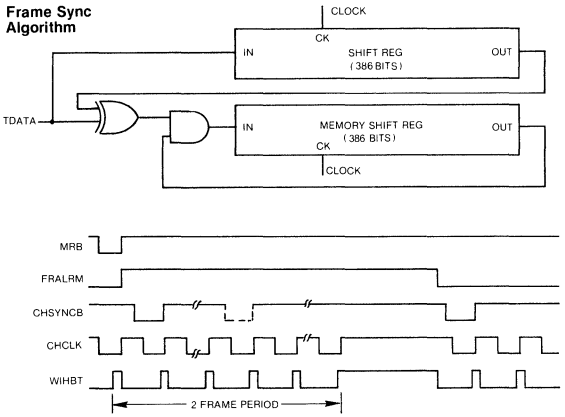
T-1 formatting.
8 bits to a channel
24 channels to a frame
12 frames to a super-frame
193 bits to a frame
FT insertion at beginning of odd frames
FS insertion at beginning of even frames

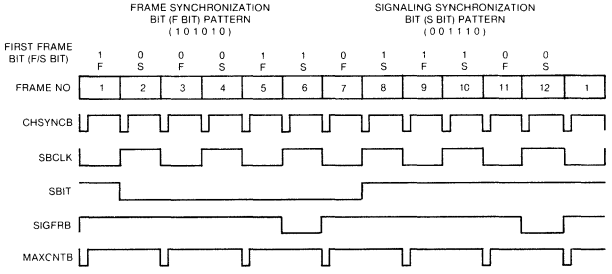
FRAME ALARM

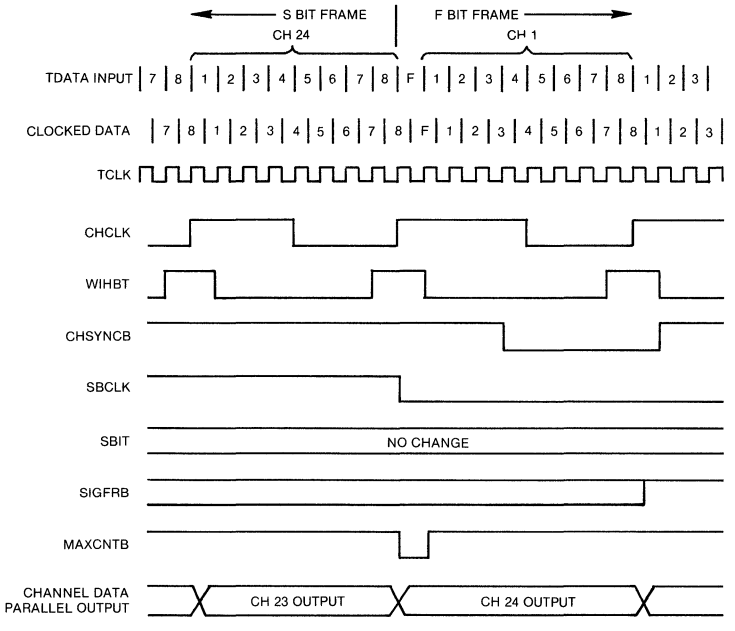
FRALRM goes high indicating an out-of-frame condition when:
(1) The frame sinchronization algorithm is in progress.
(2) MRB is low.
(3) The current FT is in error and a previous FT error occurred in the past four frames.
(4) CALRM is low.

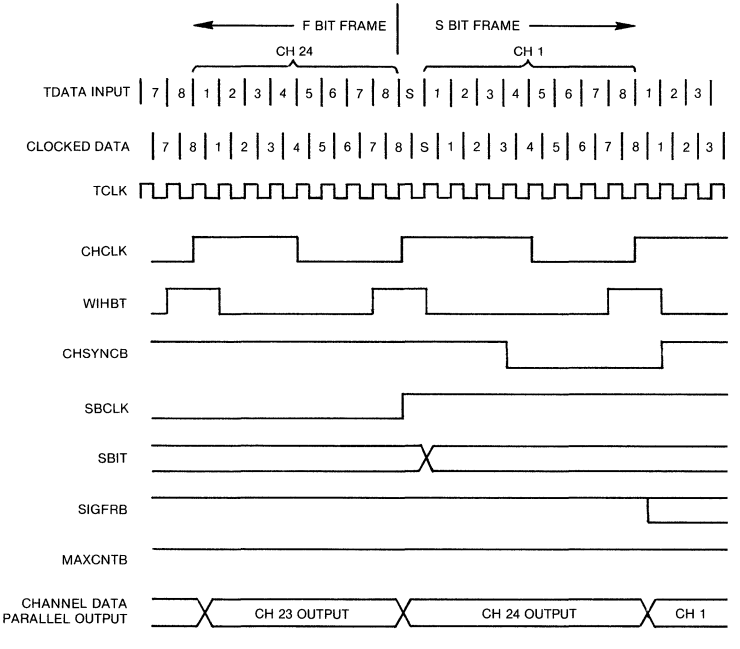
FRALRM returns low when:
(1) Frame synchronization is complete.
(2) CALRM is high.

During frame sync output signals CHCLK, CHSYNC, and WIHBT will continue normally for 2 frame periods — afterwards they will be high. For most data patterns frame sync requires less than 5 milliseconds to acquire frame lock.






S BIT FRAME
F BIT FRAME
CH 24
CH 1
TDATA INPUT
CLOCKED DATA
TCLK
CHCLK
WIHBT
CHSYNCB
SBCLK
SBIT
NO CHANGE
SIGFRB
MAXCNTB
CHANNEL DATA PARALLEL OUTPUT
CH 23 OUTPUT
CH 24 OUTPUT


F BIT FRAME
S BIT FRAME
CH 24
CH 1
TDATA INPUT
CLOCKED DATA
TCLK
CHCLK
WIHBT
CHSYNCB
SBCLK
SBIT
SIGFRB
MAXCNTB
CHANNEL DATA PARALLEL OUTPUT
CH 23 OUTPUT
CH 24 OUTPUT
CH 1

Absolute Maximum Ratings

Positive 5.0V Supply Voltage, VCC 7V
Storage Temperature . . . . . – 65 to 150 °C
Lead Temperature (Soldering 10 sec.) . . . . . 260 °C
Input Pins . . . . . – 0.3V to VDD + 0.3V
Output Pins . . . . . – 0.3V to VDD + 0.3V or 15 mA

Inputs and outputs are protected against static discharge with industry standard protection devices

Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Unit
IDD	VDD Supply Current	Clock active, Outputs open, Inputs to rail	—	5	mA
—	CLOCK Frequency	—	10	1600	kHz
VDD	VDD	—	4.5	5.5	V
—	Ambient Temperature	—	0	70	°C

DC Requirements

Symbol	Parameter	Test Conditions	Min	Max	Unit
VIH	Input Hi Voltage	—	2.0	—	V
VIL	Input Lo Voltage	—	—	0.8	V
VOH	Output Hi Voltage	I source = – 1.0mA	2.4	—	V
VOL	Output Lo Voltage	I sink = 2.0mA	—	0.4	V

Timing Requirements

Symbol	Parameter	Test Conditions	Min	Max	Unit
t1s	TDATA setup time	from CLOCK edge falling	100	—	ns
t1h	TDATA hold time	from CLOCK edge falling	100	—	ns
t2h	Setup time	(1) from WIHBT edge rising	0	—	ns
t3h	CDB1-8 hold time	from CHCLK edge rising	0	200	ns
td1	Output delay	(2) from CLOCK edge rising	—	300	ns
—	Output delay	(3) from CLOCK edge rising	—	400	ns
—	CALRM delay	from CLOCK edge	—	300	ns
—	FRALRM delay	from CLOCK edge	—	600	ns
tr, tf	Output rise, fall time	90% to 10%	—	100	ns
—	SYNCEN low (inhibit sync)	before FRALRM edge rising	200	—	ns
—	SYNCEN high (initiate sync)	before MRB edge rising	200	—	ns
—	CDB1-7 valid/high	after CDINH edge falling/rising	—	150	ns
—	FRALRM high	after MRB falling edge	—	250	ns

(1) SIGFRM, FRALRM
(2) CHCLK, CHSYNC, WIHBT, MAXCNTB, SBCLK
(3) SIGFRM, SBALRM, B2ALRM, SBIT, CDB1-8

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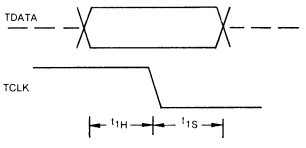
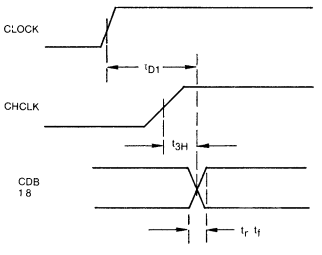
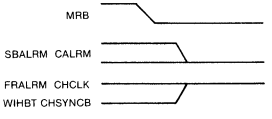
INPUT TIMING



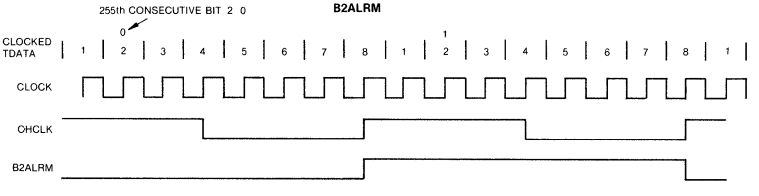
OUTPUT TIMING



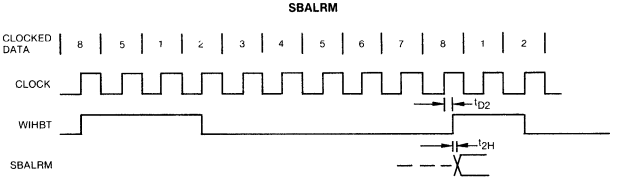
MRB



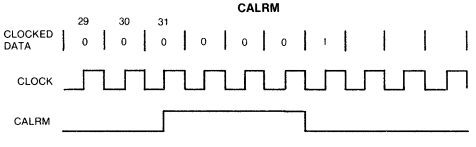
B2ALRM



SBALRM



CALRM



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SSI 22100 CMOS 4x4 Crosspoint Switch with Control Memory

Data Sheet

GENERAL DESCRIPTION

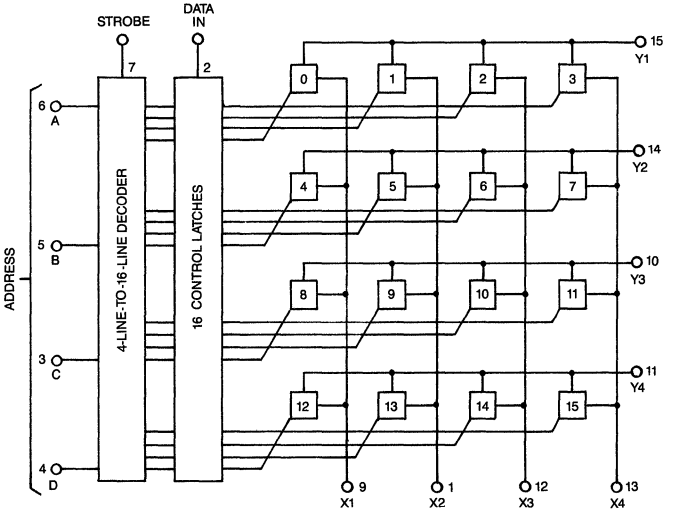
The SSI 22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line-to-16 decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned ON or OFF by applying a logical ONE or ZERO respectively to DATA IN and strobing the STROBE input to a logical ONE. Any number of the transmission gates can be ON simultaneously. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned OFF by setting the STROBE high and DATA IN low, then addressing all switches in succession.

The SSI 22100 is supplied in 16-lead hermetic dual-in-line ceramic packages and 16-lead dual-in-line plastic packages.

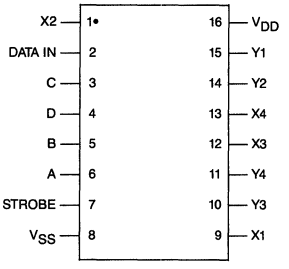
FEATURES

- **Low ON resistance—75Ω typ. at V_{DD} = 12V**
- **"Built-In" control latches**
- **Large analog signal capability—$\pm V_{DD}/2$**
- **10-MHz switch bandwidth**
- **Matched switch characteristics—ΔR_{ON} = 18Ω typ. at V_{DD} = 12V**
- **High linearity—0.5% distortion (typ.) at f = 1kHz, $V_{IN} = 5V_{p-p}$, V_{DD} = 10V, and R_L = 1kΩ**
- **Standard CMOS noise immunity**
- **100% tested for maximum quiescent current at 20V**
- **Second source for RCA CD22100**

SSI 22100 Block Diagram



PIN CONFIGURATION



Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

PIN DESCRIPTION

Pin No.	Symbol	Description
9, 1, 2, 3	X_1 to X_4	Transmission lines in X direction
2	DATA IN	Data input. The selected crosspoints can be turned on or off by applying a logical ONE or ZERO, respectively, to the data input and a logical ONE to the STROBE.
6, 5, 3, 4	A, B, C, D	Address inputs
7	STROBE	STROBE input
8	V_{SS}	Ground
15,14,10,11	Y_1 to Y_4	Transmission lines in Y direction
16	V_{DD}	Positive Power Supply

Maximum Ratings, Absolute-Maximum Values:

DC supply-voltage range, (V_{DD})
(Voltages referenced to V_{SS} Terminal . . . −0.5 to +20 V
Input voltage range, all inputs . . . . . −0.5 to V_{DD} +0.5 V
DC input current, any one input* . . . . . ±10 mA
Power dissipation per package (P_D):
For T_A = −40 to +60 °C (package type P) . . . . . 500 mW
For T_A = +60 to +85 °C (package type P)
Derate Linearly at 12 mW/°C to 200mW
For T_A = −55 to +100 °C (package types D) . . . 500mW
For T_A = +100 to +125 °C (package types D)
Derate Linearly at 12 mW °/C to 200 mW
Device dissipation per transmission gate
For T_A = full package-temperature range
(all package types) 100mW

Maximum Ratings, Absolute-Maximum Values: (cont.)

Operating-temperature range (T_A):
Package type D . . . . . −55 to +125 °C
Package type P . . . . . −40 to +85 °C
Storage temperature range (T_{stg}) . . . . . −65 to +150 °C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265 °C

*Maximum current through transmission gates (switches) = 25 mA

Recommended Operating Conditions
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

Characteristic	MIN.	MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

TRUTH TABLE

Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

Dynamic Electrical Characteristics at T_A = 25°C

Characteristic	Conditions				Limits			Units
	f_{is} kHz	R_L kΩ	V_{is}• (V)	V_{DD} (V)	Min.	Typ.	Max.	
Crosspoints								
Propagation Delay Time, (Switch ON) Signal Input to Output, t_{PHL}, t_{PLH}	—	10	5	5	—	30	60	ns
			10	10	—	15	30	
			15	15	—	10	20	
	C_L = 50 pF; t_r, t_f = 20 ns							
Frequency Response, (Any Switch ON)	1	1	5	10	—	40	—	MHz
	Sine wave input, $20 \log \frac{V_{OS}}{V_{is}}$ = -3 dB							
Sine Wave Response, (Distortion)	1	1	5	10	—	0.5	—	%
Feedthrough (All Switches OFF)	1.6	1	5	10	—	-80	—	dB
	Sine wave input							

• Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$

Dynamic Electrical Characteristics at T_A = 25°C (cont.)

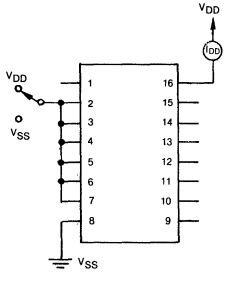
Characteristic	Conditions				Limits			Units
	f_{is} kHz	R_L kΩ	V_{is}* (V)	V_{DD} (V)	Min.	Typ.	Max.	
Crosspoints (cont'd)								
Frequency for Signal Crosstalk	—	1	10	10				
Attenuation of 40 dB	Sine wave input				—	1.5	—	MHz
Attenuation of 110 dB						0.1		kHz
Capacitance,								
X_n to Ground		—	—	5-15	—	18	—	
X_n to Ground		—	—	5-15	—	30	—	pF
Feedthrough		—	—	—	—	0.4	—	
Controls								
Propagation Delay Time:								
Strobe to Output, t_{PZH}	$R_L = 1k\Omega$			5	—	300	600	
(Switch Turn-ON to High Level)	$C_L = 50pF$,			10	—	125	250	
	$t_r, t_f = 20$ ns			15	—	80	160	
Data-In to Output, t_{PZH}				5	—	110	220	
(Turn-On to High Level)				10	—	40	80	ns
				15	—	25	50	
Address to Output, t_{PZH}				5	—	350	700	
(Turn-ON to High Level)				10	—	135	270	
				15	—	90	180	
Propagation Delay Time:				5	—	165	330	
Strobe to Output, t_{PHZ}				10	—	85	170	
(Switch Turn-OFF)				15	—	70	140	
Data-In to Output, t_{PZL}				5	—	210	420	
(Turn-ON to Low Level)				10	—	110	220	ns
				15	—	100	200	
Address to Output, t_{PHZ}				5	—	435	870	
(Turn-OFF)				10	—	210	420	
				15	—	160	320	
Minimum Setup Time,				5	—	95	190	
Data-In to Strobe, Address, t_{SU}				10	—	25	50	ns
				15	—	15	30	
Minimum Hold Time,				5	—	180	360	
Data-In to Strobe, Address, t_H				10	—	110	220	ns
				15	—	35	70	
Maximum Switching Frequency, f_0	$R_L = 1k\Omega$, $C_L = 50pF$			5	0.6	1.2	—	
				10	1.6	3.2	—	MHz
	$t_r, t_f = 20$ ns			15	2.5	5	—	
Minimum Strobe Pulse Width, t_W				5	—	300	600	
				10	—	120	240	ns
				15	—	90	180	
Control Crosstalk,	—	10	10	10	—	75	—	mV
Data-In, Address, or Strobe to Output	Square wave input $t_r, t_f = 20$ ns							(peak)
Input Capacitance, C_{IN}	Any Control Input			—	—	5	7.5	pF

*Peak-to-peak voltage symmetrical about $V_{DD}/2$

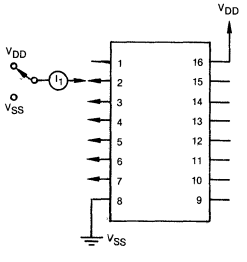
Static Electrical Characteristics

Characteristic	Conditions	V_{IN} (V)	V_{DD} (V)	Limits at Indicated Temperature (°C)†							Units
				−55 Max.	−40 Max.	+25 Min.	+25 Typ.	+25 Max.	+85 Max.	+125 Max.	
Crosspoints											
Quiescent Device Current, I_{DD} Max.		—	5	5	5	—	0.04	5	150	150	μA
		—	10	10	10	—	0.04	10	300	300	
		—	15	20	20	—	0.04	20	600	600	
		—	20	100	100	—	0.08	100	3000	3000	
ON Resistance R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	—	5	475	500	—	225	600	725	800	Ω
		—	10	135	145	—	85	180	205	230	
		—	12	100	110	—	75	135	155	175	
		—	15	70	75	—	65	95	110	125	
ΔON Resistance ΔR_{ON}	Between any two switches	—	5	—	—	—	25	—	—	—	Ω
		—	10	—	—	—	10	—	—	—	
		—	12	—	—	—	8	—	—	—	
		—	15	—	—	—	5	—	—	—	
OFF Switch Leakage Current I_L Max.	All switches OFF	0,18	18	±100		—	±1	±100*	±1000		nA
Controls											
Input Low Voltage V_{IL} Max.	OFF Switch $I_L < 0.2\,\mu A$	—	5	1.5		—	—	1.5	1.5		V
		—	10	3		—	—	3	3		
		—	15	4		—	—	4	4		
Input High Voltage, V_{IH} Min.	ON switch see R_{ON} characteristic	—	5	3.5		3.5	—	—	3.5		
		—	10	7		7	—	—	7		
		—	15	11		11	—	—	11		
Input Current, I_{IN} Max.	Any control	0,18	18	±0.1		—	$\pm 10^{-5}$	±0.1	±1		μA

*Determined by minimum feasible leakage measurements for automatic testing
†Values at −55, +25, +125, apply to D package Values at −40, +25, +85, apply to P package

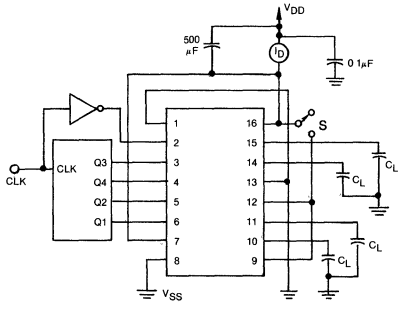


Quiescent current test circuit



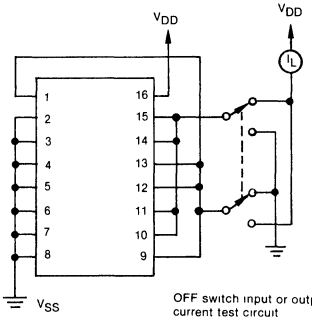
Input current test circuit

Note
Measure inputs sequentially to both V_{DD} and V_{SS} Connect all unused inputs to either V_{DD} or V_{SS}.

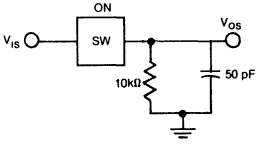


Note Close switch S after applying V_{DD}

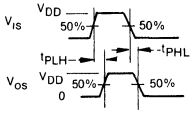
Dynamic power dissipation test circuit



OFF switch input or output leakage current test circuit

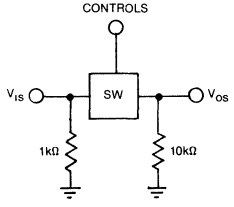


SW = ANY CROSSPOINT

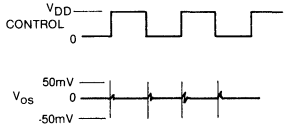


STROBE = DATA-IN = V_{DD}

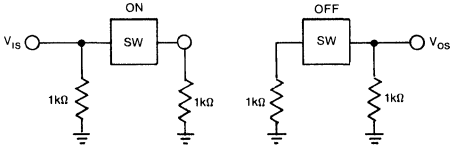
Propagation delay time test circuit and waveforms (signal input to signal output, switch ON)



SW = ANY CROSSPOINT

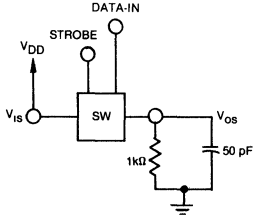


Test circuit and waveforms for crosstalk (control input to signal output)

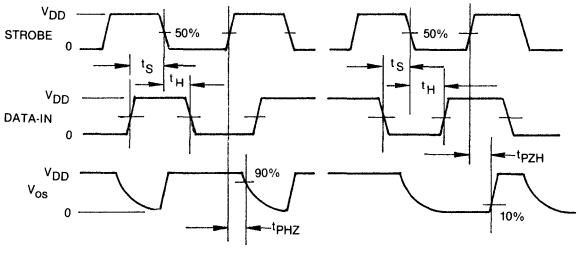


SW = ANY CROSSPOINT

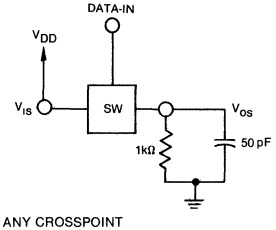
Test circuit for crosstalk between switch circuits in the same package



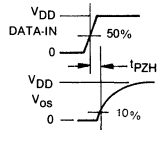
SW = ANY CROSSPOINT

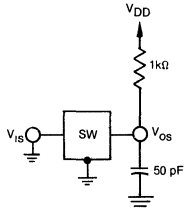


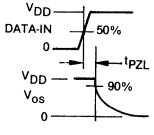
Propagation delay time test circuit and waveforms (STROBE to signal output, switch Turn-ON or Turn-OFF)



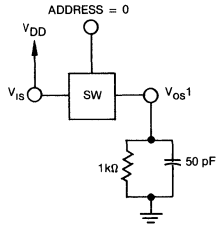
SW = ANY CROSSPOINT
STROBE = V_{DD}

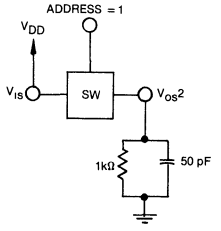




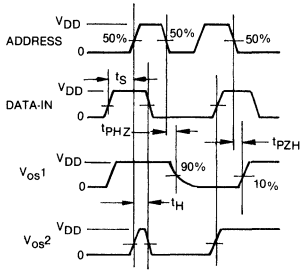


Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level)





SW = ANY CROSSPOINT
STROBE = V_{DD}



Propagation delay time test circuit and waveforms (address to signal output, switch Turn-ON or Turn-OFF)

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SSI 22101/22102 CMOS 4x4x2 Crosspoint Switches with Control Memory

Data Sheet

GENERAL DESCRIPTION

The SSI 22101 and 22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates), 4-line to 16-line decoders, and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, and any number of crosspoints can be ON simultaneously. Corresponding crosspoints in each array are turned on and off simultaneously, also.

In the SSI 22101, the selected crosspoint pair can be turned on or off by applying a logical ONE or ZERO, respectively, to the DATA input, and applying a ONE to the STROBE input. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the STROBE high, DATA low, and then addressing all switches in succession.

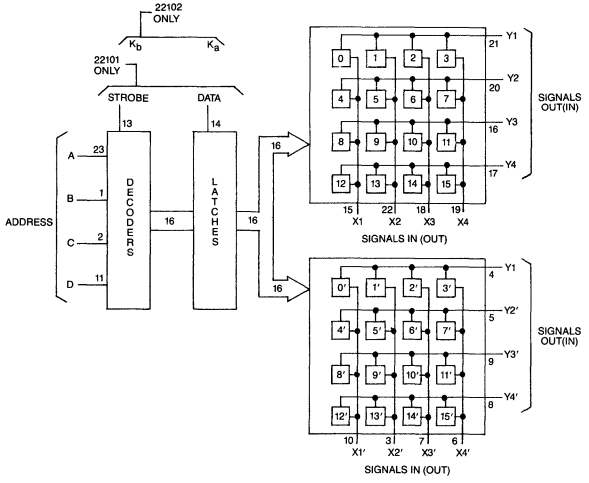
The selected pair of crosspoints in the SSI 22102 is turned on by applying a logical ONE to the K_a (set) input while a logical ZERO is on the K_b input, and turned off by applying a logical ONE to the K_b (reset) input while a logical ZERO is on the K_a input. In this respect, the control latches of the SSI 22102 are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONEs to the K_a and K_b inputs turns off (resets) all crosspoints. All crosspoints in both devices must be turned off as V_{DD} is applied.

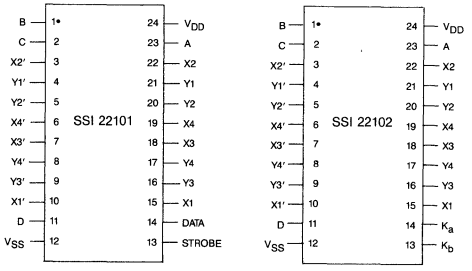
The SSI 22101 and SSI 22102 are supplied in 24-lead hermetic dual-in-line ceramic packages and 24-lead dual-in-line plastic packages.

FEATURES

- **Low ON resistance—75Ω typ. at V_{DD} = 12V**
- **"Built-In" latched inputs**
- **Large analog signal capability—$\pm V_{DD}/2$**
- **10-MHz switch bandwidth**
- **Matched switch characteristics—ΔR_{ON} = 8Ω typ. at V_{DD} = 12V**
- **High linearity—0.25% distortion (typ.) at f = 1kHz, $V_{IN} = 5V_{p-p}$, $V_{DD} - V_{SS}$ = 10V, and R_l = 1kΩ**
- **Standard CMOS noise immunity**
- **Second source for RCA CD22101 & CD22102**

Block Diagram SSI 22101/22102





Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

PIN DESCRIPTION

Pin No.	Symbol	Description
23,1, 2,11	A—D	Address line inputs
10,3, 7,6,	X1'-X4'	Input transmission lines to be paired with Y1'-Y4'.
4,5,9, 8,	Y1'-Y4'	Output transmission lines to be paired with X1'-X4'.
12	Vss	Ground
13	STROBE (220101 only)	Strope input. A logical "one" of STROBE will turn on or off the specified switches when DATA is ONE or ZERO respectively.
14	DATA (22101 only)	Data input
14,13	Ka, Kb (22102 only)	Switch control inputs. When Ka = 1 and Kb = 0, the selected switches are turned on. When Ka = 0 and Kb = 1, the selected switches are turned off. While Ka = 1 and Kb = 1, all the switches are turned off.
15,22, 18,19	X1-X4	Input transmission lines to be paired with Y1-Y4.
21,20, 16,17	Y1-Y4	Output transmission lines to be paired with X1-X4.
24	V_{DD}	Positive power supply.

Maximum Ratings, Absolute-Maximum Values:

DC supply-voltage range, (V_{DD})
(Voltages referrenced to V_{SS} Terminal ...-0.5 to +20 v
Input voltage range, all inputs .....-0.5 to V_{DD} + 0.5 V
DC input current, any one input* ..... ± 10 mA
Power dissipation per package (P_D):
For T_A = -40 to +60 °C (package type P) .....500 mW
For T_A = +60 to +85 °C (package type P) ..Derate Linearly at 12 mW/ °C to 200mW
For T_A = -55 to +100 °C (package type D) ...500 mW
For T_A = 100 to 125 °C (package type D) .....Derate Linearly at 12 mW °/C to 200 mW
Device dissipation for transmission gate
For T_A = full package-temperature range (all package types) 100mW
Operating-temperature range (T_A):
Package type D .....-55 to +125 °C
Package type P .....-40 to +85 °C
Storage temperature range (T_{stg}) .....-65 to +150 °C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max..... ± 265 °C

*Maximum current through transmission gates (switches) = 25 mA

Recommended Operating Conditions
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

Characteristic	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

Control Truth Table for SSI22101

Function	Address	Strobe	Data	Select
	A B C D			
Switch On	1 1 1 1	1	1	15 (X4Y4) & 15' (X4'Y4')
Switch Off	1 1 1 1	1	0	15 (X4Y4) & 15' (X4'Y4')
No Change	X X X X	0	X	XXX X

1 = High Level; 0 = Low Level, X = Don't Care

Control Truth Table for SSI 22102

Function	Address	K_a	K_b	Select
	A B C D			
Switch On	1 1 1 1	1	0	15 (X4Y4) & 15' (X4'Y4')
Switch Off	1 1 1 1	0	1	15 (X4Y4) & 15' (X4'Y4')
All Switches Off#	X X X X	1	1	ALL
No Change	X X X X	0	0	X X X X

1 = High Level; 0 = Low Level; X = Don't Care
# In the event that K_a and K_b are changed from levels 1,1 to 0,0 K_b should not be allowed to go to 0 before K_a, otherwise a switch which was off will inadvertently be turned on

Decoder Truth Table

Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1 & X1'Y1'	0	0	0	1	X1Y3 & X1'Y3'
1	0	0	0	X2Y1 & X2'Y1'	1	0	0	1	X2Y3 & X2'Y3'
0	1	0	0	X3Y1 & X3'Y1'	0	1	0	1	X3Y3 & X3'Y3'
1	1	0	0	X4Y1 & X4'Y1'	1	1	0	1	X4Y3 & X4'Y3'
0	0	1	0	X1Y2 & X1'Y2'	0	0	1	1	X1Y4 & X1'Y4'
1	0	1	0	X2Y2 & X2'Y2'	1	0	1	1	X2Y4 & X2'Y4'
0	1	1	0	X3Y2 & X3'Y2'	0	1	1	1	X3Y4 & X3'Y4'
1	1	1	0	X4Y2 & X4'Y2'	1	1	1	1	X4Y4 & X4'Y4'

Static Electrical Characteristics

Characteristic	Conditions	Fig.	V_{IS} (V)	V_{DD} (V)	Limits at Indicated Temperature (°C)†							Units
					−55 Max.	−40 Max.	+25 Min.	+25 Typ.	+25 Max.	+85 Max.	+125 Max.	
Crosspoints												
Quiescent Device Current, I_{DD} Max.		1	—	5	5	5	—	0.04	5	150	150	μA
			—	10	10	10	—	0.04	10	300	300	
			—	15	20	20	—	0.04	20	600	600	
			—	20	100	100	—	0.08	100	3000	3000	
ON Resistance R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}		—	5	475	500	—	225	600	725	800	Ω
			—	10	135	145	—	85	180	205	230	
			—	12	100	110	—	75	135	155	175	
			—	15	70	75	—	65	95	110	125	
ΔON Resistance, ΔR_{ON}	Between any two switches		—	5	—	—	—	25	—	—	—	Ω
			—	10	—	—	—	10	—	—	—	
			—	12	—	—	—	8	—	—	—	
			—	15	—	—	—	5	—	—	—	
OFF Leakage Current I_L Max.	All switches OFF	4	0,18	18	±1000		—	±1	±100*	±1000		nA
Controls												
Input Low Voltage V_{IL} Max.	OFF Switch $I_L < 0.2\,\mu A$		—	5	1.5		—	—	1.5	1.5		V
			—	10	3		—	—	3	3		
			—	15	4		—	—	4	4		
Input High Voltage, V_{IH} Min.	ON switch see R_{ON} characteristic		—	5	3.5		3.5	—	—	3.5		
			—	10	7		7	—	—	7		
			—	15	11		11	—	—	11		
Input Current, I_{IN} Max.	Any control	2	0,18	18	±0.1	±0.1	—	$\pm 10^{-5}$	±0.1	±1	±1	μA

*Determined by minimum feasible leakage measurements for automatic testing
†Values at −55, +25, +125, apply to D package Values at −40, +25, +85, apply to P package

Dynamic Electrical Characteristics at T_A = 25°C

Characteristic	Conditions					Limits			Units
	f_{is} kHz	R_L kΩ	V_{is} • (V)	V_{DD} (V)	Fig.	Min.	Typ.	Max.	
Crosspoints									
Propagation Delay Time, (Switch ON) Signal Input to Output, t_{PHL}, t_{PLH}	—	10	5 10 15	5 10 15	5	— — —	30 15 10	60 30 20	ns
	C_L = 50pF; t_r, t_f = 20ns								
Frequency Response, (Any switch ON)	1	1	5	10		—	40	—	MHz
	Sine wave input, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB								
Sine Wave Response, (Distortion)	1 1 1	1 1 1	2.5 5 7.5	5 10 15		— — —	1 0.25 0.15	— — —	%
Feedthrough All Switches OFF (See Fig. 13)	1.6	0.6	2 *	10	13	—	−96	—	dB
	Sine wave input								
Frequency for Signal Crosstalk Attenuation of 40 dB Attenuation of 95 dB (See Fig. 12)	—	0.6	1	10		— —	2.5 0.1	—	MHz kHz
	Sine wave input								
Capacitance, X_n to Ground Y_n to Ground Feedthrough	— — —	— — —	— — —	— — —		— — —	25 60 0.6	— — —	pF
Controls									
Propagation Delay Time, High Impedance to High Level or Low Level, t_{PZH}, t_{PZL} Strobe to Output, SSI 22101	R_L = 1kΩ C_L = 50 pF, t_r, t_f = 20 ns			5 10 15	6	— — —	500 230 170	1000 460 340	ns
Data-In to Output, SSI 22101				5 10 15	7	— — —	515 220 170	1000 440 340	
K_a to Output, SSI 22102				5 10 15		— — —	500 215 160	1000 430 320	
Address to Output, SSI 22101, SSI 22102				5 10 15	8	— — —	480 225 155	960 450 300	
Propagation Delay Time, High Level or Low Level to High Impedance, t_{PHZ}, t_{PLZ} Strobe to Output, SSI 22101				5 10 15	6	— — —	450 200 135	900 400 270	
K_b to Output, SSI 22102				5 10 15		— — —	450 200 130	900 400 260	
Data-In to Output, SSI 22101				5 10 15		— — —	450 165 110	900 330 220	
K_a • K_b to Output, SSI 22102				5 10 15		— — —	280 130 90	560 260 180	

• Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$ unless otherwise specified.

* RMS

Dynamic Electrical Characteristics at T_A = 25°C (cont'd)

Characteristic	Conditions				Limits			Units
	f_{is} kHz	R_L kΩ	V_{DD} (V)	Fig	Min.	Typ.	Max.	
Controls (cont'd)								
Address to Output, SSI 22101, SSI 22102	R_L = 1k, C_L = 50 pF, t_r, t_f = 20ns		5		—	425	850	
			10	8	—	190	380	
			15		—	130	260	
Minimum Strobe Pulse Width t_W SSI 22101			5		—	260	500	
			10		—	120	240	
			15		—	80	160	
Address to Strobe Setup or Hold Times, t_{SU}, t_H, SSI 22101			5		—	−160	0	
			10	9	—	−70	0	
			15		—	−50	0	
Strobe to Data-In Hold Time, Time, t_{hHL}; t_{hLH}, SSI 22101			5		—	200	400	
			10	10	—	80	160	
			15		—	60	120	ns
Address to K_a and K_b Setup or Hold Times, t_{SU}, t_H, SSI 22102			5		—	−160	0	
			10		—	−70	0	
			15		—	−50	0	
Minimum K_a • K_b Pulse Width, t_W SSI 22102			5		—	375	750	
			10		—	160	320	
			15		—	110	220	
Minimum K_a Pulse Width, t_W SSI 22102			5		—	425	850	
			10		—	175	350	
			15		—	120	240	
Minimum K_b Pulse Width, t_W SSI 22102			5		—	200	400	
			10		—	90	180	
			15		—	70	140	
Control Crosstalk, Data-In, Address, or Strobe to Output	100	10	5	11	—	75	—	mV (peak)
	Square wave input = 5V, t_r,t_f = 20ns, R_S = 1kΩ							
Input Capacitance, C_{IN}	Any Control Input		—		—	5	7.5	pF

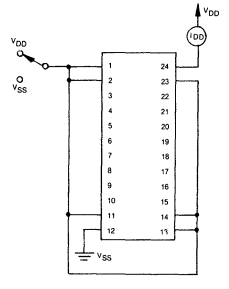
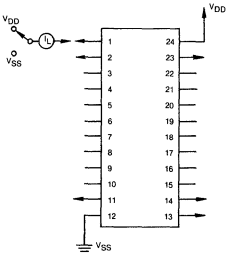


Fig 1 — Quiescent current test circuit



Note
Measure inputs sequentially to both V_{DD} and V_{SS}
Connect all unused inputs to either V_{DD} or V_{SS}

Fig 2 — Input current test circuit

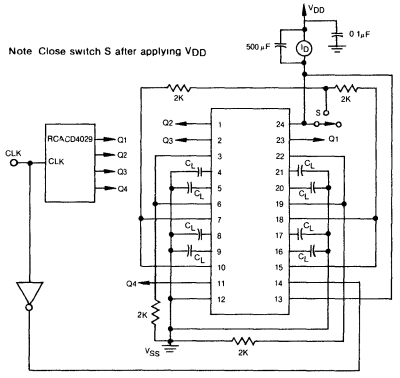


Fig 3 — Dynamic power dissipation test circuit for SSI 22101

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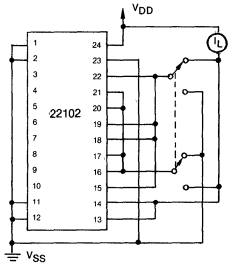


Fig 4 — OFF switch input or output leakage current test circuit (16 or 32 switches)

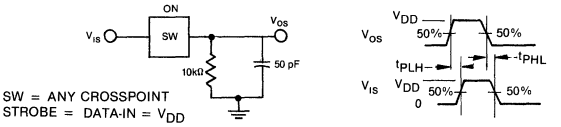


Fig 5 — Propagation delay time test circuit and waveforms (signal input to signal output, switch ON)

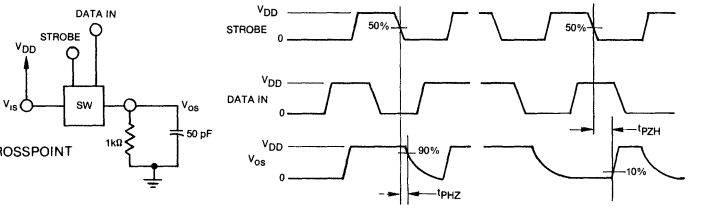


Fig 6 — Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF)

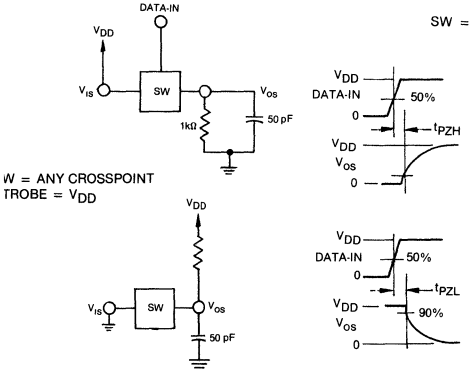


Fig 7 — Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level)

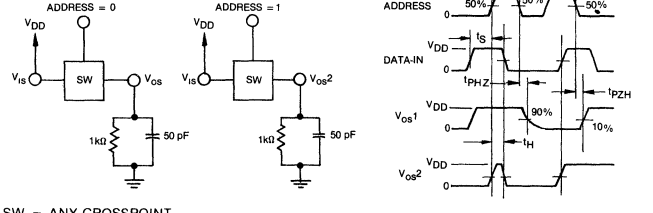
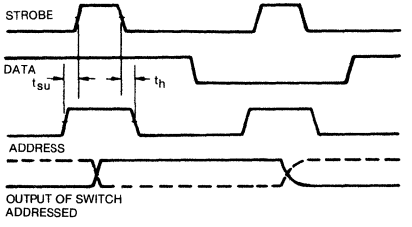
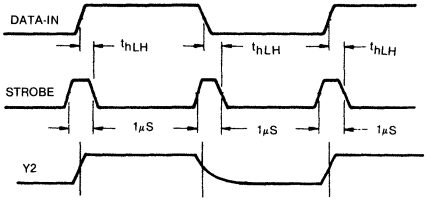


Fig 8 — Propagation delay time test circuit waveforms (address to signal output, switch Turn-ON or Turn-OFF)



Note
If setup and hold times provided are too short, an unaddressed switch may be turned on or off simultaneously with the addressed switch

Fig 9 — Address to strobe setup and hold times



Note
Set all switches to OFF initially Apply V_{DD} to all X inputs and return all Y outputs to V_{SS} through 1K Address X1Y2 (ABCD) with t_{in} 10kHz

Fig 10 — Strobe to Data-In hold time t_h for SSI 22101

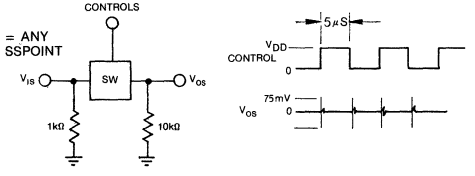


Fig 11 — Test circuit and waveforms for crosstalk (control input to signal output)

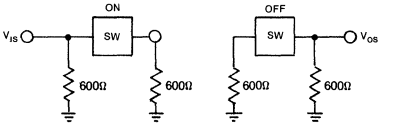


Fig. 12 — Test circuit for crosstalk between switch circuits in the same package

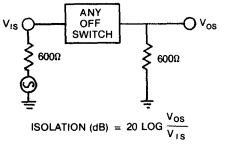


Fig 13 — Test circuit for feedthrough (any OFF switch)

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SSI 22106
8x8x1 Crosspoint Switch with Control Memory

Data Sheet

GENERAL DESCRIPTION

The SSI 22106 is an 8x8x1 analog switch array of CMOS transmission gates designed using high-speed CMOS technology. It offers high noise immunity and has very low static power consumption.

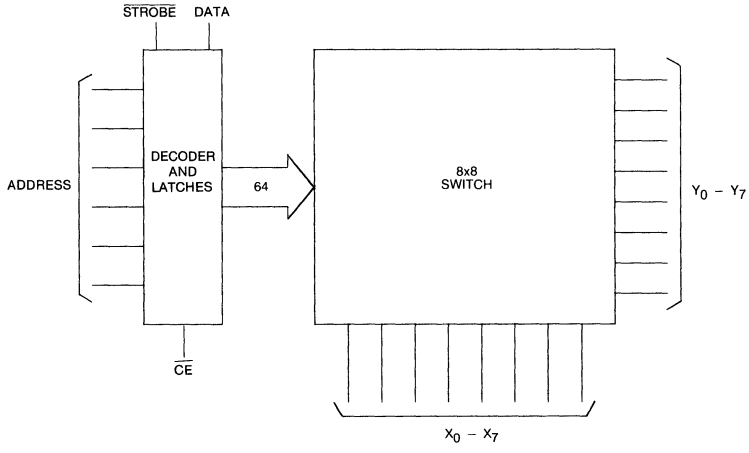
At power up all switches are automatically reset. A "low" on the Master Reset turns OFF all switches and clears the control latches. A 6-bit address through a 6-line-to-64-line decoder selects the transmission gate which can be turned ON by applying a logical ONE to the DATA INPUT and a logical ZERO to the $\overline{\text{STROBE}}$. Similarly, any transmission gate can be turned OFF by applying a logical ZERO to the DATA INPUT while strobing the $\overline{\text{STROBE}}$ with a logical ZERO.

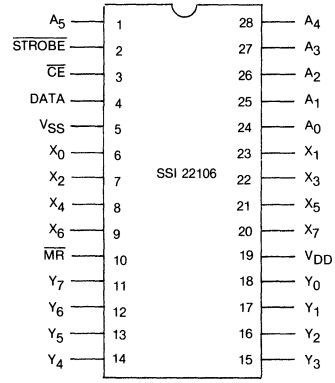
A $\overline{\text{CE}}$ allows the crosspoint array to be cascaded for matrix expansion in both the X and Y direction. The SSI 22106 is supplied in a 28-lead hermetic dual-in-line ceramic package and 28-lead dual-in-line plastic packages.

FEATURES

- **64 crosspoint switches in an 8x8 array**
- **μP compatible control inputs**
- **On chip line decoder and control latches**
- **Ron resistance 95Ω max @ 4.5V**
- **ΔRon 25Ω typical @ 4.5V**
- **Operation voltage 2 - 10V**
- **Analog signal capability Vdd/2**
- **Automatic power up reset**
- **Parallel data input**
- **Second source for RCA CD 22106**
- **Address latches on-chip**
- **CMOS or TTL ("T" suffix) compatible inputs**

SSI 22106 Block Diagram





CAUTION: Use handling procedures necessary for a static sensitive component

PIN DESCRIPTION

Pin No.	Symbol	Description
24,25, 26,27, 28,1,	A0-A5	6 bit address control inputs
2	$\overline{STROBE}$	Strobe input. A "low" of $\overline{STROBE}$ input permits DATA input to turn on or off the switch specified to connect X's and Y's
3	$\overline{CE}$	Chip Enable input. A "low" of $\overline{CE}$ allows the crosspoint array to be cascaded for matrix expansions in both the X and Y directions.
4	DATA	Data Input. With a "zero" of $\overline{STROBE}$, a "one" of DATA turns on the switch and a "zero" of DATA input turns off the switch.
5	Vss	Ground
6,23, 7,22, 8,21, 19,20	X_0-X_7	8 lines in X direction
10	$\overline{MR}$	Master Reset input. A "low" of $\overline{MR}$ turns off all switches and clears the control latches.
18-11	Y_0-Y_7	8 lines in Y direction.
19	V_{DD}	Positive Power Supply.

Maximum Ratings, Absolute — Maximum Values:
DC Supply — Voltage (Vcc)
(Voltages referenced to ground) . . . . . – 0.5 to 11 V
DC Input Diode Current, I_{IK}
(For $V_I < -0.5V$ or $V_I > Vcc + 0.5V$) . . . . . ± 20mA
DC Output Current, I_{OK}
(For $V_O < -0.5V$ or $V_O > Vcc + 0.5V$) . . . . . ± 20mA
DC transmission gate current . . . . . ± 25mA

Power Dissipation per Package (P_D):
For T_A = – 40 to + 60 °C (Package Type P) 500mW
For T_A = + 60 to + 85 °C (Package Type P)
. . . . . Derate Linearly at 12mW/ °C to 200mW
For T_A = – 55 to + 100 °C (Package Type D) . . . 500mW
For T_A = + 100 to 125 °C (Package Type D)
. . . . . Derate Linearly at 12mW/ °C to 200mW

Operating — Temperature Range (T_A):
Package Type D . . . . . – 55 to + 125 °C
Package Type P . . . . . – 40 to + 85 °C

Storage Temperature (T_{stg}) . . . . . – 65 to + 150 °C

Recommended Operating Conditions:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

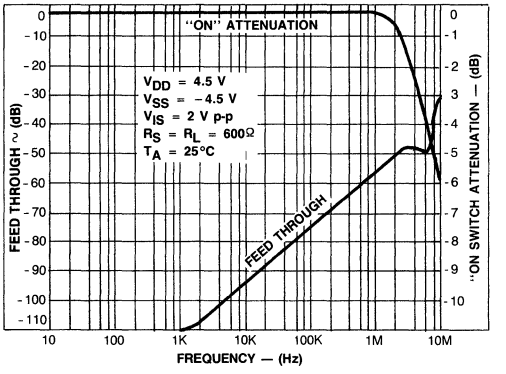
Characteristic	Min	Max	Units
Supply-Voltage Range (For T_A = Full Package Temperature Range) Vcc			
SSI 22106IP, 22106MD	2	10	V
SSI 22106ITP, 22106MTD	4.5	5.5	V
DC Input or Output Voltage Vin, Vout	0	Vcc	V

Static Electrical Characteristics

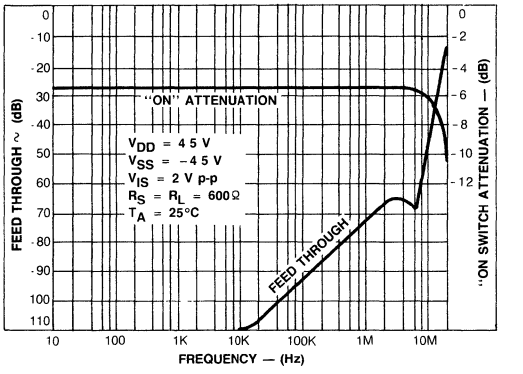
Characteristic	SSI 22106																			Units
	Test Conditions			1P/MD Types			1P Types		MD Types		Test Conditions		1TP/MTD Types			1TP Types		MTD Types		
	V_I	I_O	V_{CC}	+25°C			–40/ +85°C		–55/ +125°C		V_I	V_{CC}	+25°C			–40/ +85°C		–55/ +125°C		
	V	mA	V	Min	Typ	Max	Min	Max	Min	Max	V	V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1 5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4 5	3.15	—	—	3 15	—	3 15	—										
			9	6.3	—	—	6.3	—	6.3	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4 5 to 5.5	—	—	0 8	—	0 8	—	0.8	V
			4.5	—	—	1 35	—	1.35	—	1 35										
			9	—	—	2.7	—	2 7	—	2.7										
Input Leakage Current I_I (Any Control)	V_{CC} or Gnd		10	—	—	±0 1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC} (with $\overline{MR}$ = 1)	V_{CC} or Gnd		10	—	—	5	—	50	—	100	V_{CC} or Gnd	5 5	—	—	2	—	20	—	40	μA

Static Electrical Characteristics (Cont.)

Characteristic	SSI 22106																			Units
	Test Conditions			1P/MD Types			1P Types		MD Types		Test Conditions		1TP/MTD Types			1TP Types		MTD Types		
	V_I	I_O	V_{CC}	+25°C			−40/ +85°C		−55/ +125°C		V_I	V_{CC}	+25°C			−40/ +85°C		−55/ +125°C		
	V	mA	V	Min	Typ	Max	Min	Max	Min	Max	V	V	Min	Typ	Max	Min	Max	Min	Max	
Off Leakage Current I_L (with $\overline{MR}$ = 1)	All Switches OFF		10	—	—	0.1	—	1	—	1	—	5.5	—	—	0.1	—	1	—	1	μA
"On" Resistance R_{on}	V_{CC} to Gnd		2	—	470	700	—	875	—	1050	—	4.5	—	64	95	—	120	—	140	Ω
			4.5	—	64	95	—	120	—	140										
			9	—	45	70	—	90	—	100										
	$V_{CC}/2$		—	—	—	—	—	—	—	—	—	4.5	—	58	85	—	110	—	130	Ω
			4.5	—	58	85	—	110	—	130										
			9	—	40	60	—	80	—	90										
"On" Resistance Between Any Two Channels ΔR_{on}	V_{CC} to Gnd		—	—	—	—	—	—	—	—	V_{CC} to Gnd	4.5	—	25	—	—	—	—	—	Ω
			4.5	—	25	—	—	—	—	—										
			9	—	23	—	—	—	—	—										



Typical "ON" resistance and crosstalk as a function of frequency



Typical "ON" switch attenuation and "OFF" switch feed through as a function of frequency

Switching Characteristics

Characteristic	Test Conditions	V_{SS}	V_{CC}	SSI 22106										Units
				25°C				−40°C to +85°C				−55°C to +125°C		
				IP & MD		ITP & MTD		IP		ITP		MD		MTD		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CONTROLS																
Propagation Delay Time		0	2	—	370	—	—	—	385	—	—	—	400	—	—	
t_{PZH} for Strobe to Output		0	4.5	—	110	—	120	—	125	—	135	—	135	—	150	ns
(Switch Turn-on to High Level)	R_L = 10KΩ	0	9	—	65	—	—	—	70	—	—	—	75	—	—	
t_{PZH} for Data-in to Output	C_L = 50pF	0	2	—	240	—	—	—	255	—	—	—	270	—	—	
(Turn-on to High Level)	t_r,t_f = 6ns	0	4.5	—	75	—	85	—	85	—	95	—	90	—	100	
		0	9	—	50	—	—	—	55	—	—	—	60	—	—	

Switching Characteristics (cont.)

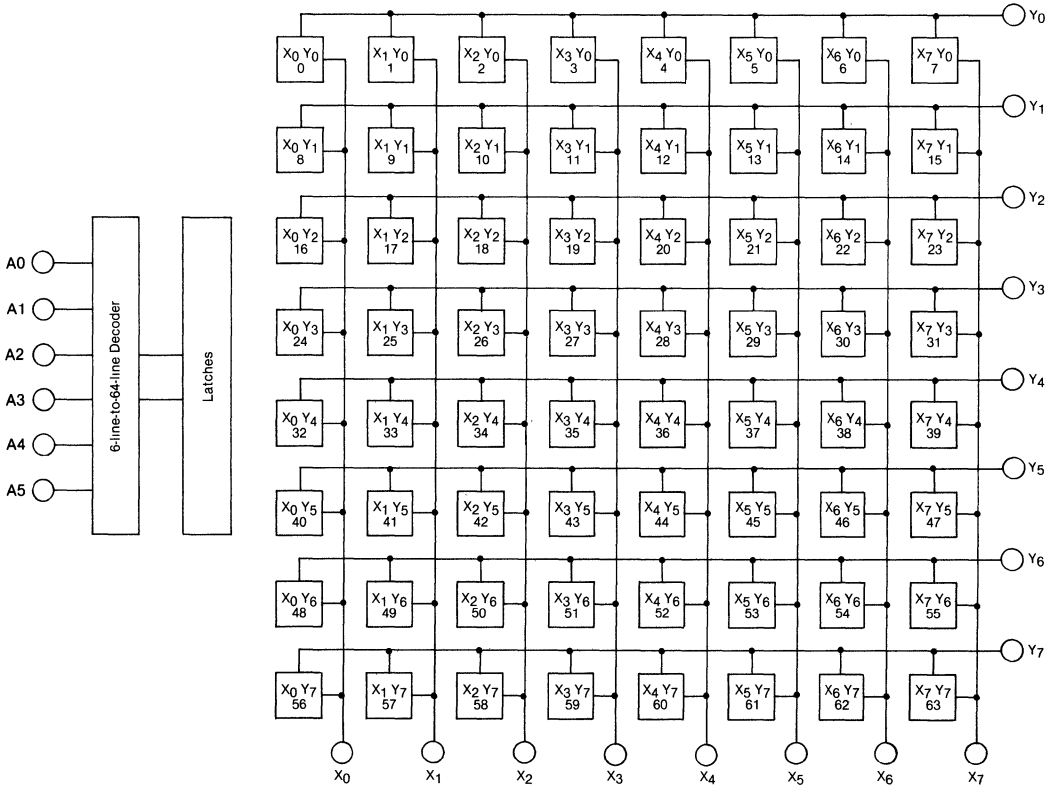
Characteristic	Test Conditions	V_{SS}	V_{CC}	SSI 22106												Units
				25°C				−40°C to +85°C				−55°C to +125°C				
				1P & MD		1TP & MD		1P		1TP		MD		MTD		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Address to Output t_{PZH} (Turn-on to High Level)	R_L = 10 kΩ, C_L = 50 pF, t_r t_r = 6 ns	0	2	—	380	—	—	—	400	—	—	—	420	—	—	
		0	4.5	—	110	—	120	—	125	—	135	—	135	—	150	ns
		0	9	—	65	—	—	—	75	—	—	—	80	—	—	
Propagation Delay Time Strobe to Output t_{PHZ} (Switch Turn-off		0	2	—	400	—	—	—	420	—	—	—	400	—	—	
		0	4.5	—	135	—	150	—	155	—	170	—	160	—	180	
		0	9	—	90	—	—	—	100	—	—	—	110	—	—	
Data-in to Output t_{PZL} (Turn-on to Low Level)		0	2	—	240	—	—	—	255	—	—	—	270	—	—	
		0	4.5	—	75	—	85	—	85	—	95	—	90	—	100	ns
			9	—	50	—	—	—	55	—	—	—	60	—	—	
Address to Output t_{PHZ} (Turn-off)		0	2	—	420	—	—	—	440	—	—	—	460	—	—	
		0	4.5	—	140	—	150	—	155	—	170	—	165	—	180	
		0	9	—	95	—	—	—	100	—	—	—	105	—	—	
Minimum Set-up Time t_{su} Data-in to Strobe, Address		0	2	35	—	—	—	40	—	—	—	45	—	—	—	
		0	4.5	20	—	20	—	20	—	20	—	20	—	20	—	ns
		0	9	15	—	—	—	15	—	—	—	15	—	—	—	
Minimum Hold Time t_H Data-in to Strobe, Address		0	2	85	—	—	—	90	—	—	—	95	—	—	—	
		0	4.5	25	—	25	—	25	—	25	—	25	—	25	—	ns
		0	9	20	—	—	—	20	—	—	—	20	—	—	—	
Minimum Strobe Pulse Width t_W		0	2	200	—	—	—	210	—	—	—	220	—	—	—	
		0	4.5	45	—	55	—	55	—	65	—	60	—	—	70	ns
		0	9	25	—	—	—	30	—	—	—	35	—	—	—	
Maximum Switching Frequency F_O		0	2	0.7	—	—	—	0.6	—	—	—	0.5	—	—	—	
		0	4.5	3.0	—	2.8	—	2.8	—	2.6	—	2.7	—	2.5	—	MHz
		0	9	7	—	—	—	6.5	—	—	—	6.0	—	—	—	
Input (Control) Capacitance C_I		—	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

Analog Channel Characteristics

Characteristic	Test Conditions	V_{IS}	V_{SS}	V_{CC}	SSI 22106											Units
					25°C				−40°C to +85°C				−55°C to +125°C			
					IP & MD		ITP & MD		IP		ITP		MD		MTD	
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation Delay Time t_{PHL} Signal Input to Output t_{PLH}	R_L = 10kΩ, C_L = 50 pF, t_r,t_f = 6 ns	—	0	2	—	30	—	—	—	33	—	—	—	35	—	—	
		—	0	4.5	—	20	-	20	—	22	—	22	—	25	—	25	ns
		—	—	9	—	15	—	—	—	17	—	—	—	19	—	—	
Switch Frequency Response@ −3dB	R_S=R_L=600Ω	2Vp-p	−2.25	2.25	Typ 5		Typ 5										MHz
		2Vp-p	−4.5	4.5	6		6										
Crosstalk Between Any Two Channels	R_S=R_L=600Ω				Typ.		Typ.										
	f=1 KHz	2Vp-p	−2.25	2.25	−110		−110										dB
	f=1 MHz	2Vp-p	−2.25	2.25	−53		−53										
		2Vp-p	−4.5	4.5	−55		−55										

Analog Channel Characteristics (cont.)

Characteristic	Test Conditions	V_{IS}	V_{ss}	V_{cc}	SSI 22106										Units
					25°C				−40°C to +85°C				−55°C to +125°C				
					1P & MD		1TP & MTD		1P		1TP		MD		MTD		
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Switch "OFF"					Typ.		Typ.										
−40dB Feed Through	$R_S = R_L = 600\Omega$	2Vp-p	−2.25	2.25	7		7										MH
−Frequency		2Vp-p	−4.45	4.45	8		8										
Total Harmonic Distortion T_{HD}					Typ.		Typ.										
	$R_L = 10k\Omega$	4Vp-p	−2.25	2.25	.05		.05										
	f=1 kHz sinewave	8Vp-p	−4.5	4 5	.05		.05										%
	$R_L = 600\Omega$	4Vp-p	−2.25	2.25	0.25		0.25										
	f=1kHz sinewave	7Vp-p	−4 5	4.5	0.12		0.12										
Control to Switch					Typ		Typ.										
Feed-thru Noise	$R_L = 10k\Omega$	5	0	5	35		35										
(DATA IN, Strobe, Address)	$t_r, t_f = 6$ ns	10	0	10	65		65										mV
Capacitance C_0					Typ.		Typ.										
X_n to Gnd	f=1 MHz		0	10	48		48										pF
Y_n to Gnd	f=1 MHz		0	10	44		44										



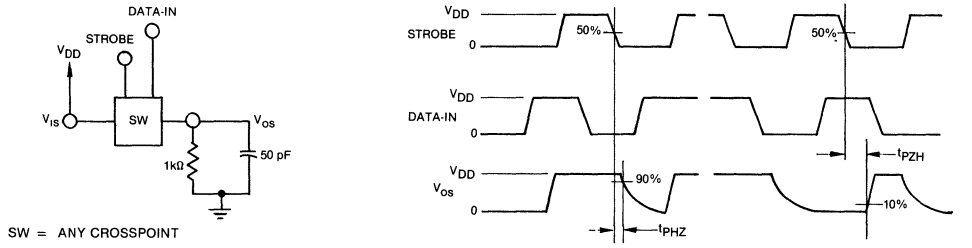
Truth Table

A_5	A_4	A_3	A_2	A_1	A_0	Switch Select
0	0	0	0	0	0	X_0 Y_0
0	0	0	0	0	1	X_1 Y_0
0	0	0	0	1	0	X_2 Y_0
0	0	0	0	1	1	X_3 Y_0
0	0	0	1	0	0	X_4 Y_0
0	0	0	1	0	1	X_5 Y_0
0	0	0	1	1	0	X_6 Y_0
0	0	0	1	1	1	X_7 Y_0
0	0	1	0	0	0	X_0 Y_1
0	0	1	0	0	1	X_1 Y_1
0	0	1	0	1	0	X_2 Y_1
0	0	1	0	1	1	X_3 Y_1
0	0	1	1	0	0	X_4 Y_1
0	0	1	1	0	1	X_5 Y_1
0	0	1	1	1	0	X_6 Y_1
0	0	1	1	1	1	X_7 Y_1

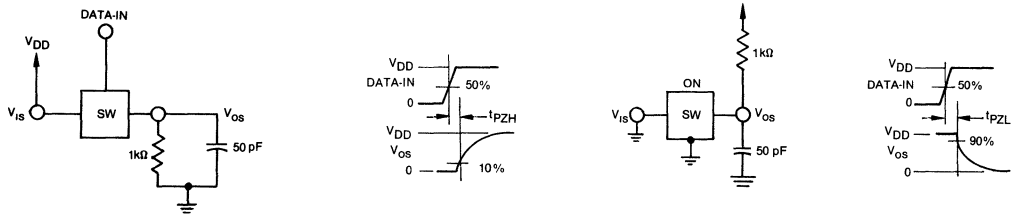
A_5	A_4	A_3	A_2	A_1	A_0	Switch Select
0	1	0	0	0	0	X_0 Y_2
0	1	0	0	0	1	X_1 Y_2
0	1	0	0	1	0	X_2 Y_2
0	1	0	0	1	1	X_3 Y_2
0	1	0	1	0	0	X_4 Y_2
0	1	0	1	0	1	X_5 Y_2
0	1	0	1	1	0	X_6 Y_2
0	1	0	1	1	1	X_7 Y_2
0	1	1	0	0	0	X_0 Y_3
0	1	1	0	0	1	X_1 Y_3
0	1	1	0	1	0	X_2 Y_3
0	1	1	0	1	1	X_3 Y_3
0	1	1	1	0	0	X_4 Y_3
0	1	1	1	0	1	X_5 Y_3
0	1	1	1	1	0	X_6 Y_3
0	1	1	1	1	1	X_7 Y_3

A_5	A_4	A_3	A_2	A_1	A_0	Switch Select
1	0	0	0	0	0	X_0 Y_4
1	0	0	0	0	1	X_1 Y_4
1	0	0	0	1	0	X_2 Y_4
1	0	0	0	1	1	X_3 Y_4
1	0	0	1	0	0	X_4 Y_4
1	0	0	1	0	1	X_5 Y_4
1	0	0	1	1	0	X_6 Y_4
1	0	0	1	1	1	X_7 Y_4
1	0	1	0	0	0	X_0 Y_5
1	0	1	0	0	1	X_1 Y_5
1	0	1	0	1	0	X_2 Y_5
1	0	1	0	1	1	X_3 Y_5
1	0	1	1	0	0	X_4 Y_5
1	0	1	1	0	1	X_5 Y_5
1	0	1	1	1	0	X_6 Y_5
1	0	1	1	1	1	X_7 Y_5

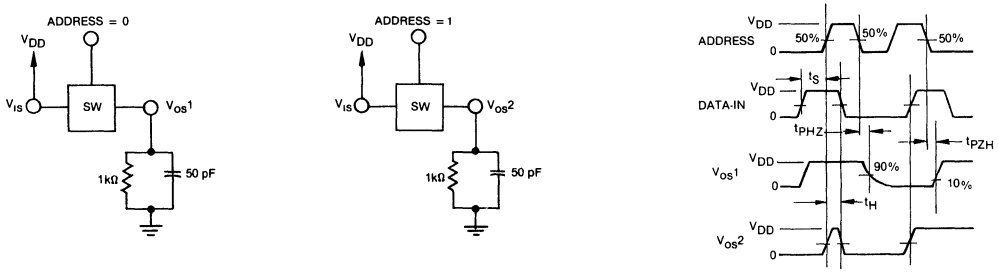
A_5	A_4	A_3	A_2	A_1	A_0	Switch Select
1	1	0	0	0	0	X_0 Y_6
1	1	0	0	0	1	X_1 Y_6
1	1	0	0	1	0	X_2 Y_6
1	1	0	0	1	1	X_3 Y_6
1	1	0	1	0	0	X_4 Y_6
1	1	0	1	0	1	X_5 Y_6
1	1	0	1	1	0	X_6 Y_6
1	1	0	1	1	1	X_7 Y_6
1	1	1	0	0	0	X_0 Y_7
1	1	1	0	0	1	X_1 Y_7
1	1	1	0	1	0	X_2 Y_7
1	1	1	0	1	1	X_3 Y_7
1	1	1	1	0	0	X_4 Y_7
1	1	1	1	0	1	X_5 Y_7
1	1	1	1	1	0	X_6 Y_7
1	1	1	1	1	1	X_7 Y_7



Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF)

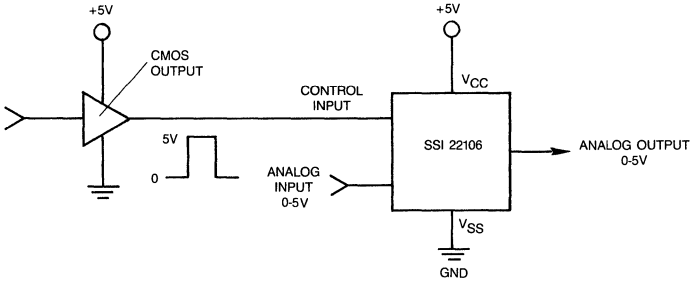


Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level)

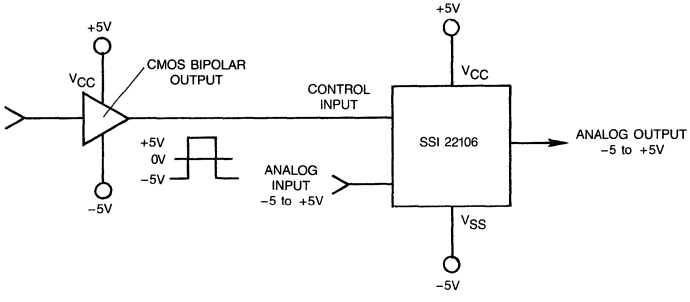


SW-ANY CROSSPOINT
STROBE = V_{DD}

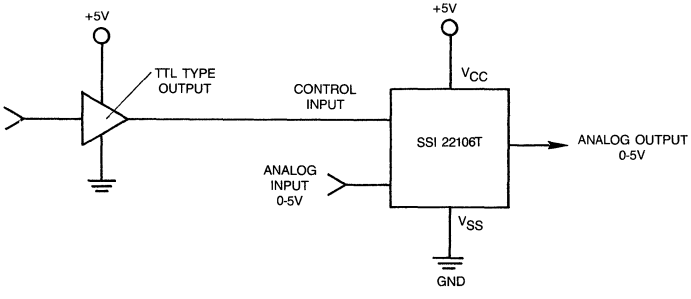
Propagation delay time test circuit waveforms (address to signal output, switch Turn-ON or Turn-OFF)



TYPICAL SINGLE-SUPPLY CONNECTION FOR SSI 22106



TYPICAL DUAL-SUPPLY CONNECTION FOR SSI 22106



TYPICAL SINGLE-SUPPLY CONNECTION FOR SSI 22106T WITH TTL INPUT

silicon systems
14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

Telecommunications Circuits

Device	Circuit Function	Features	Power Supplies	Package
Tone Signaling Products				
SSI 201	Integrated DTMF Receiver	Binary or 2-of-8 output	12V	22 DIP
SSI 202	Integrated DTMF Receiver	Low-power, binary output	5V	18 DIP
SSI 203	Integrated DTMF Receiver	Binary output, Early Detect	5V	18 DIP
SSI 204	Integrated DTMF Receiver	Low-power, binary output	5V	14 DIP
SSI 207	Integrated MF Receiver	Detects central office tone signals	10V	20 DIP
SSI 957	Integrated DTMF Receiver	Early Detect, Dial Tone reject	5V	22 DIP
SSI 20C89	Integrated DTMF Transceiver	Generator and Receiver, µP interface	5V	22 DIP
SSI 20C90	Integrated DTMF Transceiver	Generator and Receiver, µP interface, Call Progress Detect	5V	22 DIP
SSI 980	Call Progress Detector	Detects supervision tones, Teltone second-source	5V	8 DIP
SSI 981	Precise Call Progress Detector	Detects supervision tones, Teltone second-source	5V	22 DIP
SSI 982	Precise Call Progress Detector	Detects supervision tones, Teltone second-source	5V	22 DIP
Modem Products				
SSI K212	1200/300 bps Modem	DPSK/FSK, single chip, autodial, Bell 212A	10V	28 DIP
SSI K214	2400 bps Analog Front End	Analog Processor for DSP V 22 bis Modems	10V	28 DIP
SSI K222	1200, 600, 300 bps Modem	DPSK, FSK, single chip, autodial, V22	5V	28 DIP
SSI 223	1200 bps Modem	FSK, HDX/FDX	10V	16 DIP
SSI K224	2400 bps Modem	QAM, DPSK, FSK single chip V22 bis	10V	28 DIP
SSI 291/213	1200 bps Modem	DPSK, two chips, low-power	10V	40/16 DIP
SSI 3522	1200 bps Modem Filter	Bell 212 compatible, AMI second-source	10V	16 DIP
Speech Synthesis Products				
SSI 263A	Speech Synthesizer	Phoneme-based, low data rate, VOTRAX second-source	5V	24 DIP
Switching Products				
SSI 80C50	T1 Transmitter	Bell D2, D3, D4, serial format and mux, low power	5V	28 DIP,Q
SSI 80C60	T1 Receiver	Bell D2, D3, serial synchron. and demux, low power	5V	28 DIP,Q
SSI 22100	Cross-point Switch	4x4x1, control memory, RCA second-source	12V	16 DIP
SSI 22101/2	Cross-point Switch	4x4x2, control memory, RCA second-source	12V	24 DIP
SSI 22106	Cross-point Switch	8x8x1, control memory, RCA second-source	5V	28 DIP
SSI 22301	PCM Line Repeater	T1 carrier signal recondition	5V	18 DIP

silicon systems™
INNOVATORS IN INTEGRATION

SSI 22301
PCM Line Repeater

Data Sheet

GENERAL DESCRIPTION

The SSI 22301 monolithic PCM repeater circuit is designed for T1 carrier systems operating with a bipolar pulse train of 1.544 Mb/s. It can also be used in the T148 carrier system operating with a ternary pulse train of 2.37 Mb/s. The circuit operates from a 5.1V ± 5% externally regulated supply.

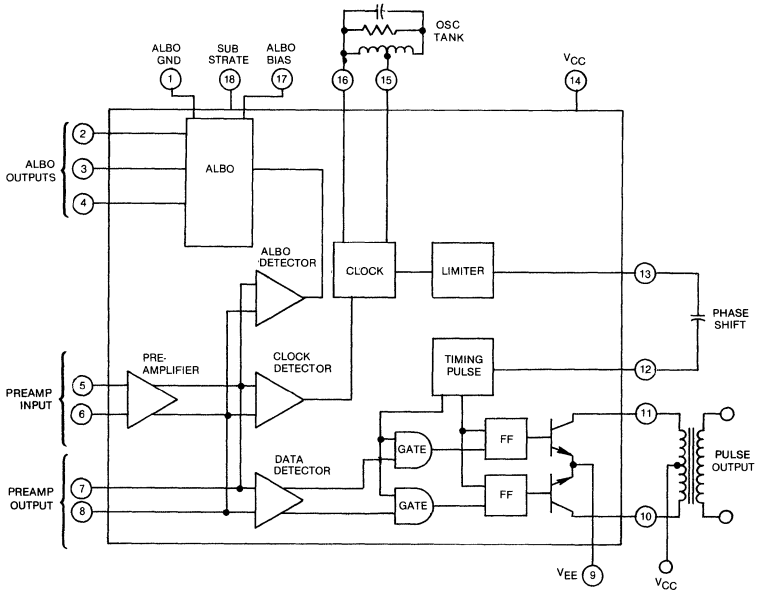
The SSI 22301 provides active circuitry to perform all functions of signal equalization and amplification, automatic line buildout (ALBO), threshold detection, clock extraction, pulse timing, and buffered output formation.

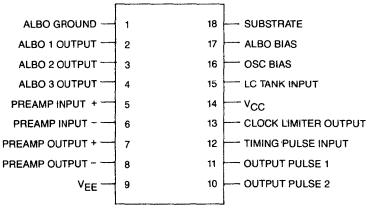
The SSI 22301 is supplied in an 18-lead dual-in-line plastic package.

FEATURES

- **Automatic line buildout**
- **5.IV supply voltage**
- **Buffered output**
- **Second source for RCA CD22301**

Fig. 1 — SSI 22301 Block Diagram





Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

PIN DESCRIPTIONS

No.	Symbol	Description
1.	ALBO Ground	ALBO Ground
2.	ALBO 1 Output	Automatic line build out Output 1
3.	ALBO 2 Output	Automatic line build out Output 2
4.	ALBO 3 Output	Automatic line build out Output 3
5.	Preamp Input +	Positive terminal for pulse input
6.	Preamp Input –	Negative terminal for pulse input
7.	Preamp Output+	Positive terminal for preamplified output pulse
8.	Preamp Output–	Negative terminal for preamplified output pulse
9.	V_{EE}	Emitter power supply or digital ground
10.	Output Pulse 2	Output pulse 2
11.	Output Pulse 1	Output pulse 1
12.	Timing Pulse Input	Phase shifted clock input
13.	Clock Limiter Output	Clock limiter output
14.	Vcc	Collector power supply
15.	LC Tank Input	External LC clock input
16.	OSC Bias	Oscillation bias for LC resonance

PIN DESCRIPTIONS

Pin No.	Symbol	Description
17.	ALBO Bias	ALBO Bias control input
18.	Sub-strate	Substrate ground

Maximum Ratings — Absolute Maximum Values at ambient temperature (T_A) = 25°C

DC Supply Voltage 10V
DC Current (Into Pin 9 or 10) ..... 25 mA
Peak Current (Into Pin 9 or 10) ..... 100 mA
Input Surge Voltage
(Between Pins 5 and 6, t = 10ms) ..... 50 V
Output Surge Voltage
(Between Pins 10 and 11, t = 1 ms) ..... 50 V
Power dissipation per package (P_D)
For T_A = −40 to +60°C ..... 500 mW
For T_A = +60°C
to +85°C .... Derate linearly at 12 mW/°C) to 200 mW
Device dissipation per output transistor
For T_A = full package-temperature range ..... 100 mW
Operating temperature range ..... −40 to +85°C
Storage temperature range ..... −65 to +150°C
Lead temperature (during soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max ..... +256°C

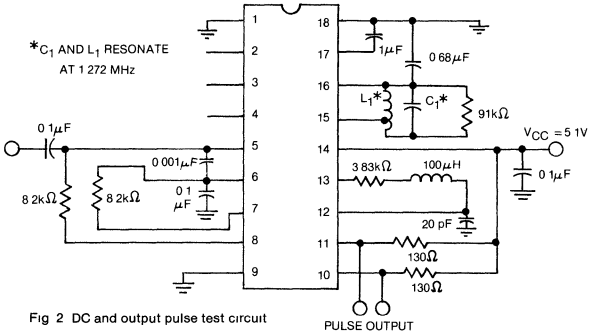


Fig 2 DC and output pulse test circuit

Static Electrical Characteristics T_A = 25°C, V_{CC} = 5.1V ± 5%

Characteristic	Pins	Fig.	Min.	Typ.	Max.	Units
ALBO Ports Off Voltage	2,3,4,17	2	—	0	0.1	V
Amplifier Pin Voltage	5,6,7,8		2.4	2.9	3.4	V
Output Voltage	10,11		—	5.1	—	V
Clock Pin Voltage	12,13,15,16		3.1	3.6	4.1	V
DC Currents						
Supply Current	14	2	—	22	30	mA
Output Leakage Current	10,11		—	0	100	A

Dynamic Electrical Characteristics T_A = 25°C, V_{CC} = 5.1 V ± 5%

Characteristic	Symbol	Fig.	Note	Min.	Typ.	Max.	Units
Preamplifier Input Impedance	Zin	3	—	20	—	—	kΩ
Preamplifier Output Impedance	Zout	3	—	—	—	2	kΩ
Preamplifier Gain @ 2.37 MHz	Ao	3	—	47	50	—	dB

Dynamic Electrical Characteristics (cont'd)

Characteristic	Symbol	Fig.	Note	Min.	Typ.	Max.	Units
Preamplifier Output Offset Voltage	ΔVout	3	1	– 50	0	50	mV
Clock Limiter Input Impedance	Zin (CL)	4	2	10	—	—	kΩ
ALBO Off Impedance	Z_{ALBO} (off)	4	3	20	—	—	kΩ
ALBO On Impedance	Z_{ALBO} (on)	4	4	—	—	10	Ω
DATA Threshold Voltage	V_{TH} (D)	5	5,8	0.75	0.8	0.85	V
CLOCK Threshold Voltage	V_{TH}(CL)	5	6,8	—	1.12	—	V
ALBO Threshold	V_{TH} (AL)	5	7,8	1.5	1.6	1.7	V
V_{TH} (D) as % of V_{TH} (AL)	—	—	—	—	42	45	49	%
V_{TH} (CL) as % of V_{TH} (AL)	—	—	—	—	65	70	75	%
Buffer Gate Voltage (low)	V_{OL}	2	9	0.65	0.8	0.95	V
Differential Buffer Gate Voltage	ΔV_{OL}	2	9	– 0.15	0	0.15	V
Output Pulse Rise Time	t_r	2,6	9,10	—	—	40	ns
Output Pulse Fall Time	t_f	2,6	9,10	—	—	40	ns
Output Pulse Width	tw	2,6	9,10	290	324	340	ns
Pulse Width Differential	Δtw	2,6	9,10	– 10	0	10	ns
Clock Drive Current	ICL	—	—	—	2	—	mA

Notes.
1. No signal input Measure voltage between pins 7 and 8
2 Measure clock limiter input impedance at pin 15.
3 Adjust potentiometer for 0 volts. Measure ALBO off impedances from pins 2, 3 and 4 to pin 1
4 Increase potentiometer until voltage at pin 17 = 2 Vdc Measure ALBO on impedances from pins 2, 3 and 4 to pin 1
5 Adjust potentiometer for ΔV = 0 volts Then slowly increase ΔV in the positive direction until pulses are observed at the DATA terminal
6 Continue increasing ΔV until the DC level at the clock terminal drops to 4 volts
7 Continute increasing ΔV until the ALBO terminal rises to 1 volt
8 Turn potentiometer in the opposite direction and measure negative threshold voltages by repeating tests outlined in notes 5, 6, and 7
9 Set e_{in} = 2 75 mV (rms) at f = 1 185 MHz. Adjust frequency until maximum amplitude is obtained at pin 15 Observe output pulses at pins 10 and 11
10 Adjust input signal amplitude until pulses just appear in outputs Increase input amplitude by three dB

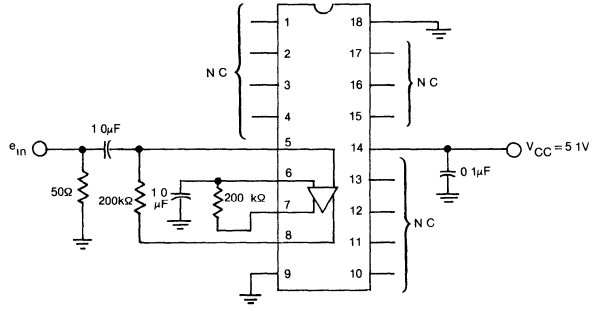


Fig 3 - Preamplifier gain and impedance measurement circuit

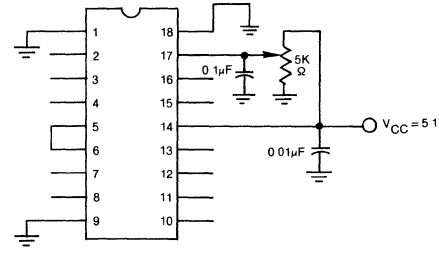


Fig 4 - Test circuit for impedance measurement

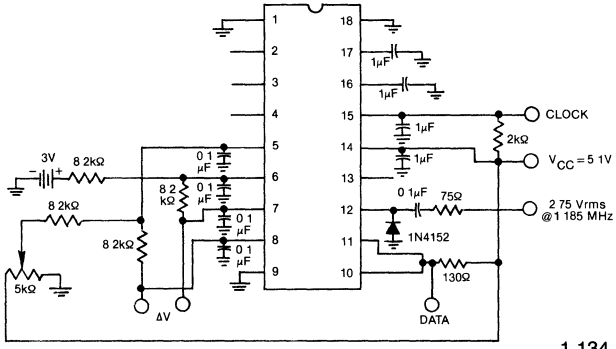


Fig 5 - Test circuit for threshold voltage measurement

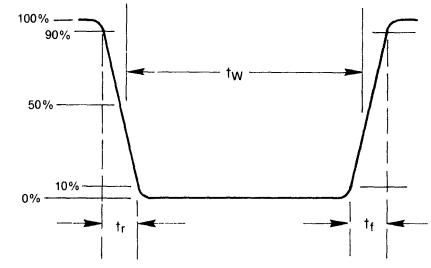


Fig 6 - Output pulse waveform

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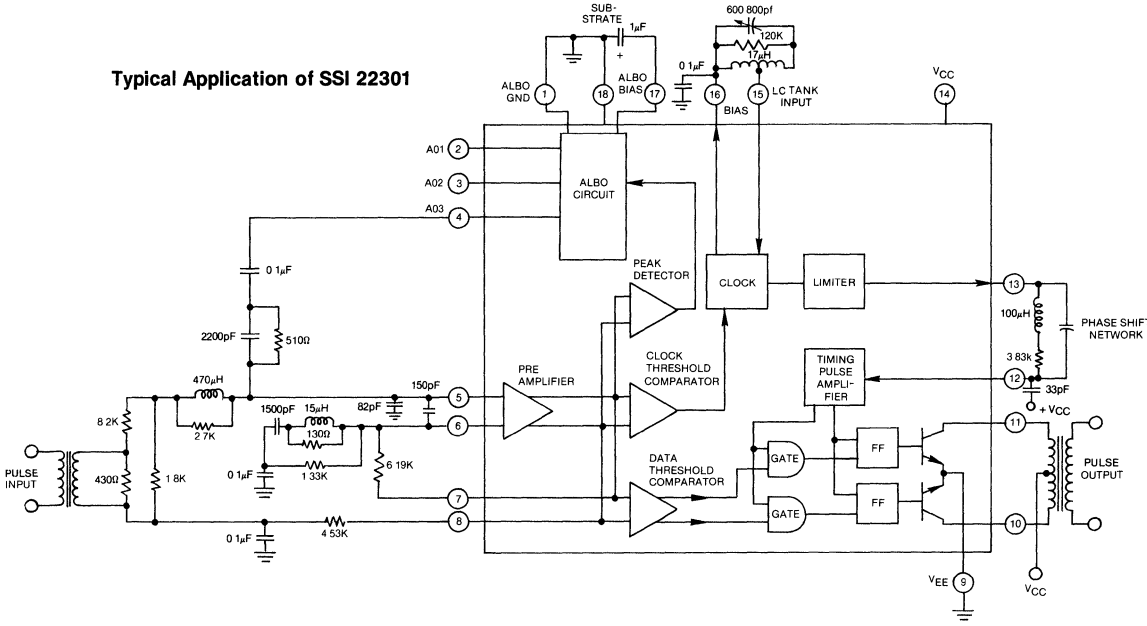
Typical Application of SSI 22301



Section 2
MICROPERIPHERAL PRODUCTS

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SSI MPD Product Selector Guide

MICROPERIPHERAL PRODUCTS

Device	Head Type	# of Channels	Power Supplies	Internal Write Current Source	Internal Center Tap Voltage Source	Internal R_d Option	Read Gain (typ)	Write Current Range (mA)	Read/Write Data Port(s)	Page No.
HDD Read/Write Amplifiers										
SSI 104	Ferrite	4	+6V, −4V			x	35	15 to 45	Differential, Bi-directional	2-2
SSI 104L	Ferrite	4	+6V, −4V			x	35	15 to 45	Differential, Bi-directional	2-2
SSI 108	Ferrite	4	+6V, −4V			x	35	15 to 45	Differential, Bi-directional	2-2
SSI 114	Thin Film	4	±5V	x	N/A	x	123	55 to 110	Differential/Differential	2-6
SSI 115	Ferrite	2,4,5	±5V		x		40	30 to 50	Differential, Bi-directional	2-10
SSI 117	Ferrite	2,4,6	+5V, +12V	x	x	x	100	10 to 50	Differential/TTL	2-16
SSI 117A	Ferrite	2,4,6	+5V, +12V	x	x	x	100	10 to 50	Differential/TTL	2-22
SSI 122	Ferrite	4	+6V, −4V				35	15 to 45	Differential, Bi-directional	2-2
SSI 188	Ferrite	4	+6V, −5V		x		43	35 to 70	Directional, Bi-directional	2-28
SSI 501	Ferrite	6,8	+5V, +12V	x	x	x	100	10 to 50	Differential/TTL	2-34
SSI 510	Ferrite	4	+5V, +12V	x	x	x	100	10 to 35	Differential/TTL	2-40
SSI 520	Thin Film	4	±5V	x	N/A	x	123	30 to 75	Differential/Differential	2-46
SSI 521	Thin Film	6	+5V, +12V	x	N/A	x	100	20 to 70	Differential/TTL	2-50

Device	Function	Power Supplies	Features	Page No.
HDD Head Positioning				
SSI 101A	Preamplifier-Ferrite Head	8.3V/10V	Av = 93, BW = 10MHz, e_n = 7.0nV/√Hz	2-54
SSI 101A-2	Preamplifier-Ferrite Head	+12V	Av = 93, BW = 10MHz, e_n = 7.0nV/√Hz	2-54
SSI 116	Preamplifier-Thin Film Head	8.3V/10V	Av = 250, BW = 20MHz, e_n = 0.94nV/√Hz	2-56
SS116-2	Preamplifier-Thin Film Head	+12V	Av = 250, BW = 20MHz, e_n = 0.94nV/√Hz	2-56
HDD Read Data Path				
SSI 531	Data Separator	+5V	High Performance PLL, XTAL OSC, Write Precompensation	2-58
SSI 540	Read Data Processor	+5V, +12V	Time Domain Filter	2-66
SSI 541	Read Data Processor	+5V, +12V	AGC, Amplitude & Time Pulse Qualification, RLL Compatible	2-74
HDD Motor Control/Support Logic				
SSI 545	Support Logic	+5V	Includes 57506 Bus Drivers/Receivers	2-80
SSI 590	2-Phase Motor Speed Control	+12V	±0.035% Speed Accuracy	2-84
SSI 591	3-Phase Motor Speed Control	+12V	±0.05% Speed Accuracy	2-88
Floppy Disk Drive Circuits				
SSI 570	Read Data Path	+5V, +12V	2 Channel Read/Write With Read Data Path	2-92
SSI 575	Read/Write	+5V, +12V	2,4 Channel Read/Write Circuit	2-98
SSI 580	Support Logic	+5V, +12V	Port Expander, Includes SA400 Interface Drivers/Receivers	2-102
Tape Drive Circuits				
SSI 550	Read Data Path	+5V, +12V	4 Channel Read/Write w/ Read Data Path	2-108
Memory Products				
SSI 67C401	64 x 4 FIFO	+5V	Low Power, High Speed Buffer (10MHz, 15MHz)	2-114
SSI 67C402	64 x 5 FIFO	+5V	Low Power, High Speed Buffer (10MHz, 15MHz)	2-114

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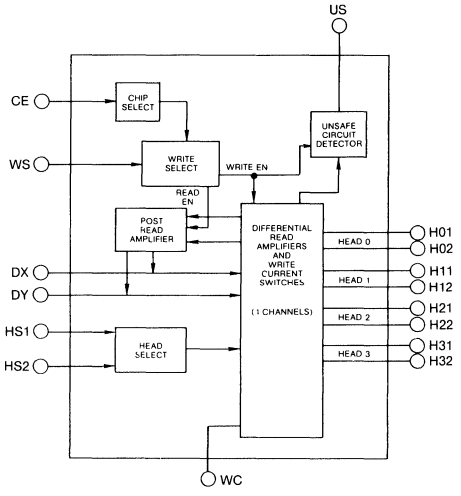
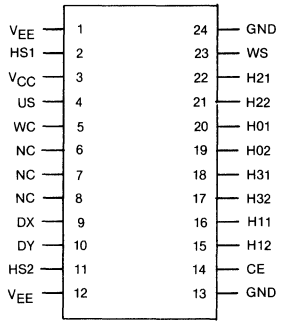
4-Channel Read/Write Circuit SSI 104, 104L, 108, 122

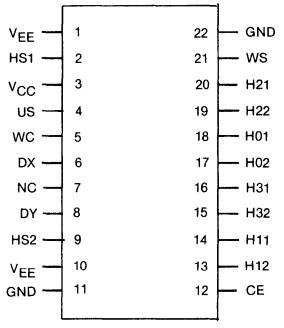
Data Sheet



Block Diagram



SSI 104/108 Pin Out



SSI 122 Pin Out

FEATURES

- **IBM 3350 compatible performance.**
- **IBM compatible power supply voltages and logic levels.**
- **Four read/write channels.**
- **Safety circuits**

DESCRIPTION

The SSI 104 is a monolithic bipolar integrated circuit for use in high performance disk drive systems where it is desirable to locate the control circuitry directly on the data arm. Each circuit controls four heads and has three modes of operation: Read, Write and Idle.

The 104L is a low-noise version of the 104 with all other parameters identical. Both are packaged in a 24 pin flat pack.

The SSI 108 and 122 are identical in performance to the 104. The 108 is packaged in a 24 pin dip package while the 122 is packaged in a 22 pin dip.

4-Channel Read/Write Circuit SSI 104, 104L, 108, 122

CIRCUIT OPERATION

WRITE MODE

In the write mode, the circuit functions as a current gate. Externally supplied write current is gated by the state of the head select and data inputs to one side of one head. Head voltage swings are monitored by the head transition detect circuit. Absence of proper head voltage swings, indicating an open or short on either side of the head or absence of write current, will cause a fault current to flow into the unsafe pin.

READ MODE

In the read mode, the circuit functions as a low noise differential amplifier. The state of the head select inputs determines which amplifer is active. Data is differentially read from one of four heads and an open collector differential signal is put across the Data X and Data Y pins. If a fault condition exists such that write current is applied to the chip when the chip is in read mode, the write current will be drawn from the unsafe pin and the fault will be detected.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage V_{CC} 7.0V
Negative Supply Voltage, V_{EE} . . . . . −5.5V
Operating Junction Temperature . . . . . 0 °C to 110 °C
Storage Temperature . . . . . −65 °C to 150 °C

Input Voltages
- Head Select (HS) . . . . . V_{EE} −0.3V to + 0.3V
- Unsafe (US) . . . . . −0.3V to V_{CC} + 0.5V
- Write Current (WC) . . . . . V_{EE} −2 to 0.3V

Data (Dx, Dy) . . . . . V_{EE} −0.3V to 0.3V
Chip Enable (CE) . . . . . V_{EE} −0.3V to V_{CC} + 0.5V
Write Select (WS) . . . . . −0.3V to V_{CC} + 0.3V

ELECTRICAL CHARACTERISTICS Unless otherwise specified, $5.7 \leq V_{CC} \leq 6.7$, $-4.2 \leq V_{EE} \leq -3.8$, $0° \leq T, \leq 110°C$.

POWER SUPPLY **ALL UNITS**

Parameter	Test Conditions	Min.	Max.	Units
Positive Supply Current (ICC)	Read/Write	11.5	23	mA
Positive Supply Current (ICC)	Idle		75 + ICE	mA
Negative Supply Current (IEE)	Read/Write		70	mA
Negative Supply Current (IEE)	Idle		52	mA

LOGIC SIGNALS

Parameter	Test Conditions	Min.	Max.	Units
Chip Enable Low Voltage (VLCE)	Read/Write	0.0	0.7	V
Chip Enable High Voltage (VHCE)	Idle	VCC − 1.0	VCC + 0.3	V
Chip Enable Low Current (ILCE)	VCE = 0.0V	−1.45	−0.47	mA
Chip Enable High Current (IHCE1)	VCE = VCC − 1.0	−350	−100	μA
Chip Enable High Current (IHCE2)	VCE = VCC + .3V		+100	μA
Write Select High Voltage (VHWS)	Write/Idle	3.2	3.8	V
Write Select Low Voltage (VLWS)	Read/Idle	−0.1	0.1	V
Write Select High Current (IHWS)	Write/Idle, VWS = 3.8V Transition unsafe current off Transition unsafe on	 0.6 0.6	 3.2 4.2	 mA mA
Write Select Low Current (ILWS)	Read/Idle, VWS = 3.8V		0.1	mA
Head Select High Voltage (VHHS)		−1.12	−0.72	V
Head Select Low Voltage (VLHS)		−2.38	−1.51	V
Head Select High Current (IHHS)			240	μA
Head Select Low Current (ILHS)			60	μA
Total Head Input Current	Sum of all head input currents with IWC = 0 Write, VCT = 3.5V Read, VCT = 0.0V Idle		 3.7 0.16 1.25	 mA mA mA

READ MODE

Parameter	Test Conditions	Min.	Max.	Units
Differential Gain	Vin = ImV p-p, 0VDC, f = 300kHz			
	Tj = 22°C	28	43	V/V
	Tj = 0°C	28	46	V/V
	Tj = 110°C	22.2	43	V/V
Common Mode Rejection Ratio	Vin = 100mVpp, 0VDC, f≤ 5MHz	45		dB
Power Supply Rejection Ratio	Vin = 0V, f≤ 5MHz △VCC or △VEE = 100mVpp	45		dB
Bandwidth	Zin = 0Ω , Vin = 1mVPP, f midband = 300kHz	30		MHz
Input Noise	Vin = 0V, Zin = 0Ω, Power Bandwidth = 15MHz		9.3	μVRMS
Input Noise (104L)	Vin = 0V, Zin = 0Ω, Power Bandwidth = 15MHz		6.6	μVRMS
Input Current	Vin = 0V		26	μA
Differential Input Capacitance	Vin = 0V		23.5	pF
Differential Input Resistance	Vin = 0V			
	Tj = 22°C	585	915	Ω
	Tj = 0°C	565	915	Ω
	Tj = 110°C	585	1070	Ω
Output Offset Voltage	Zin = 0		120	mV
Common Mode Output Voltage	Vin = 0	−0.78	−0.32	V
Unsafe Current	Write Current = 0mA		0.1	mA
	Write Current = −45mA	40	45	mA
Dynamic Range	DC input voltage where AC gain falls to 90% of 0VDC input value. (Measured with 0.5mVpp AC input, Tj = 30°C	2.0		mVp
Channel Separation	Vin = 1mVpp, 0VDC, f = 5MHz 3 channels driven	40		dB

WRITE MODE

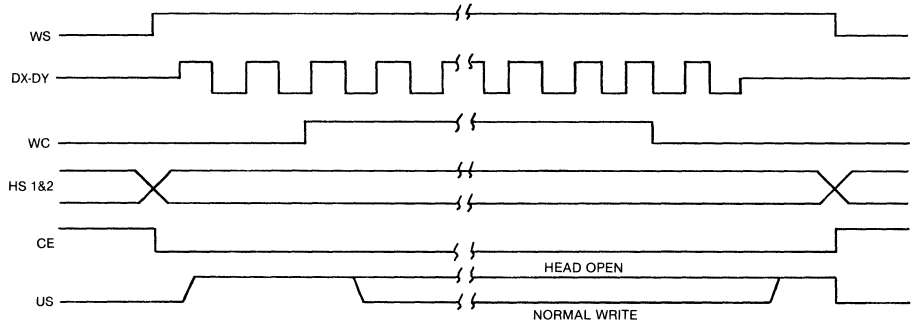
Parameter	Test Conditions	Min.	Max.	Units
Differential Input Voltage		0.175		V
Single Ended Input Voltage		−0.68	−0.45	V
Write Current		−45		mA
Current Gain	IWC = −45mA	0.95	1.0	
Write Current Voltage	IWC = −45mA	VEE+0.25	VEE+1.0V	V
Unsafe Voltage	IUS = +45mA	4	VCC+.3	V
Head Center Tap Voltage		3.2	3.8	V
Differential Head Voltage	IWC = −45mA, Lh = 10μH	5.7	7.2	Vp
Single Ended Head Voltage	IWC = −45mA, Unselected heads at 3.5V			
	Selected Side of Selected			
	Head Current = 0mA	0.0	0.9	V
	= 90mA	1.4+VCC	3.7+VCC	V
Unsafe Current	IWC = −30mA, f = 2MHz; Lh = 9μH		1.0	mA
	VUS = 5.0V − 6.3V, Lh = 0	15	45	mA
	IWC = 45mA, Rh = ∞one side of head only	15	45	mA
Unselected Head Current	IWC = −45mA, f = 2MHz, Lh = 9.5μH		2.0	mAp
DX DY Input Current		−2.0	2.0	mA

SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min.	Max.	Units
Idle to Read/Write Transition Time		—	0.5	μS
Read/Write to Idle Transition Time		—	0.5	μS
Read to Write Transition Time		—	0.5	μS
Write to Read Transition Time		—	0.5	μS
Head Select Switching Delay		—	50.0	nS
Head Current Transition Time	IWC = −45mA, Lh = 0, f = 5MHz	—	15	nS
Head Current Switching Delay Time	IWC = −45mA, Lh = 0, f = 5MHz	—	15	nS
Head Current Switching Hysterisis	IWC = −45mA, Lh = 0, f = 5MHz Data rise and fall time $\leq$1nSec	—	2	nS
Unsafe Switching Delay Time	IWC = −30mA, f = 2MHz; Lh = 9μH Lh = 0μH	— 0.8	1 5.1	μS μS

HEAD SELECT TABLE

Head Selected	HS1	HS2
0	1	1
1	0	1
2	1	0
3	0	0



WRITE MODE SYSTEM TIMING

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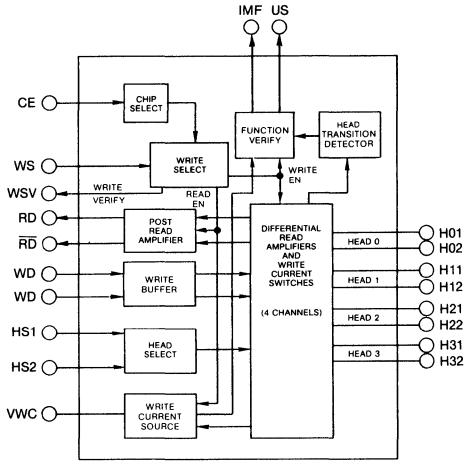
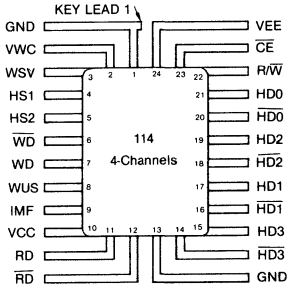
Thin Film - 4-Channel Read/Write Circuit SSI 114

Preliminary Data Sheet



SSI 114 Block Diagram



SSI 114 Pin Out

FEATURES

- **Thin film head compatible performance**
- **Four Read/Write Channels**
- **TTL - compatible logic levels**
- **Operates on standard +5 volt and −5 volt power supplies**

DESCRIPTION

The SSI 114 is an integrated read/write circuit designed for use with non-center tapped thin film heads in disk drive systems. Each chip controls four heads and has three modes of operation: read, write, and idle. The circuit contains four channels of read amplifiers and write drivers and also has an internal write current source.

A current monitor (IMF) output is provided that allows a multichip enable fault to be detected. An enabled chip's output will produce one unit of current. An open collector output, write select verify (WSV), will go low if the write current source transistor is forward biased. The circuit operates on +5 volt, and −5 volt power and is available in a 24 pin flatpack.

Thin Film - 4-Channel Read/Write Circuit SSI 114

CIRCUIT DESCRIPTION

WRITE MODE

In the write mode (R/$\overline{W}$ and CE low) the circuit functions as a differential current switch. The Head Select inputs (HS1 and HS2) determine the selected head. The Write Data Inputs (WD, $\overline{WD}$) determine the polarity of the head current. The write current magnitude is adjustable by an external 1% resistor, R_X from VWC to VCC, where

$$I_W = \frac{K_W}{R_X\left(1 + \frac{R_h}{R_d} + \frac{R_h}{1k}\right)} - 0.7mA$$

Where K_W = Current Gain Factor = 130 Amp-Ohms
R_h = Head plus External Wire Resistance
R_d = Damping Resistance

READ MODE

In the Read Mode, (R/$\overline{W}$ high and CD low), the circuit functions as a differential amplifier. The amplifier input terminals are determined by the Head Select inputs.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage, V_{CC} 6V
Negative Supply Voltage, V_{EE} . . . . . −6V
Operating Junction Temperature . . . . . 25°C to 125°C
Storage Temperature . . . . . −65°C to 150°C
Lead Temperature (Soldering, 10 sec) . . . . . 260°C
Input Voltages
- Head Select (HS) . . . . . −0.4V to V_{CC} + 0.3V
- Chip Enable ($\overline{CE}$) . . . . . −0.4V to V_{CC} + 0.3V
- Read Select (R/$\overline{W}$) . . . . . −0.4V or −2mA to V_{CC} + 0.3V
- Write Data (WD, $\overline{WD}$) . . . . . V_{EE} to 0.3V
- Head Inputs (Read Mode) . . . . . −0.6V to +0.4V

Outputs
- Read Data (RD, $\overline{RD}$) . . . . . 0.5V to V_{CC} + 0.3V
- Write Unsafe (WUS), ... −0.4V to V_{CC} + 0.3V and 20mA
- Write Select Verify (WSV) . . . . . −0.4V to V_{CC} + 0.3V and 20mA
- Current Monitor (IMF) . . . . . −0.4V to V_{CC} + 0.3V
- Current Reference (VWC) . . . . . V_{EE} to V_{CC} + 0.3V and 8mA
- Head Outputs (Write Mode) . . . . . I_W max = 150mA

Thermal Characteristics
- Flatpack Package . . . . . ΘJA = 144°C/W(still air), ΘJA = 30°C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75 ≤ VCC ≤ 5.25, −5.5 ≤ VEE ≤ −4.95V, 25° ≤ T (junction) ≤ 125°C.

POWER SUPPLY

Parameter	Test Conditions	Min.	Max.	Units
Power Dissipation	All modes, 25 ≤ T_j ≤ 100 100° ≤ T_j ≤ 125°C	— —	612 + 6.7 Iw 563 + 6.7 Iw	mW mW
Positive Supply Current (ICC)	Idle Mode	—	10 + Iw/19	mA
Positive Supply Current (ICC)	Read Mode	—	40 + Iw/19	mA
Positive Supply Current (ICC)	Write Mode	—	38 + Iw/19	mA
Negative Supply Current (IEE)	Idle Mode	−12 − Iw/19	—	mA
Negative Supply Current (IEE)	Read Mode	−66 − Iw/19	—	mA
Negative Supply Current (IEE)	Write Mode	−75 − 1.16Iw	—	mA

LOGIC SIGNALS

Parameter	Test Conditions	Min.	Max.	Units
Chip Enable Low Voltage (VLCE)	Read or Write Mode	—	0.8	V
Chip Enable High Voltage (VHCE)	Idle Mode	2.0	—	V
Chip Enable Low Current (ILCE)	VLCE = 0V	−1.60	—	mA
Chip Enable High Current (IHCE)	VHCE = 2.0V	—	−0.3	mA
Read Select High Voltage (VHR/W)	Read or Idle Mode	2.0	—	V
Read Select Low Voltage (VLR/W)	Write or Idle Mode	—	0.8	V
Read Select High Current (IHR/W)	VHR/W = 2.0V	—	0.015	mA
Read Select Low Current (ILR/W)	VLR/W = 0V	−0.15	—	mA
Head Select High Voltage (VHHS)		2.0	—	V
Head Select Low Voltage (VLHS)		—	0.8	V

HEAD SELECT TABLE

Head Selected	HS1	HS2
0	0	0
1	1	0
2	0	1
3	1	1

LOGIC SIGNALS

Parameter	Test Conditions	Min.	Max.	Units
Head Select High Current (IHHS)	VHHS = VCC	—	0.25	mA
Head Select Low Current (ILHS)	VLHS = 0V	−0.1	0.25	mA
WUS, WSV Low Level Voltage	ILUS = 8mA (denotes safe condition)	—	0.5	V
WUS, WSV High Level Current	VHUS = 5.0V (denotes unsafe condition)	—	100	μA
IMF on Current		2.20	3.70	mA
IMF off Current		—	0.02	mA
IMF Voltage Range		0	VCC + 0.3	V

READ MODE Tests performed with 100Ω load resistors from RD and $\overline{RD}$ through series isolation diodes to VCC.

Parameter	Test Conditions	Min.	Max.	Units
Differential Voltage Gain	Vin = 1mVpp, f = 300kHz	75	170	V/V
Voltage Bandwidth (−3dB)	Zs < 5Ω , Vin = 1mVpp f midband = 300kHz	45	—	MHz
Input Noise Voltage	Zs = 0Ω , Vin = 0V, Power Bandwidth = 15MHz	—	1.1	$nV/\sqrt{Hz}$
Differential Input Capacitance	Vin = 0V, f = 5MHz	—	65	pF
Differential Input Resistance	Vin = 0V, f = 5MHz	45	96	Ω
Input Bias Current (per side)	Vin = 0V	—	0.17	mA
Dynamic Range	DC input voltage where AC gain falls to 90% of the gain with .5mVpp input signal	−3.0	3.0	mV
CMRR	Vin = 100mVpp, 0V DC 1MHz ≤ f ≤ 10MHz 10MHz ≤ f ≤ 20MHz	 54 48	 — —	 dB dB
Power Supply Rejection Ratio	VCC or VEE = 100mVpp 1MHz ≤ f ≤ 10MHz 10MHz ≤ f ≤ 20MHz	 54 36	 — —	 dB dB
Channel Separation	The 3 unselected channels are driven with Vin = 100mVpp 1MHz ≤ f ≤ 10MHz 10MHz ≤ f ≤ 20MHz	 43 37	 — —	 dB dB
Output Offset Voltage		−360	360	mV
Output Leakage Current	Idle Mode	—	0.01	mA
Output Common Mode Voltage		VCC − 1.1	VCC − 0.3	V
Single Ended Output Resistance		10	—	KΩ
Single Ended Output Capacitance		—	10	pF

WRITE MODE

Parameter	Test Conditions	Min.	Max.	Units
Current Range (Iw)		55	110	mA
Current Tolerance	Current set to nominal value by Rx, Rh = 7Ω ± 10%, Tj = 50°C, Rd = 59Ω	−8	+8	%
(Iw) (Rh) Product		0.24	1.30	V
Differential Head Voltage Swing	Iw = 100mA, Lh = 0.2 μH, Rh = 10Ω	3.8	—	Vpp

WRITE MODE

Parameter	Test Conditions	Min.	Max.	Units
Unselected Head Transient Current	Iw = 100mA, Lh = 0.2 μH, Rh = 10Ω, Non adjacent heads tested to minimize external coupling effects	—	2	mAp
Head Differential Load Resistance, Rd		48	97	Ω
Head Differential Load Capacitance		—	30	pF
Differential Data Voltage, (WD—$\overline{WD}$)		0.20	—	V
Data Input Voltage Range		−1.87	+0.1	V
Data Input Current (per side)	Chip Enabled	—	150	μA
Data Input Capacitance	per side to GND	—	10	pF

SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min.	Max.	Units
Idle to Read/Write Transition Time		—	1.0	μS
Read/Write to Idle Transition Time		—	1.0	μS
Read to Write Transition Time	VLCE = 0.8V, Delay to 90% of Iw	—	0.6	μS
Write to Read Transition Time	VLCE = 0.8V, Delay to 90% of 20MHz Read Signal envelope, Iw decay to 10%	—	1.0	μS
Head Select Switching Delay	Read or Write Mode	—	0.40	μS
Shorted Head Current Transition Time	Iw = 100mA, Lh < 0.05 μH, Rh = 0	—	13	nS
Shorted Head Current Switching Delay Time	Iw = 100mA, Lh < 0.05 μH, Rh = 0, measured from 50% of input to 50% of current change	—	18	nS
Head Current Switching Time Symmetry	Iw = 100mA, Lh = 0.2 μH, Rh = 10Ω, WD & $\overline{WD}$ transitions 2nS, switching time symmetry 0.2nS	—	1.5	nS
WSV Transition Time	Delay from 50% of write select swing to 90% of final WSV voltage, Load = 2KΩ // 20pF	—	1.0	μS
Unsafe to Safe Delay After Write Data Begins (WUS)	f(data) = 10MHz	—	1.0	μS
Safe to Unsafe Delay, (WUS)	Non-switching write data, no write current, or shorted head close to chip	0.6	3.6	μS
Safe to Unsafe Delay, (WUS)	Head open or head select input open	—	0.6	μS
IMF Switching Time	Delay from 50% of CE to 90% of final IMF current	—	1.0	μS

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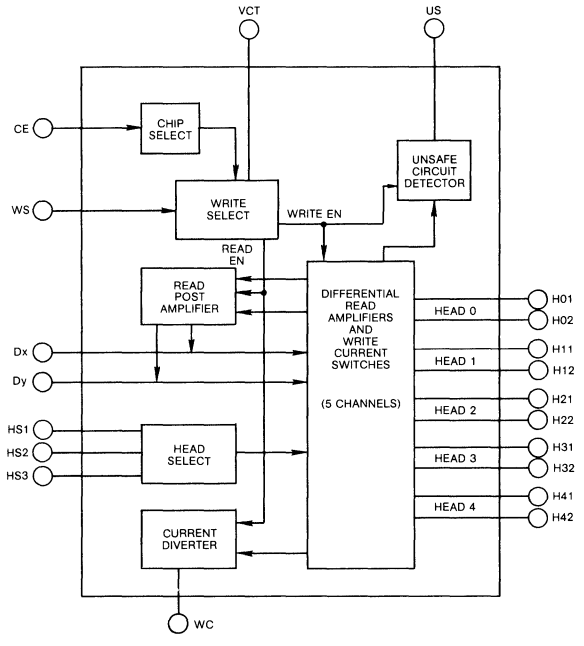
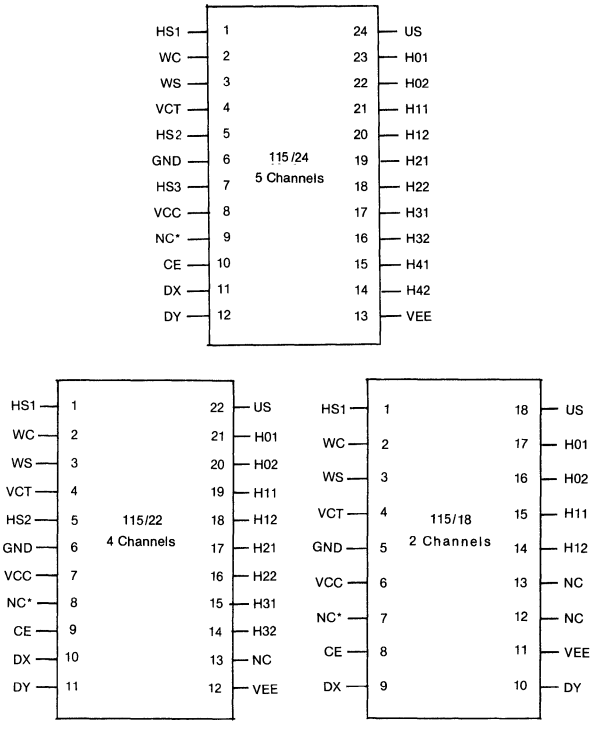
SSI 115
Winchester Read/Write Circuit

Data Sheet



SSI 115 Block Diagram



SSI 115 Pin Out
(Top View)

*Do not connect to any etch or any part of any circuit

FEATURES

- **Electrically compatible with 8 inch and 5-1/4 inch Winchester disk drive magnetic recording heads.**
- **Supports up to five recording heads per circuit.**
- **Detects and indicates unsafe write conditions.**
- **On-chip current diverter eliminates the need for external write current switching.**
- **Control signals are TTL compatible.**
- **Operates on standard +5 volt and −5 volt (or −5.2 volt) power sources.**

DESCRIPTION

The SSI 115 is a monolithic bipolar integrated circuit designed for use with 8 inch and 5-1/4 inch Winchester disk drive magnetic recording heads. The circuit interfaces with up to five magnetic recording heads providing the required read/write electronic functions as well as various control and data protect functions. The circuit operates on +5 volt and −5 volt (or −5.2 volt) power and is available in a variety of packages. The 115/24 is a 5 channel circuit available in both flatpack and dip packages. The 115/22 is a 4 channel circuit packaged in a 22 pin dip and the 115/18 is a 2 channel circuit offered in a 18 pin dip package.

SSI 115
Winchester
Read/Write Circuit

CIRCUIT OPERATION

WRITE MODE

With both the chip enable and write select signals activated, the SSI 115 is switched to the write mode and the circuit operates as a differential current switch. The center tap head voltage (VCT) is turned on, the unsafe circuit detector is activated, and the current diverter is disabled. The head select signals (HS1, HS2, HS3) select one of five differential current switches. The selected current switch senses the polarity of the data input signal (Dx−Dy) and gates write current to the corresponding side of the head (HN1 or HN2). Head overshoot voltages that occur during normal write operation are sensed to determine safe or unsafe head circuit conditions. The detector senses the following unsafe conditions—no data transitions, head open, or no write current.

READ MODE

With chip enable active and write select disabled, the SSI 115 is switched to the read mode and the circuit operates as a differential amplifier. The center tap head voltage is turned off, the unsafe circuit detector is deactivated, and the write current diverter is enabled. The differential head input signal (HN1−HN2), selected by the head select signals, is amplified by a differential read amplifier and appears as a differential output signal on the data lines (Dx, Dy).

During the read and idle modes, the on-chip current diverter circuit prevents write current from flowing in the head circuits. Therefore, external gating of the write current source is not required.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage, VCC 6V
Negative Supply Voltage, VEE..... −6V
Write Current (IWC) ..... 70 mA
Operating Junction Temperature ..... 25°C to 135°C
Storage Temperature..... −65°C to 150°C
Lead Temperature (Soldering, 10 SEC)..... 260°C

Input Voltages

Head Select (HS) .. .. −0.4V to VCC +0.3V
Unsafe (US) (IHUS ≤ 15mA)... −0.3V to VCC +0 3V
Write Current (WC) Voltage in read idle modes. (Write mode must be current limited to −70mA) .... VEE −0.3V to 0.3V
Data (Dx, Dy) ..... VEE to 0.3V
Chip Enable ($\overline{CE}$) .. .. −0.4V to VCC +0.3V
Write Select ($\overline{WS}$) ..... −0.4V to VCC +0.3V

RECOMMENDED OPERATING CONDITIONS

VCC ..... 5V IWC . ..... −45mA
VEE..... −5V (−5.2)V LH..... 10μh

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $4.75 \leq VCC \leq 5.25V$, $-5.5V \leq VEE \leq -4.75V$
$25°C \leq T$ (Junction) $\leq 135°C$

POWER SUPPLY

Parameter	Test Conditions	Min.	Max.	Units
Total Power Dissipation (PD)	Write Mode, IWC≤45mA, TJ≥125°C		700	mW
Positive Supply Current (ICC)	Read/Write Mode		35 + IWC	mA
Positive Supply Current (ICC)	Idle Mode		10	mA
Negative Supply Current (IEE)	Read/Write Mode	-65		mA
Negative Supply Current (IEE)	Idle Mode	−10		mA

LOGIC SIGNALS

Parameter	Test Conditions	Min.	Max.	Units
Chip Enable Low Voltage (VLCE)	Read or Write Mode	−0.3	0.8	V
Chip Enable Low Current (ILCE)	VLCE = 0V	−2.4		mA
Chip Enable High Current (IHCE)	Idle Mode	−250		μA
Write Select Low Voltage (VLWS)	Write or Idle Mode	−0.3	0.8	V
Write Select Low Current (ILWS)	VLWS = 0V	−3 2		mA

LOGIC SIGNALS (Cont.)

Parameter	Test Conditions	Min.	Max.	Units
Write Select High Current (IHWS)	Read or Idle Mode	−250		μA
Head Select High Level Voltage (VHHS)		2.0	VCC	V
Head Select High Level Current (IHHS)	VHHS = VCC		100	μA
Head Select Low Level Voltage (VLHS)		−0.3	0.8	V
Head Select Low Level Current (ILHS)	VLHS = 0V	−0 6		mA
Unsafe Low Level Voltage (VLUS)*	ILUS = 8mA (Denotes Unsafe Condition)		0.5	V
Unsafe High Level Current (IHUS) *	VHUS = 5.0V (Denotes Safe Condition)		100	μA

*Note: Unsafe is an open collector output

READ MODE: Tests performed with 50 load resistors from Dx and Dy to ground.

Parameter	Test Conditions	Min.	Max.	Units
Input Common Mode Range		−0.6	0.1	V
Total Input Bias Current	$-0.6V \leq Vin \leq 0.1V$		60	μA
Differential Voltage Gain	Vin = 1mVpp, f = 300kHz	26	52	V/V
Voltage Bandwidth (−3dB)	$Zs \leq 10\Omega$, Vin = 1mVpp, $f_{midband}$ = 300kHz	30		MHz
Input Noise Voltage	Zs = 0, Vin = 0V, Power Bandwidth = 15MHz		7	μV_{rms}
Differential Input Capacitance	Vin = 0, f = 5MHz		20	pF
Differential Input Resistance (Internal Damping Resistor)	Vin = 0, f = 300kHz	560	1070	Ω
Output Offset Voltage			120	mV
Differential Head Current	IWC = 45mA, LH = 10μH, f = 2MHz		2	mAp
Output Common Mode Voltage		−0 4	− 125	V
Single Ended Output Resistance	f = 300kHz	10		kΩ
Single Ended Output Capacitance			10	pF
Dynamic Range	DC input voltage where the AC gain falls to 90% of its 0VDC input value (Measured with 0.5mVpp AC input voltage)	2		mVp
Common Mode Rejection Ratio	Vin = 100mVpp, 0VDC, f = 5MHz	50		dB
Power Supply Rejection Ratio	ΔVCC or ΔVEE, 100 mVpp, f=5MHz	45		dB
Channel Separation	The 4 unselected channels are driven with Vin = 100mVpp, f = 5MHz	45		dB
Write Current Voltage	IWC = 45mA	−2.7	−0.5	V
Total Head Input Current	IWC = 0		200	μA

WRITE MODE

Parameter	Test Conditions	Min.	Max.	Units
Current Gain (IH/IWC)	IWC = 45mA, IH ≙ Head Current	0.95	1.0	
Write Current Pin Voltage	IWC = 45mA	−3.7	−1.5	V
Center Tap Head Voltage (VCT)	IWC = 45mA	3.0	VCC-0.5	V
Differential Head Voltage Swing	3.0 ≤ VCT ≤ VCC −0.5V IWC = 45mA, LH = 10μH	5.7	7.7	V
Differential Data Voltage (Dx-Dy)		.175		V
Single Ended Data Input Voltage (Dx, Dy)		−0.9	0.1	V
Data Input Current	−0.9 ≤ VDx, VDy ≤ 0.1	−10	100	μA
Data Input Differential Resistance	f = 300kHz	5		kΩ
Data Input Capacitance			10	pF
Unselected Diff Head Current	IWC = 45mA, LH = 10μH, f = 2MHz		2	mA_p
Write Current Range		30	50	mA
Total Head Input Current	IWC = 0		500	μA

IDLE MODE

Parameter	Test Conditions	Min.	Max.	Units
Write Current Pin Voltage	IWC = 45mA	VEE		V
Differential Head Current	IWC = 45mA, LH = 10μH, f = 2MHz		2	mA_p
Total Head Input Current	IWC = 0		500	μA

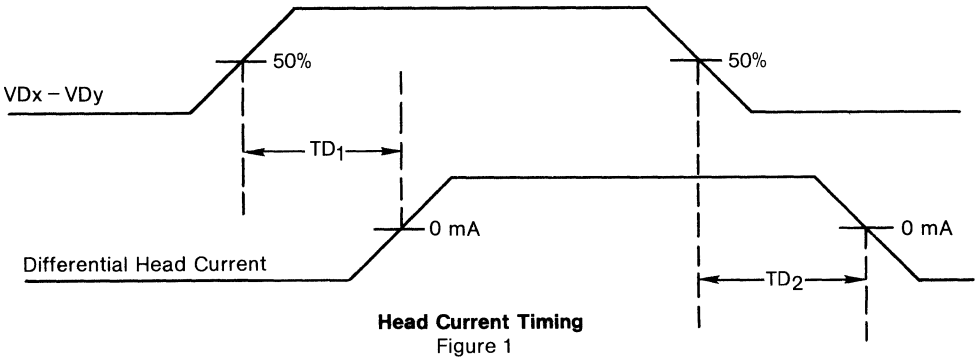
SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min.	Max.	Units
Idle to Read/Write Transition Time			0.6	μS
Read/Write to Idle Transition Time			0.6	μS
Read to Write Transition Time	0 ≤ VLCE ≤ 0.8V (Circuit Enabled)		0.6	μS
Write to Read Transition Time	0 ≤ VLCE ≤ 0.8V (Circuit Enabled)		0.6	μS
Head Select Switching Delay Time			0.25	μS
Head Current Transition Time	(10% to 90% points) IWC = 45mA, LH = 0H, RH = 0 Ω		15	nS
Head Current Switching Delay Time (TD_1, TD_2)	IWC = 45mA, LH = 0H, RH = 0 Ω f = 5MHz (see figure 1)		19	nS
Head Current Switching Hysteresis TH = (TD_1-TD_2)	IWC = 45mA, LH = 0H, RH = 0 Ω f = 5MHz (VDx-VDy) Rise Time = 2nS (see figure 1)		3	nS
Unsafe to Safe Delay After Write Data Begins (TD_3)	IWC = 30mA, LH = 10μH f = 2MHz (see figure 2A)		1.0	μS
Safe to Unsafe Delay (TD_4)	LH' = 10μH, f = 2MHz IWC = 45mA (see figure 2B)	1.6	8.0	μS

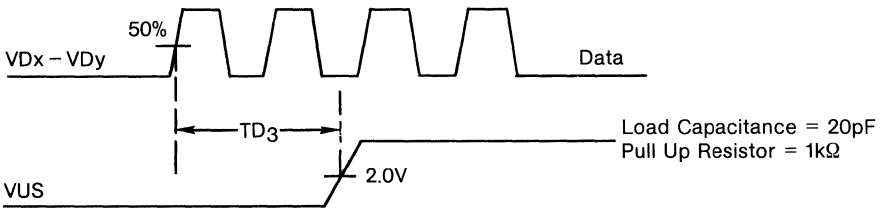
HEAD SELECT TABLE

Head Selected	HS1	HS2	HS3
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1

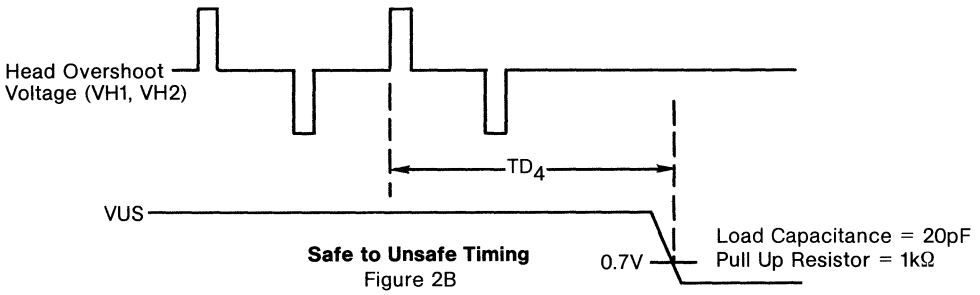
Note: Invalid Head Select input codes (5, 6 and 7) have the effect of not selecting any heads.



Head Current Timing
Figure 1



Unsafe to Safe Timing
Figure 2A



Safe to Unsafe Timing
Figure 2B

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INNOVATORS IN INTEGRATION

SSI 117/117 R– Series 2, 4, or 6-Channel Read/Write Circuits

Data Sheet

GENERAL DESCRIPTION

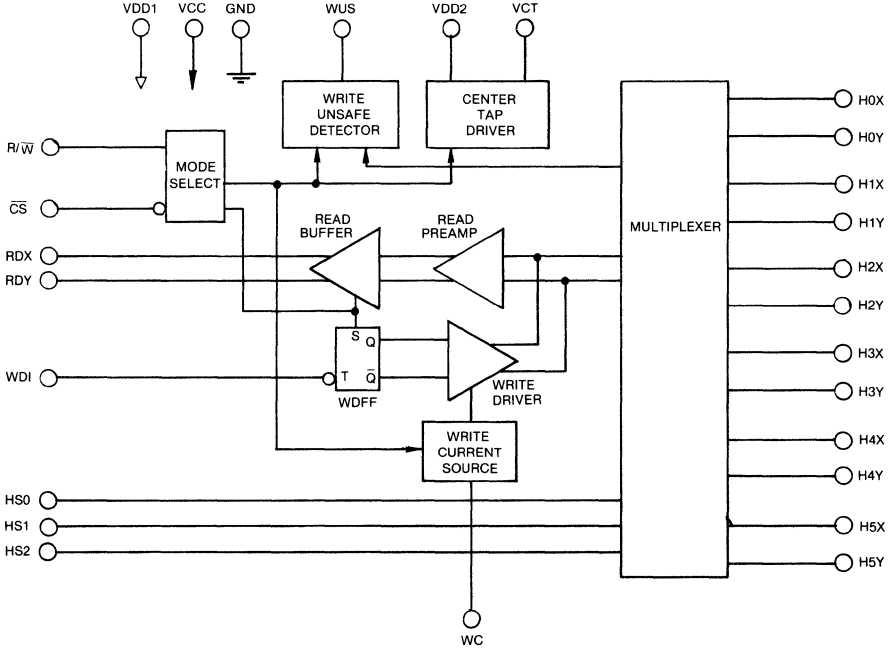
The SSI 117 devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as six channels. The SSI 117 requires +5V and +12V power supplies and is available in 2, 4, or 6 channel versions with a variety of packages.

The SSI 117R differs from the SSI 117 by having internal damping resistors.

FEATURES

- **+5V, +12V power supplies**
- **Single- or multi-platter Winchester drives**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Available in 2, 4, or 6 channels**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**

SSI 117 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

Circuit Operation

The SSI 117 functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables 2 & 3. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the SSI 117A as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data Flip Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by

Iw = K/Rwc, where K = Write Current Constant

is set by the external resistor, Rwc, connected from pin WC to GND.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

READ MODE

In the Read mode the SSI 117A is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. They should be AC coupled to the load.

Note that the internal write current source is deactivated for both the Read and the chip deselect mode. This eliminates the need for external gating of the write current source.

TABLE 1: PIN DESCRIPTIONS

Symbol	Name — Description
HS0 - HS2	Head Select: selects up to six heads
$\overline{CS}$	Chip Select: a low level enables device
R/$\overline{W}$	Read/Write: a high level selects Read mode
WUS	Write Unsafe: a high level indicates an unsafe writing condition
WDI	Write Data In: a negative transition toggles the direction of the head current
H0X - H5X H0Y - H5Y	X, Y head connections
RDX, RDY	X, Y Read Data: differential read signal out
WC	Write Current: used to set the magnitude of the write current
VCT	Voltage Center Tap: voltage source for head center tap
VCC	+5V
VDD1	+12V
VDD2	Positive power supply for the Center Tap voltage source
GND	Ground

TABLE 2: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 3: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	none

0 = Low level
1 = High level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND)

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD1 VDD2 VCC	−0.3 to +14 −0.3 to +14 −0.3 to +6	VDC VDC VDC
Digital Input Voltage Range	Vin	−0.3 to VCC +0.3	VDC
Head Port Voltage Range	VH	−0.3 to VDD +0.3	VDC
WUS Port Voltage Range	Vwus	−0.3 to +14	VDC
Write Current	IW	60	mA
Output Current: RDX, RDY VCT WUS	Io	−10 −60 +12	mA mA mA
Storage Temperature Range Junction Temperature Range Lead Temperature (10 sec Soldering)	Tstg Tj	−65 to +150 +25 to +125 260	°C °C °C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD1 VCC	12 ± 10% 5 ± 10%	VDC VDC
Head Inductance	Lh	5 to 15	μH
Damping Resistor (117 only)	RD	500 to 2000	ohms
RCT Resistor	RCT	130 ± 5% (1/2 watt)	ohms
Write Current	IW	25 to 50	mA

DC CHARACTERISTICS Unless otherwise specified VDD1 = 12V ± 10%, VCC = 5V ± 10%, +25°C ≤ Tj ≤ +125°C.

Parameter	Test Conditions	Min.	Max.	Units
VCC Supply Current	Read/Idle Mode Write Mode	— —	25 30	mA mA
VDD Supply Current	Idle Mode Read Mode Write Mode	— — —	25 50 30 + IW	mA mA mA
Power Dissipation	Tj = +125°C Idle Mode Read Mode Write Mode, IW = 50mA, RCT = 130Ω Write Mode, IW = 50mA, RCT = 0Ω	 — — — —	 400 600 700 1050	 mW mW mW mW
Digital Inputs: Input Low Voltage (V_{IL}) Input High Voltage (V_{IH}) Input Low Current Input High Current	 V_{IL} = 0.8V V_{IH} = 2.0V	 −0.3 2.0 −0.4 —	 0.8 VCC + 0.3 — 100	 VDC VDC mA μA
WUS Output V_{OL} I_{OH}	I_{OL} = 8mA V_{OH} = 5.0V	— —	0.5 100	VDC μA
Center Tap Voltage (V_{CT})	Read Mode Write Mode	4.0 (typ) 6.0 (typ)		VDC VDC

WRITE CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, +25°C ≤ Tj ≤ +125°C IW = 45mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz, CL (RDX, RDY) ≤20pF.

Parameter	Test Conditions		Min.	Max.	Units
Write Current Range			10	50	mA
Write Current Constant "K"			133	147	V
Differential Head Voltage Swing			8	—	V (pk)
Unselected Head Transient Current			—	2	mA (pk)
Differential Output Capacitance			—	15	pF
Differential Output Resistance		117	10K	—	Ω
		117R	562	938	Ω
WDI Transition Frequency	WUS = low		125	—	KHz
Iwc to Head Current Gain			20 (typ)		—
Unselected Head Leakage	Sum of X & Y Side Leakage Current		—	85	μA

READ CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, IW = 45mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz, CL (RDX, RDY) ≤20pF (Vin is referenced to VCT), +25°C ≤ Tj ≤ +125°C

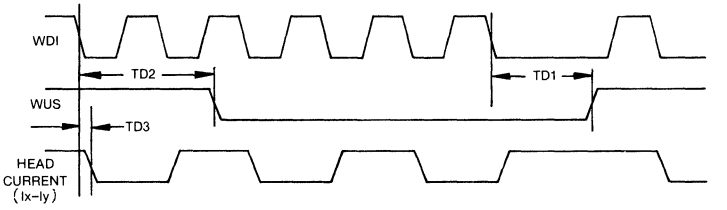
Parameter	Test Conditions		Min.	Max.	Units
Differential Voltage Gain	Vin = 1mVpp @ 300kHz RL (RDX), RL (RDY) = 1kohm		80	120	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5mVpp @ 300kHz		−3	3	mV
Bandwidth (−3db)	|Zs| < 5Ω, Vin = 1mVpp		30	—	MHz
Input Noise Voltage	BW = 15MHz, Lh = 0, Rh = 0		—	2.1	nV/√Hz
Differential Input Capacitance	f = 5MHz		—	20	pF
Differential Input Resistance	f = 5 MHz	117	2K	—	Ω
		117R	390	810	Ω
Input Bias Current (per side)			—	45	μA
Common Mode Rejection Ratio	Vcm = VCT + 100mVpp @ 5MHz		50	—	db
Power Supply Rejection Ratio	100mVpp @ 5MHz on VDD1, VDD2, or VCC		45	—	db
Channel Separation	Unselected Channels: Vin = 100mVpp @ 5MHz and Selected Channel: Vin = 0mVpp		45	—	db
Output Offset Voltage			−480	+480	mV
Common Mode Output Voltage		Read Mode	5	7	V
		Write/Idle Mode	4.3 typ		V
Single Ended Output Resistance	f = 5MHz		—	30	Ω
Leakage Current, RDX, RDY	RDX, RDY = 6V Write/Idle Mode		−100	100	μA
Output Current	AC Coupled Load RDX to RDY		2	—	mA

SWITCHING CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, +25°C ≤ Tj ≤ +125°C IW = 45mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz.

Parameter		Test Conditions	Min.	Max.	Units
R/$\overline{W}$:	R/$\overline{W}$ to Write	Delay to 90% of Write Current	—	1.0	μS
	R/$\overline{W}$ to Read	Delay to 90% of 100mV 10MHz Read Signal Envelope or to 90% Decay of Write Current	—	1.0	μS
$\overline{CS}$:	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope	—	1.0	μS
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current	—	1.0	μS

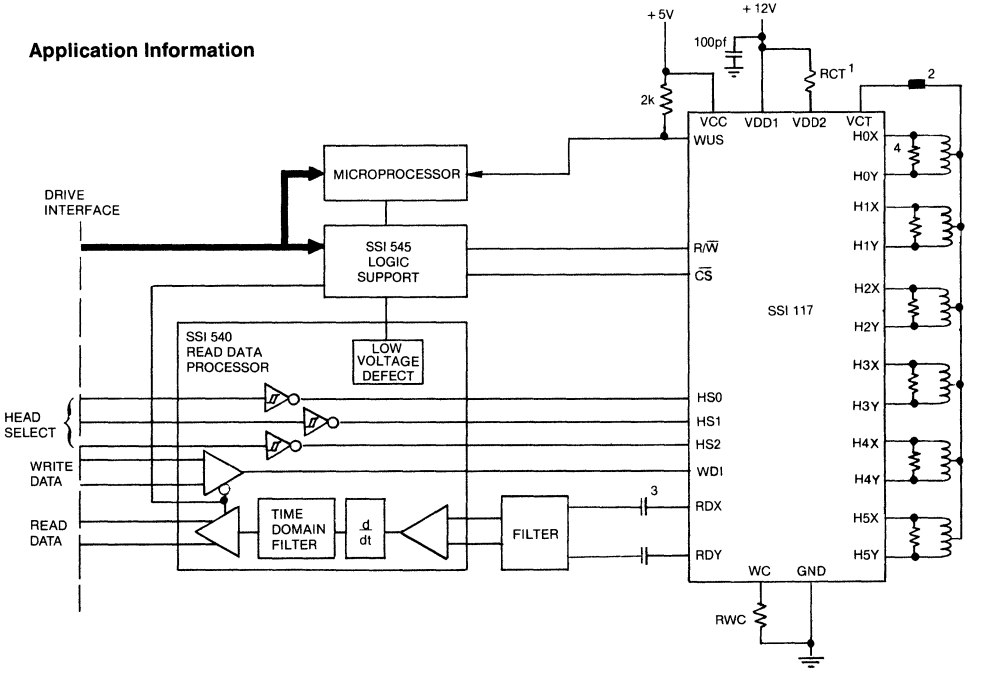
SWITCHING CHARACTERISTICS (cont'd)

Parameter		Test Conditions	Min.	Max.	Units
HS0 HS1 HS2	to any Head	Delay to 90% of 100mV 10MHz Read Signal Envelope	—	1.0	μS
WUS:	Safe to Unsafe – TD1 Unsafe to Safe – TD2	Iw = 50mA Iw = 20mA	1.6 —	8.0 1.0	μS μS
Head Current: Prop. Delay – TD3		Lh = 0μH, Rh = 0Ω From 50% Points	—	25	nS
Asymmetry		WDI has 50% Duty Cycle and 1ns Rise/Fall Time	—	2	nS
Rise/Fall Time		10% — 90% Points	—	20	nS



WRITE MODE TIMING DIAGRAM

Application Information



Note 1 An external 1/2 watt resistor, RCT, given by

RCT = 130(55/Iw) ohms, where Iw is in mA

can be used to limit internal power dissipation Otherwise connect VDD2 to VDD1

Note 2 A ferrite bead (Ferroxcube 5659065/4A6) can be used to suppress write current overshoot and ringing induced by flex cable parasitics

Note 3 Limit DC current from RDX and RDY to 100μA and load capacitance to 20pF

Note 4 Damping resistors not required on 117R version

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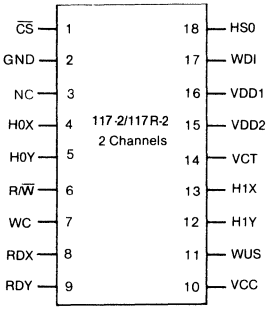
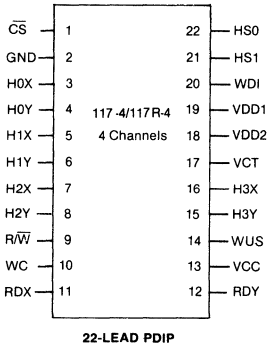
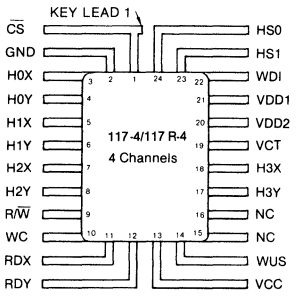
SSI 117A Pin Assignments



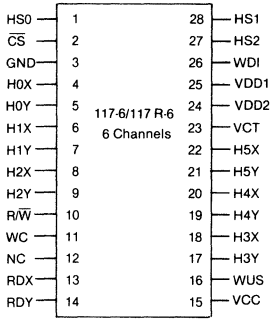
18-LEAD PDIP



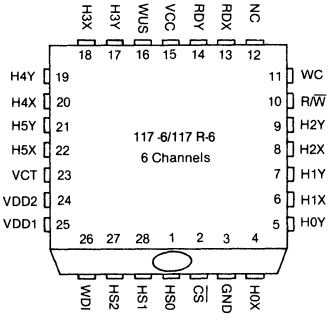
22-LEAD PDIP



24-LEAD FLAT PACK



28-LEAD PDIP, FLAT PACK



28-LEAD PLCC (QUAD)

THERMAL CHARACTERISTICS: θ_{JA}

18-LEAD	
PDIP	100°C/W
22-LEAD	
PDIP	90°C/W
24-LEAD	
FLAT PACK	60°C/W
28-LEAD	
PDIP	80°C/W
FLAT PACK	TBD
PLCC	50°C/W

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SSI 117A/117AR– Series 2, 4, or 6-Channel Read/Write Circuits

Data Sheet

GENERAL DESCRIPTION

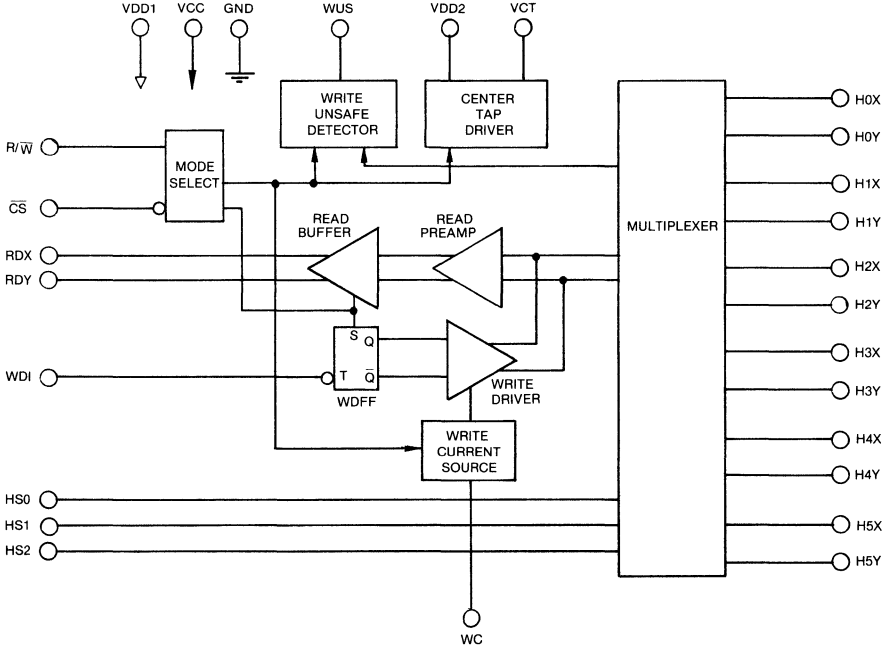
The SSI 117A devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as six channels. The SSI 117A requires +5V and +12V power supplies and is available in 2, 4, or 6 channel versions with a variety of packages.

The SSI 117AR differs from the SSI 117A by having internal damping resistors.

FEATURES

- **+5V, +12V power supplies**
- **Single- or multi-platter Winchester drives**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Available in 2, 4, or 6 channels**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**

SSI 117A Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

Circuit Operation

The SSI 117A functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables 2 & 3. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the SSI 117A as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data Flip Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by

Iw = K/Rwc, where K = Write Current Constant

is set by the external resistor, Rwc, connected from pin WC to GND.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

READ MODE

In the Read mode the SSI 117A is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports.

Note that the internal write current source is deactivated for both the Read and the chip deselect mode. This eliminates the need for external gating of the write current source.

TABLE 1: PIN DESCRIPTIONS

Symbol	Name — Description
HS0 - HS2	Head Select: selects up to six heads
$\overline{CS}$	Chip Select: a low level enables device
R/$\overline{W}$	Read/Write: a high level selects Read mode
WUS	Write Unsafe: a high level indicates an unsafe writing condition
WDI	Write Data In: a negative transition toggles the direction of the head current
H0X - H5X H0Y - H5Y	X, Y head connections
RDX, RDY	X, Y Read Data: differential read signal out
WC	Write Current: used to set the magnitude of the write current
VCT	Voltage Center Tap: voltage source for head center tap
VCC	+5V
VDD1	+12V
VDD2	Positive power supply for the Center Tap voltage source
GND	Ground

TABLE 2: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 3: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	none

0 = Low level
1 = High level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND)

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD1 VDD2 VCC	−0.3 to +14 −0.3 to +14 −0.3 to +6	VDC VDC VDC
Digital Input Voltage Range	Vin	−0.3 to VCC +0.3	VDC
Head Port Voltage Range	VH	−0.3 to VDD +0.3	VDC
WUS Port Voltage Range	Vwus	−0.3 to +14	VDC
Write Current	IW	60	mA
Output Current: RDX, RDY VCT WUS	Io	−10 −60 +12	mA mA mA
Storage Temperature Range Junction Temperature Range Lead Temperature (10 sec Soldering)	Tstg Tj	−65 to +150 +25 to +125 260	°C °C °C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD1 VDD2 VCC	12 ± 10% 6.5 to VDD1 5 ± 10%	VDC VDC VDC
Head Inductance	Lh	5 to 15	μH
Damping Resistor (117A only)	RD	500 to 2000	ohms
RCT Resistor	RCT	130 ± 5% (1/2 watt)	ohms
Write Current	IW	25 to 50	mA
RDX, RDY Output Current	Io	0 to 100	μA

DC CHARACTERISTICS Unless otherwise specified VDD1 = 12V ± 10%, VCC = 5V ± 10%, +25°C < Tj < +125°C.

Parameter	Test Conditions	Min.	Max.	Units
VCC Supply Current	Read / Idle Mode Write Mode	— —	25 30	mA mA
VDD Supply Current	Idle Mode Read Mode Write Mode	— — —	25 50 30 + IW	mA mA mA
Power Dissipation	Tj = +125°C Idle Mode Read Mode Write Mode, IW = 50mA, RCT = 130Ω Write Mode, IW = 50mA, RCT = 0Ω	 — — — —	 400 600 700 1050	 mW mW mW mW
Digital Inputs: Input Low Voltage (V_{IL}) Input High Voltage (V_{IH}) Input Low Current Input High Current	 V_{IL} = 0.8V V_{IH} = 2.0V	 −0.3 2.0 −0.4 —	 0.8 VCC + 0.3 — 100	 VDC VDC mA μA
WUS Output V_{OL} I_{OH}	I_{OL} = 8mA V_{OH} = 5.0V	— —	0.5 100	VDC μA
Center Tap Voltage (V_{CT})	Read Mode Write Mode	4.0 (typ) 6.0 (typ)		VDC VDC

WRITE CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, IW = 45mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz, CL (RDX, RDY) ≤20pF.

Parameter	Test Conditions		Min.	Max.	Units
Write Current Range			10	50	mA
Write Current Constant "K"			133	147	V
Differential Head Voltage Swing			8	—	V (pk)
Unselected Head Transient Current			—	2	mA (pk)
Differential Output Capacitance			—	15	pF
Differential Output Resistance		117A	10K	—	Ω
		117AR	638	863	Ω
WDI Transition Frequency	WUS = low		125	—	KHz
Iwc to Head Current Gain			20 (typ)		—
Unselected Head Leakage	VCT = 6V Sum of X & Y Side Leakage Current		—	85	μA

READ CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, IW = 45mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz, CL (RDX, RDY) ≤20pF. (Vin is referenced to VCT)

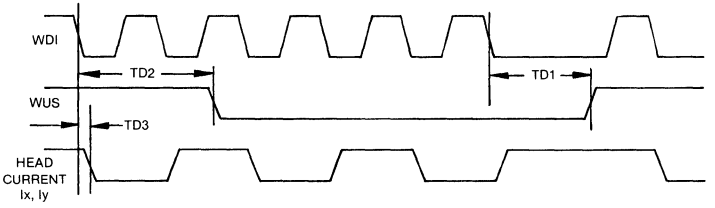
Parameter	Test Conditions		Min.	Max.	Units
Differential Voltage Gain	Vin = 1mVpp @ 300kHz RL (RDX), RL (RDY) = 1kohm		90	110	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5mVpp @ 300kHz		−3	3	mV
Bandwidth (−3db)	|Zs| < 5Ω, Vin = 1mVpp		30	—	MHz
Input Noise Voltage	BW = 15MHz, Lh = 0, Rh = 0		—	1.7	nV/√Hz
Differential Input Capacitance	f = 5MHz		—	20	pF
Differential Input Resistance	f = 5 MHz	117A	2K	—	Ω
		117AR	450	750	Ω
Input Bias Current (per side)			—	45	μA
Common Mode Rejection Ratio	Vcm = VCT + 100mVpp @ 5MHz		50	—	db
Power Supply Rejection Ratio	100mVpp @ 5MHz on VDD1, VDD2, or VCC		45	—	db
Channel Separation	Unselected Channels: Vin = 100mVpp @ 5MHz and Selected Channel: Vin = 0mVpp		45	—	db
Output Offset Voltage			−440	+440	mV
Common Mode Output Voltage		Read Mode	5	7	V
		Write/Idle Mode	4.3 typ		V
Single Ended Output Resistance	f = 5MHz		—	30	Ω
RDX, RDY Leakage Current	RDX, RDY = 6V Write/Idle Mode		−100	100	μA
Output Current	AC Coupled Load RDX to RDY		2	—	mA

SWITCHING CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, Tj = 25°C, IW = 45mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz.

Parameter		Test Conditions	Min.	Max.	Units
R/$\overline{W}$:	R/$\overline{W}$ to Write	Delay to 90% of Write Current	—	1.0	μS
	R/$\overline{W}$ to Read	Delay to 90% of 100mV 10MHz Read Signal Envelope or to 90% Decay of Write Current	—	1.0	μS
$\overline{CS}$:	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope	—	1.0	μS
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current	—	1.0	μS

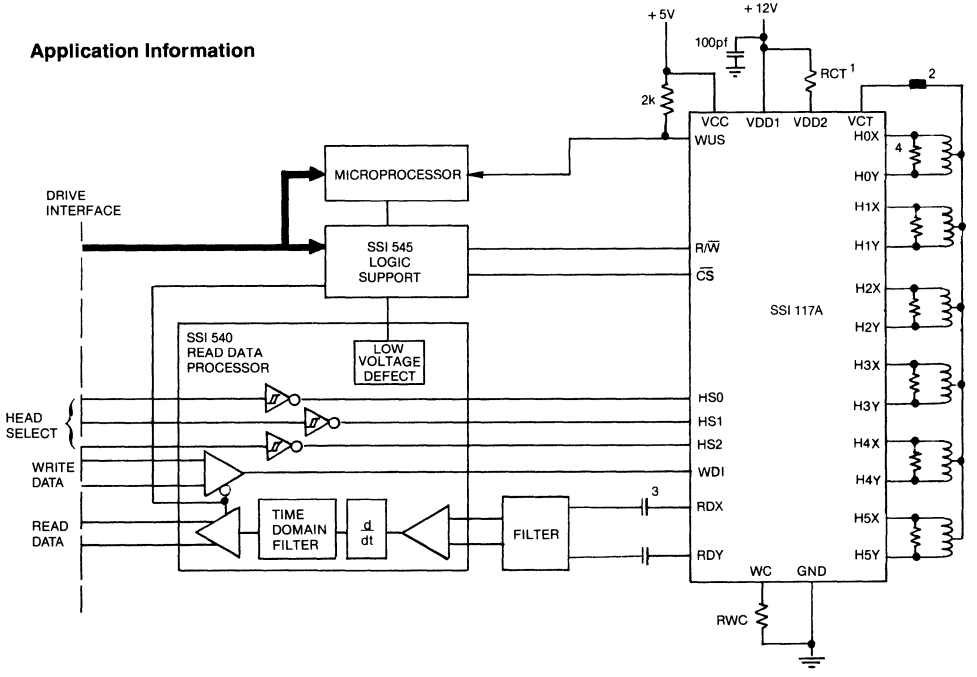
SWITCHING CHARACTERISTICS (cont'd)

Parameter	Test Conditions	Min.	Max.	Units
HS0 HS1 HS2 to any Head	Delay to 90% of 100mV 10MHz Read Signal Envelope	—	1.0	μS
WUS: Safe to Unsafe – TD1	Iw = 50mA	1.6	8.0	μS
Unsafe to Safe – TD2	Iw = 20mA	—	1.0	μS
Head Current:	Lh = 0μH, Rh = 0Ω			
Prop. Delay – TD3	From 50% Points	—	25	nS
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time	—	2	nS
Rise/Fall Time	10% — 90% Points	—	20	nS



WRITE MODE TIMING DIAGRAM

Application Information



Note 1 An external 1/2 watt resistor, RCT, given by

RCT = 130(55/Iw) ohms, where Iw is in mA

can be used to limit internal power dissipation Otherwise connect VDD2 to VDD1

Note 2 A ferrite bead (Ferroxcube 5659065/4A6) can be used to suppress write current overshoot and ringing induced by flex cable parasitics

Note 3 Limit DC current from RDX and RDY to 100μA and load capacitance to 20pF

Note 4 Damping resistors not required on 117R version

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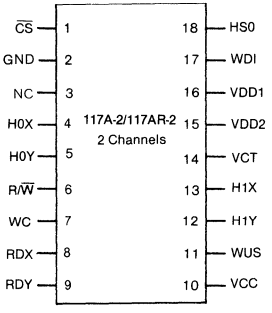
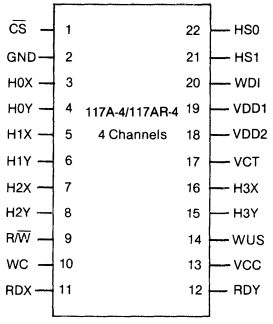
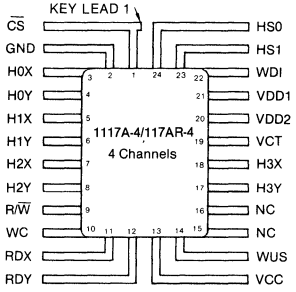
SSI 117A Pin Assignments



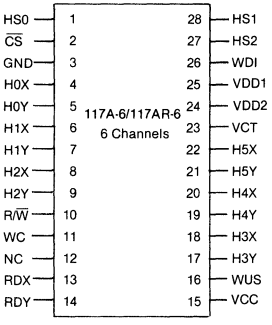
18-LEAD PDIP



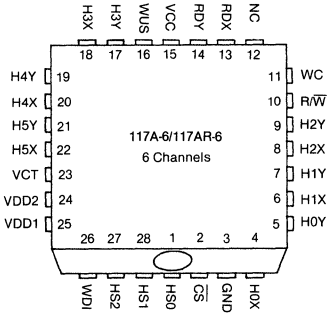
22-LEAD PDIP



24-LEAD FLAT PACK



28-LEAD PDIP, FLAT PACK



28-LEAD QUAD

THERMAL CHARACTERISTICS: θ_{JA}

18-LEAD	
PDIP	100°C/W
22-LEAD	
PDIP	90°C/W
24-LEAD	
FLAT PACK	60°C/W
28-LEAD	
PDIP	80°C/W
FLAT PACK	TBD
QUAD	50°C/W

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SSI 188
4-Channel Read/Write Circuit

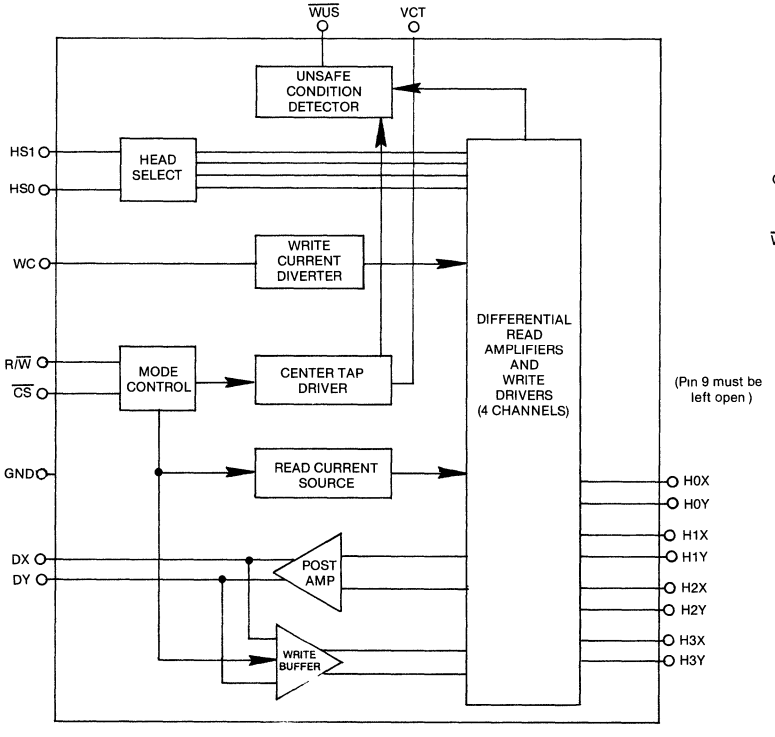
Preliminary Data Sheet

GENERAL DESCRIPTION

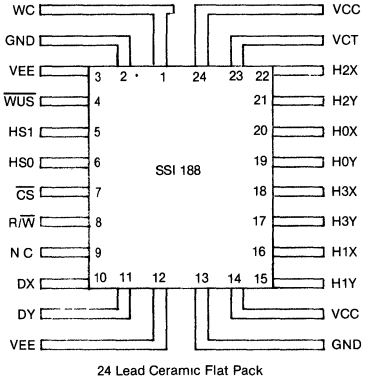
The SSI 188 is a high-performance, bipolar integrated read/write circuit for use with center tapped, ferrite heads. It provides a low noise read path, write control circuitry and data protection circuitry for 4 channels. The SSI 188 requires +6.5 V and −5.2 V power supplies. It is available in a 24 pin flat pack.

FEATURES

- **Fast switching characteristics**
- **TTL compatible control signals**
- **Four head capacity**
- **Designed for center-tapped ferrite heads**
- **Includes write unsafe detection**
- **Easily multiplexed**



Block Diagram



24 Lead Ceramic Flat Pack

Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

SSI 188
4-Channel
Read/Write Circuit

Circuit Operation

The SSI 188 has 3 selectable modes of operation as illustrated in Table 2. The R/$\overline{W}$ and $\overline{CS}$ inputs which determine these modes have internal resistor pullups to prevent an accidental write condition. Depending on the mode selected, the chip performs as a write gate or read amplifier for the selected head. Table 3 shows proper head addressing. In the Idle mode all inputs and outputs are in a high-impedance state, except the WC pin which is diverted to GND.

Write Mode

In this mode, externally supplied write current is gated to the "X" side of the chosen head when the DX input is low and to the "Y" side when DY is low. The write unsafe detector is activated when the SSI 188 is in the write mode. A low on the $\overline{WUS}$ pin indicates one of the following unsafe conditions:

- Head open or shorted
- No write current
- No write data transitions

During a normal write cycle the pin is initially low and then goes high after the differential input makes two transitions. Two transitions are also needed to clear $\overline{WUS}$ after a fault condition.

Read Mode

The SSI 188 amplifies the differential signal on the addressed head when in the read mode. The amplified signal is output on the open-collector DX and DY pins, with a gain dependent on external resistors tied from each pin to ground. The nominal values listed in this data sheet were obtained with 50 ohm resistors and can be doubled by using 100 ohm resistors. Polarity is such that the DX output is more positive when the "X" side of the head is more positive. External gating of the write current source is not necessary because an on-chip diverter circuit prevents the write current from flowing in the head circuits during the read and idle modes.

Table 1: Pin Descriptions

Symbol	Name — Description
HSO - HS1	Head Select: selects up to four heads
$\overline{CS}$	Chip Select: a low level enables device
R/$\overline{W}$	Read/Write: a high level selects Read mode
$\overline{WUS}$	Write Unsafe: open collector output, low indicates unsafe condition

Table 1: Pin Descriptions

Symbol	Name — Description
HOX-H3X HOY-H3Y	X, Y head connections
DX, DY	X, Y Read/Write Data: differential read data in/write data out signal
WC	Write Current: External write current generator connected to this pin
VCT	Voltage Center Tap: voltage source for head center tap
VCC	+6.5V.
VEE	−5.2V.
GND	Ground

Table 2: Mode Select

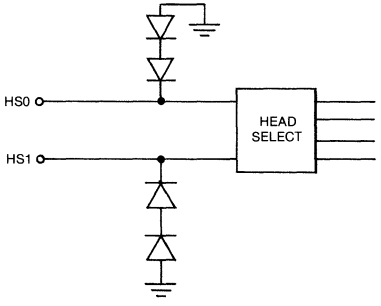
$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

Table 3: Head Select

HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

Temperature Monitoring

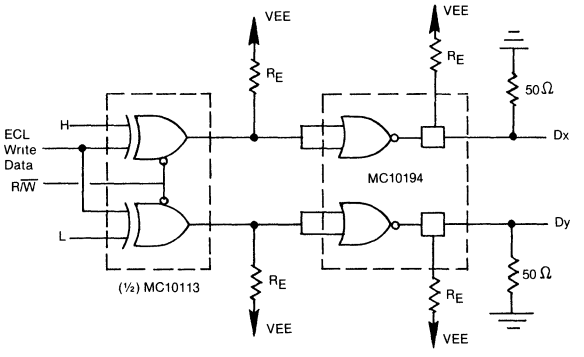
Two sets of series diodes are included on the chip for junction temperature monitoring. Between both the HS0 and HS1 pads to GND, two diodes are connected in series as shown in the figure below.

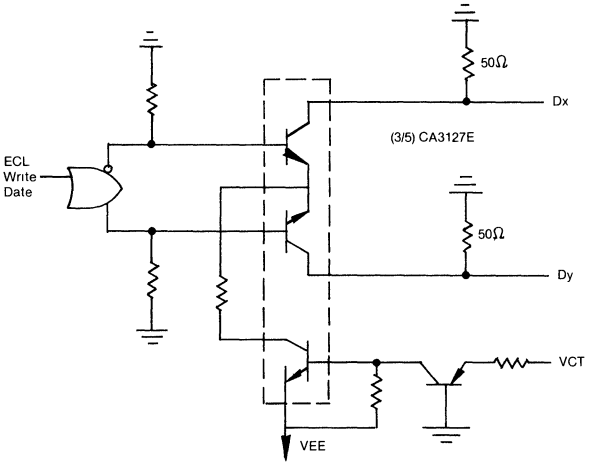


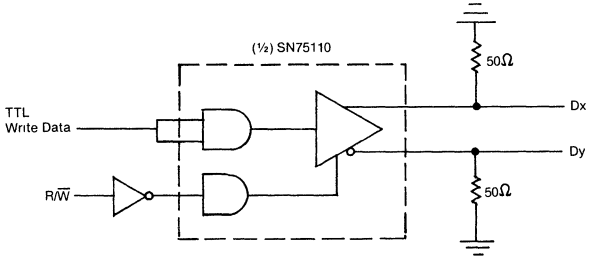
To calibrate the diodes remove power from the SSI 188, pull down on the HS0 or HS1 pin with a constant current and measure the diode forward bias voltage as the temperature is varied. To monitor temperature measure the diode forward bias voltage in either read or write mode and compare to the previously determined calibration curve.

Applications

These circuits are suggested for interfacing the differential DX and DY lines and either ECL or TTL data.







Absolute Maximum Ratings* (All voltages referenced to GND)

DC Supply Voltages (VCC)	7.5 V DC
(VEE)	−6.0 V DC
Digital Input Voltage Range	−0.3 to VCC + 0.3 V DC
Head Input (Read Mode)	−0.6 to 0.4 V DC
Head Select (HS0, HS1)	−0.4 V (or −2mA) to VCC + 0.3 V DC
$\overline{WUS}$ Port Voltage Range	−0.4 to VCC + 0.3 V DC
Write Current (Iw)	−80 mA
Output Currents (VCT)	−80 mA
($\overline{WUS}$)	10 mA
DX, DY Voltage	−0.1 to +0.3 V DC
Differential Voltage $\lvert V_{R/\overline{W}} - V_{\overline{CS}} \rvert$	6.5 V DC
Storage Temperature Range (Tstg)	−65 to +150 °C
Junction Temperature Range (Tj)	+25 to +125 °C
Lead Temperature (10 sec soldering)	260 °C

*Operation above these ratings may cause permanent damage to the device.

Recommended Operating Conditions

DC Supply Voltage	VCC VEE	6.5 ± 5% −5.2 ± 5%	VDC
Head Inductance	Lh	1.5 to 15	H
Write Current	Iw	35 to 70	mA

DC Characteristics Unless otherwise specified: VCC = 6.5 ± 5%, VEE = −5.2 ± 5%, +25°C < Tj < +125°C.

Parameter	Test Conditions	Min.	Max.	Units
VCC Supply Current	Read Mode Idle Mode Write Mode	— — —	80 35 40 + Iw	mA
VEE Supply Current	Idle Mode Read Mode Write Mode	−20 −75 −30	— — —	mA
Digital Inputs (HS0, HS1, R/$\overline{W}$, $\overline{CS}$) Input Low Voltage (V_{IL}) Input High Voltage (V_{IH}) Head Select: Input Low Current Input High Current Chip Select and Read/$\overline{Write}$: Input Low Current Input High Current	 — — V_{IL} = 0.8V V_{IH} = 2.0V V_{IL} = 0.8V V_{IH} = 2.0V	 — 2.0 −0.1 −0.1 −1.6 −1.4	 0.8 — 0.2 0.2 −0.1 −0.1	 VDC VDC mA mA mA mA
$\overline{WUS}$ Output V_{OL} I_{OH}	I_{OL} = 8mA V_{OH} = 5.0V	— −100	0.5 100	VDC μA
Center Tap Voltage (V_{CT})	Read Mode Write Mode	0.0 (typical) 4.2 (typical)		VDC

Write Characteristics Unless otherwise specified: VCC = 6.5 ± 5%, VEE = −5.2V ± 5%, Iw = 70mA, Lh = 1.8μH, Rd = 230 ohms

Parameter	Test Conditions	Min.	Max.	Units
Write Current Range	—	35	70	mA
Current Gain	Head Current/Iwc	0.95	1.01	—
Differential Head Voltage Swing	—	10.5	—	V(pk)
Unselected Diff. Head Current	—	—	3	mA (pk)
Data Input Capacitance	per side to GND	—	10	pF
Data Input Resistance	—	5	—	kΩ
WC Voltage	—	−4.5	−0.5	V
Differential Data Input Voltage	—	300	—	mV
Data Input Voltage Range	—	−0.8	+0.1	V
Data Input Current	per side	—	100	μA

Read Characteristics Unless otherwise specified: VCC = 6.5 ± 5%, VEE = −5.2V ± 5%, Lh = 1.8μH, Rd = 230Ω, f(Data) = 5MHz, RL (DX,DY) = 50Ω to GND (Vin is referenced to VCT)

Parameter	Test Conditions	Min.	Max.	Units
Differential Voltage Gain	Vin = 1mVpp @ 300 kHz	25	60	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5mVpp @ 300kHz	−2	2	mV
Bandwidth (−3db)	I Zs I< 5Ω , Vin = 1mVpp	48	—	MHz
Input Noise Voltage	Bw = 15 MHz, Vin = 0.0 VDC, Lh = 0, Rh = 0 Lh = 0, Rh = 115Ω per side	— —	2.4 3.3	nV/√Hz nV/√Hz
Differential Input Capacitance	Vin = 0.0 VDC	—	18	pF
Differential Input Resistance	V = 0.0 VDC	1.5	—	kΩ
Input Bias Current (per side)	Vin = 0.0 VDC	—	100	μA
Common Mode Rejection Ratio	Vcm = 100mVpp @ 12MHz	45	—	dB
Power Supply Rejection Ratio	100mVpp on VCC or VEE	45	—	dB
Channel Separation	Unselected Channels: Vin = 100mVpp @ 12MHz and Selected Channel: Vin = 0mVpp	34	—	dB
Input Offset Voltage	—	−10	+10	mV
Common Mode Output Voltage	—	−1.3	−0.2	V
Single Ended Output Resistance	—	5	—	kΩ
Single Ended Output Capacitance	—	—	10	pF
WC Voltage	IWC = 70mA	−3.2	−0.4	VDC
Total Head Input Current (IVCT)	IWC = 0	−500	+500	μA

Switching Characteristics Unless otherwise specified; VCC = 6.5 ± 5%, VEE = −5.2V ± 5%, Tj = 25°C, IW = 70mA, Lh = 1.8μH, Rd = 230Ω, f(Data) = 5MHz.

Parameter	Test Conditions	Min.	Max.	Units
R/$\overline{W}$: R/$\overline{W}$ to Write R/$\overline{W}$ to Read	Delay to 90% of Write Current Delay to 90% of 100mV 10MHz Read Signal Envelope or to 90% Decay of Write Current	— —	0.6 0.6	μS μS
$\overline{CS}$: $\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope	—	0.6	μS
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current	—	0.6	μS
HS0 HS1 to any Head HS2	Delay to 90% of 100mV 10MHz Read Signal Envelope	—	0.25	μS
$\overline{WUS}$: Safe to Unsafe — TD1 Unsafe to Safe — TD2	Iw = 70mA Iw = 35mA	0.4 —	4.0 1.0	μS
Head Current: Prop Delay — TD3 Asymmetry Rise/Fall Time	Lh = 0 H, Rh = 25 ohms per side From 50% Points 2 nS Max Input Switching 10% — 90% Points	— — —	19 2 15	nS nS nS

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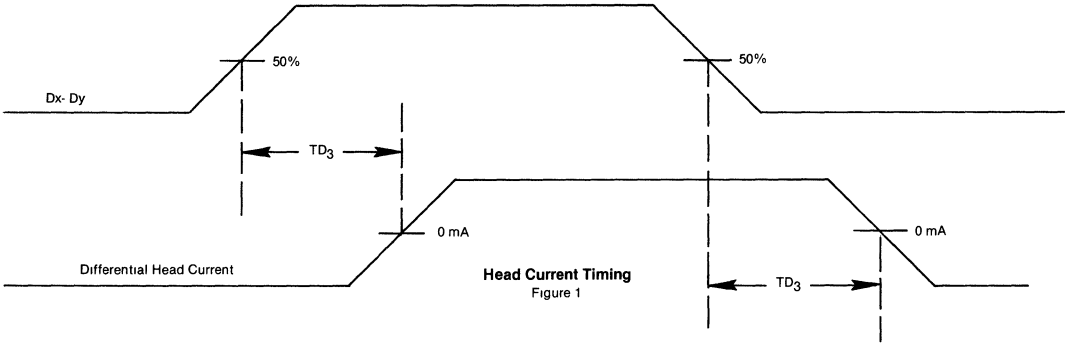
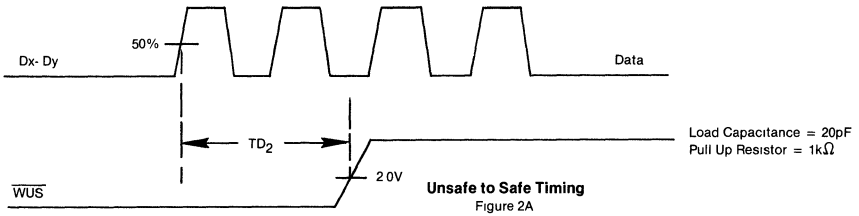
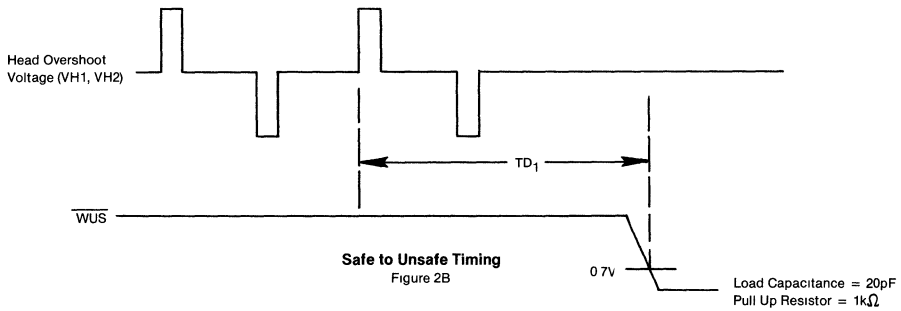
Timing Diagrams



Head Current Timing
Figure 1



Unsafe to Safe Timing
Figure 2A



Safe to Unsafe Timing
Figure 2B

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INNOVATORS IN INTEGRATION

SSI 501/501R 6 or 8 Channel Read/Write Circuit

Data Sheet

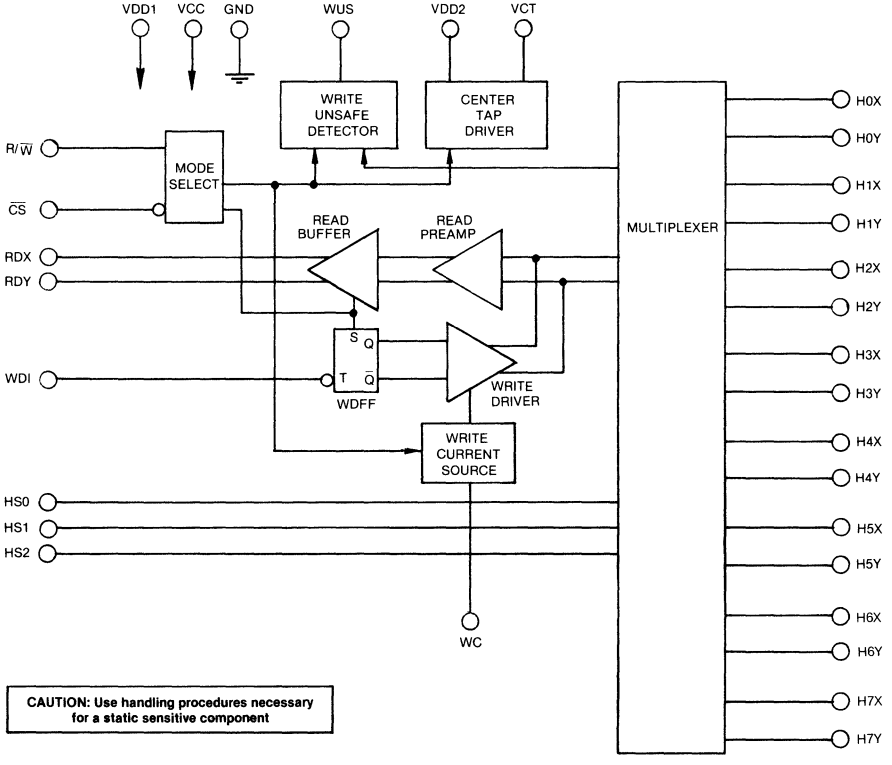
GENERAL DESCRIPTION

The SSI 501/501R devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for eight channels. The SSI 501/501R requires +5V and +12V power supplies and is available in a variety of packages. The SSI 501R differs from the SSI 501 by having internal damping resistors.

FEATURES

- **+5V, +12V power supplies**
- **Single- or multi-platter Winchester drives**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**

SSI 501/501R Block Diagram



Circuit Operation

The SSI 501/501R functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables 2 & 3. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the SSI 501/501R as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data Flip Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by

Iw = K/Rwc, where K = Write Current Constant

is set by the external resistor, Rwc, connected from pin WC to GND.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

READ MODE

In the Read mode the SSI 501/501R is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. They should be AC coupled to the load.

Note that the internal write current source is deactivated for both the Read and the chip deselect mode. This eliminates the need for external gating of the write current source.

TABLE 1: PIN DESCRIPTIONS

Symbol	Name — Description
HS0 - HS2	Head Select
$\overline{CS}$	$\overline{Chip\ Select}$: a low level enables device
R/$\overline{W}$	Read/$\overline{Write}$: a high level selects Read mode
WUS	Write Unsafe: a high level indicates an unsafe writing condition
WDI	Write Data In: a negative transition toggles the direction of the head current
H0X - H7X H0Y - H7X	X, Y head connections
RDX, RDY	X, Y Read Data: differential read signal out
WC	Write Current: used to set the magnitude of the write current
VCT	Voltage Center Tap: voltage source for head center tap
VCC	+5V
VDD1	+12V
VDD2	Positive power supply for the Center Tap voltage source
GND	Ground

TABLE 2: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 3: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low level
1 = High level

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND)

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD1 VDD2 VCC	−0.3 to +14 −0.3 to +14 −0.3 to +6	VDC VDC VDC
Digital Input Voltage Range	Vin	−0.3 to VCC +0.3	VDC
Head Port Voltage Range	VH	−0.3 to VDD +0.3	VDC
WUS Port Voltage Range	Vwus	−0.3 to +14	VDC
Write Current	IW	60	mA
Output Current: RDX, RDY VCT WUS	Io	−10 −60 +12	mA mA mA
Storage Temperature Range Junction Temperature Range Lead Temperature (10 sec Soldering)	Tstg Tj	−65 to +150 +25 to +135 260	°C °C °C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD1 VCC	12 ± 10% 5 ± 10%	VDC VDC
Head Inductance	Lh	5 to 15	μH
External Damping Resistor	RD (501 Only)	500 to 2000	ohms
RCT Resistor	RCT	120 ± 5% (1/2 watt)	ohms
Write Current	IW	22 to 50	mA

DC CHARACTERISTICS Unless otherwise specified VDD1 = 12V ± 10%, VCC = 5V ± 10%, +25°C ≤ Tj ≤ +135°C.

Parameter	Test Conditions	Min.	Max.	Units
VCC Supply Current	Read/Idle Mode Write Mode	— —	25 25	mA mA
VDD Supply Current	Idle Mode Read Mode Write Mode	— — —	20 35 20 + IW	mA mA mA
Power Dissipation	Tj = +135°C Idle Mode Read Mode Write Mode, IW = 50mA, RCT = 120Ω Write Mode, IW = 50mA, RCT = 0Ω	 — — — —	 400 600 760 1060	 mW mW mW mW
Digital Inputs: Input Low Voltage (V_{IL}) Input High Voltage (V_{IH}) Input Low Current Input High Current	 V_{IL} = 0.8V V_{IH} = 2.0V	 −0.3 2.0 −0.4 —	 0.8 VCC + 0.3 — 100	 VDC VDC mA μA
WUS Output V_{OL} I_{OH}	I_{OL} = 8mA V_{OH} = 5.0V	— —	0.5 100	VDC μA
Center Tap Voltage (V_{CT})	Read Mode Write Mode	4.0 (typ) 6.0 (typ)		VDC VDC

WRITE CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, +25°C ≤ Tj ≤ +135°C IW = 45mA, Lh = 10μH, Rd = 750Ω (SSI 501 only), f (Data) = 5MHz, CL (RDX, RDY) ≤20pF.

Parameter	Test Conditions		Min.	Max.	Units
Write Current Range			10	50	mA
Write Current Constant "K"			129	151	V
Differential Head Voltage Swing			7.5	—	V (pk)
Unselected Head Transient Current	5μH ≤ Lh ≤ 9.5 μH		—	2	mA (pk)
Differential Output Capacitance			—	15	pF
Differential Output Resistance		501	10K	—	Ω
		501R	560	940	
WDI Transition Frequency	WUS = low		125	—	KHz
Iwc to Head Current Gain			20 (typ)		—
Unselected Head Leakage	Sum of X & Y Side Current		—	85	μA

READ CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, IW = 45mA. +25°C ≤ Tj ≤ +135°C, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz, CL (RDX, RDY) ≤20pF. (Vin is referenced to VCT)

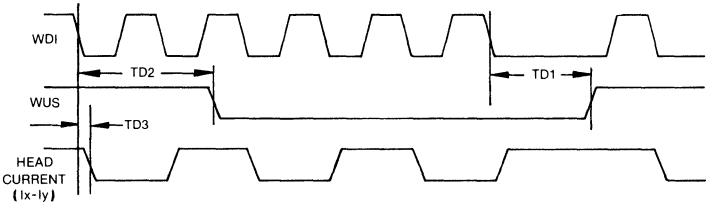
Parameter	Test Conditions		Min.	Max.	Units
Differential Voltage Gain	Vin = 1mVpp @ 300kHz RL (RDX), RL (RDY) = 1kohm (AC Coupled)		80	120	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5mVpp @ 300kHz		− 3	3	mV
Bandwidth (− 3db)	| Zs | < 5Ω, Vin = 1mVpp		30	—	MHz
Input Noise Voltage	BW = 15MHz, Lh = 0, Rh = 0		—	1.5	nV/√Hz
Differential Input Capacitance	f = 5MHz		—	23	pF
Differential Input Resistance	f = 5 MHz Vin ≤6mVpp	SSI 501	2K	—	Ω
		SSI 501R	530	790	Ω
Input Bias Current (per side)			—	100	μA
Common Mode Rejection Ratio	Vcm = VCT + 100mVpp @ 5MHz		50	—	db
Power Supply Rejection Ratio	100mVpp @ 5MHz on VDD1, VDD2, or VCC		45	—	db
Channel Separation	Unselected Channels: Vin = 100mVpp @ 5MHz and Selected Channel: Vin = 0mVpp		45	—	db
Output Offset Voltage			−480	480	mV
Common Mode Output Voltage		Read Mode	5	7	V
		Write/Idle Mode	4.3 (typ)		
Single Ended Output Resistance	f = 5MHz		—	30	Ω
External Resistive Load (AC Coupled to Output)	Per Side to GND		100	—	Ω
Leakage Current (RDX, RDY)	3.0 < RDX, RDY < 8.0V Write or Idle Mode		-50	50	μA
Center Tap Output Impedance	0 ≤ f ≤ 5 MHz		—	150	Ω
Output Current	AC Coupled Load RDX to RDY		2	—	mA

SWITCHING CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, +25°C ≤ Tj ≤ +135°C IW = 45mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz.

Parameter		Test Conditions	Min.	Max.	Units
R/$\overline{W}$:	R/$\overline{W}$ to Write	Delay to 90% of Write Current	—	600	nS
	R/$\overline{W}$ to Read	Delay to 90% of 100mV 10MHz Read Signal Envelope or to 90% Decay of Write Current	—	600	nS

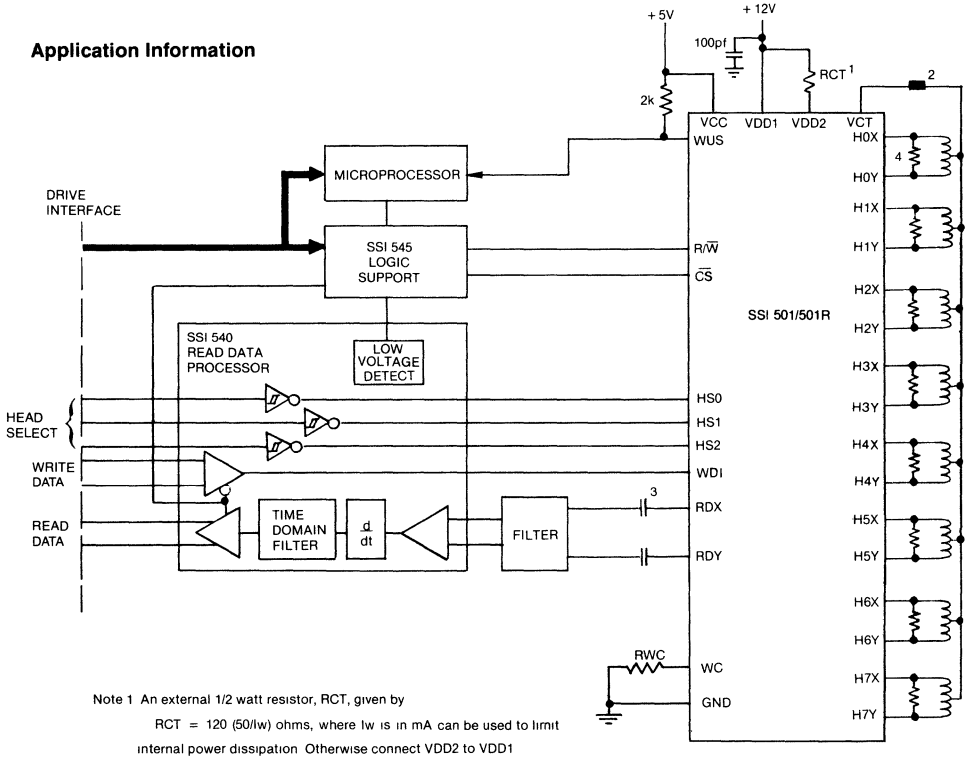
SWITCHING CHARACTERISTICS (cont'd)

Parameter		Test Conditions	Min.	Max.	Units
$\overline{CS}$:	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope	—	600	nS
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current	—	600	nS
HS0 HS1 HS2	to any Head	Delay to 90% of 100mV 10MHz Read Signal Envelope	—	600	nS
WUS:	Safe to Unsafe – TD1 Unsafe to Safe – TD2	Iw = 50mA Iw = 20mA	1.6 —	8.0 1.0	μS μS
Head Current:		Lh = 0μH, Rh = 0Ω			
	Prop. Delay – TD3	From 50% Points	—	30	nS
	Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time	—	2	nS
	Rise/Fall Time	10% — 90% Points	—	20	nS



WRITE MODE TIMING DIAGRAM

Application Information



Note 1 An external 1/2 watt resistor, RCT, given by

RCT = 120 (50/Iw) ohms, where Iw is in mA can be used to limit internal power dissipation Otherwise connect VDD2 to VDD1

Note 2 A ferrite bead (Ferroxcube 5659065/4A6) can be used to suppress write current overshoot and ringing induced by flex cable parasitics

Note 3 Limit DC current from RDX and RDY to 100uA and load capacitance to 20pF

Note 4 Damping resistors required on SSI 501 only

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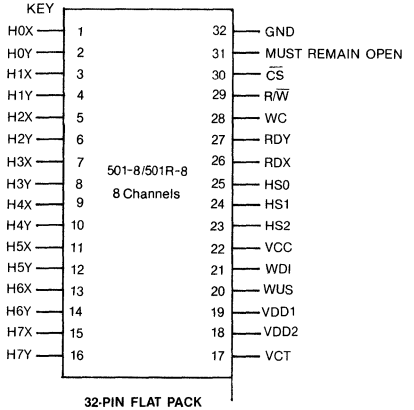
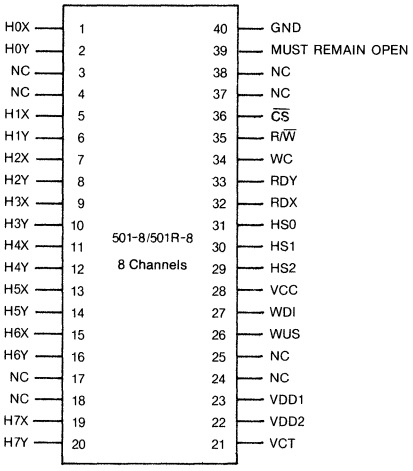
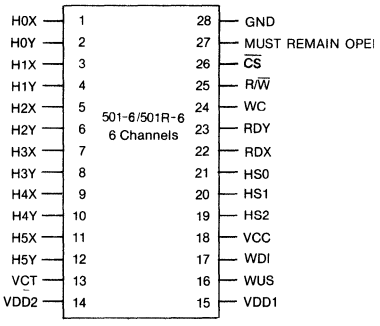
SSI 501/501R Pin Assignments



32-PIN FLAT PACK



40-LEAD CDIP, PDIP

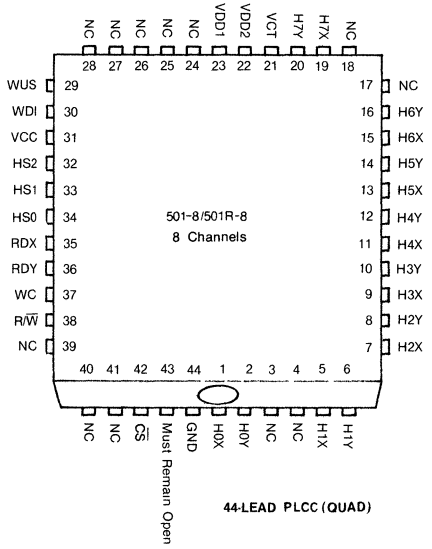


28-LEAD CDIP, PDIP

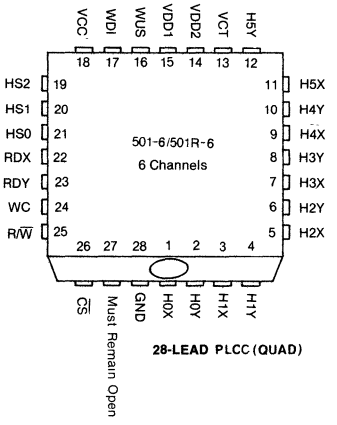
Note N/C pins have no external connection

THERMAL CHARACTERISTICS: θ_{JA}

28-LEAD		
	CDIP	52°C/W
	PDIP	80°C/W
	PLCC	50°C/W
32-LEAD	FLAT PACK	50°C/W
40-LEAD	CDIP	45°C/W
	PDIP	70°C/W
44-LEAD	PLCC	45°C/W



44-LEAD PLCC (QUAD)



28-LEAD PLCC (QUAD)

Notes All views are from top
NC pins have no internal connection

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INNOVATORS IN INTEGRATION

SSI 510/510R 4-Channel Read/Write Circuits

Preliminary Data Sheet

GENERAL DESCRIPTION

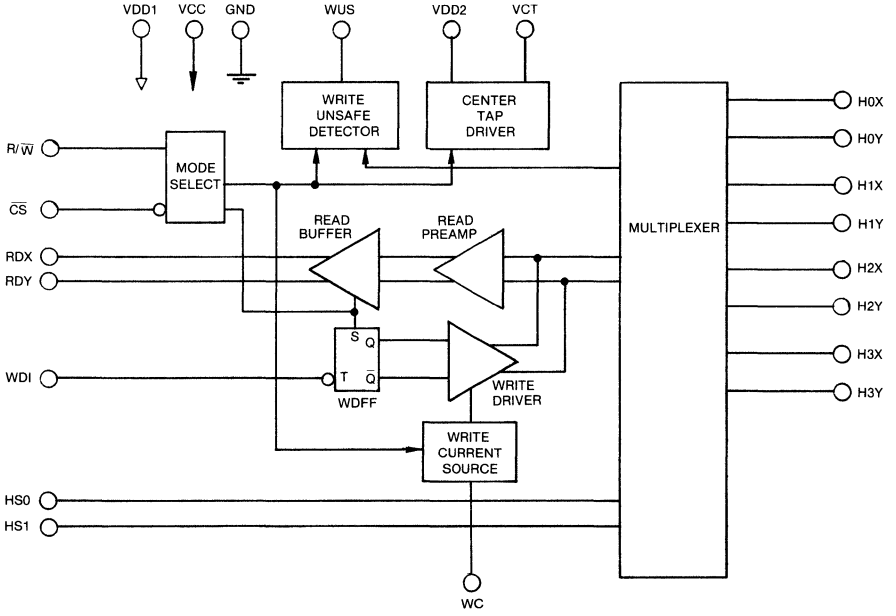
The SSI 510 devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as four channels. The SSI 510 requires +5V and +12V power supplies and is available in a variety of packages.

The SSI 510R differs from the SSI 510 by having internal damping resistors.

FEATURES

- **+5V, +12V power supplies**
- **Single- or multi-platter Winchester drives**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**

SSI 510 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

Circuit Operation

The SSI 510 functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables 2 & 3. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the SSI 510 as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data Flip Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by

Iw = K/Rwc, where K = Write Current Constant

is set by the external resistor, Rwc, connected from pin WC to GND.

A Voltage Fault detection circuit assures Data Security by preventing application of Write Current during power sequencing or power loss.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

READ MODE

In the Read mode the SSI 510 is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. They should be AC coupled to load.

Note that the internal write current source is deactivated for both the Read and the chip deselect mode. This eliminates the need for external gating of the write current source.

TABLE 1: PIN DESCRIPTIONS

Symbol	Name — Description
HS0 - HS1	Head Select
$\overline{CS}$	Chip Select: a low level enables device
R/$\overline{W}$	Read/Write: a high level selects Read mode
WUS	Write Unsafe: a high level indicates an unsafe writing condition
WDI	Write Data In: a negative transition toggles the direction of the head current
H0X - H3X H0Y - H3Y	X, Y head connections
RDX, RDY	X, Y Read Data: differential read signal out
WC	Write Current: used to set the magnitude of the write current
VCT	Voltage Center Tap: voltage source for head center tap
VCC	+5V
VDD1	+12V
VDD2	Positive power supply for the Center Tap voltage source
GND	Ground

TABLE 2: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 3: HEAD SELECT

HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

0 = Low level
1 = High level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND)

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD1 VDD2 VCC	−0.3 to +14 −0.3 to +14 −0.3 to +6	VDC VDC VDC
Digital Input Voltage Range	Vin	−0.3 to VCC +0.3	VDC
Head Port Voltage Range	VH	−0.3 to VDD +0.3	VDC
WUS Port Voltage Range	Vwus	−0.3 to +14	VDC
Write Current	IW	60	mA
Output Current: RDX, RDY VCT WUS	Io	−10 −60 +12	mA mA mA
Storage Temperature Range Junction Temperature Range Lead Temperature (10 sec Soldering)	Tstg Tj	−65 to +150 +25 to +125 260	°C °C °C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD1 VCC	12 ± 10% 5 ± 10%	VDC VDC
Head Inductance	Lh	5 to 15	μH
Damping Resistor (510 Only)	RD	500 to 2000	ohms
RCT Resistor	RCT	160 ± 5% (1/2 watt)	ohms
Write Current	IW	10 to 35	mA

DC CHARACTERISTICS Unless otherwise specified VDD1 = 12V ± 10%, VCC = 5V ± 10%, +25°C < Tj < +125°C.

Parameter	Test Conditions	Min.	Max.	Units
VCC Supply Current	Read/Idle Mode Write Mode	— —	25 30	mA mA
VDD Supply Current	Idle Mode Read Mode Write Mode	— — —	25 50 30 + IW	mA mA mA
Power Dissipation	Tj = +125°C Idle Mode Read Mode Write Mode, IW = 35mA, RCT = 160Ω Write Mode, IW = 35mA, RCT = 0Ω	 — — — —	 400 600 670 870	 mW mW mW mW
Digital Inputs: Input Low Voltage (V_{IL}) Input High Voltage (V_{IH}) Input Low Current Input High Current	 V_{IL} = 0.8V V_{IH} = 2.0V	 −0.3 2.0 −0.4 —	 0.8 VCC + 0.3 — 100	 VDC VDC mA μA
WUS Output V_{OL} I_{OH}	I_{OL} = 8mA V_{OH} = 5.0V	— —	0.5 100	VDC μA
Center Tap Voltage (V_{CT})	Read Mode Write Mode	4.0 (typ) 6.0 (typ)		VDC VDC
Head Current (per side)	Read or Idle Mode, $0 \leq V_{CC} \leq 5.5V$, $0 \leq V_{DD} \leq 13.2V$ Write Mode, $0 \leq V_{CC} \leq 3.4V$, $0 \leq VDD1 \leq 7.3V$	—	±100	μA

WRITE CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, +25°C ≤ Tj ≤ +125°C
IW = 35mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz, CL (RDX, RDY) ≤ 20pF.

Parameter	Test Conditions		Min.	Max.	Units
Write Current Range			10	35	mA
Write Current Constant "K"			106	118	V
Differential Head Voltage Swing			7.0	—	V (pk)
Unselected Head Transient Current			—	2	mA (pk)
Differential Output Capacitance			—	15	pF
Differential Output Resistance		510	10K	—	Ω
		510R	600	960	Ω
WDI Transition Frequency	WUS = low		125	—	KHz
Iwc to Head Current Gain			20 (typ)		—
Unselected Head Leakage Current	Sum of X & Y Side Current		—	85	μA

READ CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%,
IW = 35mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz, CL (RDX, RDY) ≤ 20pF.
(Vin is referenced to VCT), +25°C ≤ Tj ≤ +125°C

Parameter	Test Conditions		Min.	Max.	Units
Differential Voltage Gain	Vin = 1mVpp @ 300kHz RL (RDX), RL (RDY) = 1kohm		90	110	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5mVpp @ 300kHz		−2	2	mV
Bandwidth (−3db)	I Zs I < 5Ω, Vin = 1mVpp		30	—	MHz
Input Noise Voltage	BW = 15MHz, Lh = 0, Rh = 0		—	1.5	nV/√Hz
Differential Input Capacitance	f = 5MHz		—	20	pF
Differential Input Resistance	f = 5 MHz	510	2K	—	Ω
		510R	460	860	Ω
Input Bias Current (per side)			—	45	μA
Common Mode Rejection Ratio	Vcm = VCT + 100mVpp @ 5MHz		50	—	db
Power Supply Rejection Ratio	100mVpp @ 5MHz on VDD1, VDD2, or VCC		45	—	db
Channel Separation	Unselected Channels: Vin = 100mVpp @ 5MHz and Selected Channel: Vin = 0mVpp		45	—	db
Output Offset Voltage			−440	+440	mV
Common Mode Output Voltage		Read Mode	5	7	V
		Write/Idle Mode	4.3 (typ)		V
Single Ended Output Resistance	f = 5MHz		—	30	Ω
Leakage Current RDX, RDY	RDX, RDY = 6V, Write/Idle Mode		−100	100	μA
Output Current	AC Coupled Load, RDX to RDY		2.1	—	mA

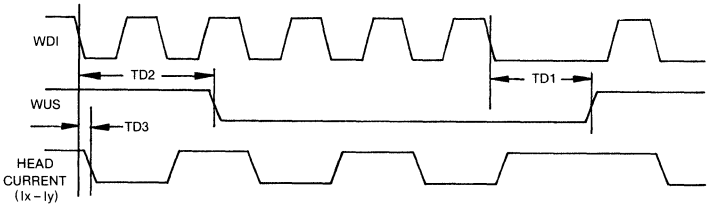
SWITCHING CHARACTERISTICS Unless otherwise specified: VDD1 = 12V ± 10%, VCC = 5V ± 10%, Tj = 25°C,
IW = 35mA, Lh = 10μH, Rd = 750Ω, f (Data) = 5MHz, +25°C ≤ Tj ≤ +125°C

Parameter		Test Conditions	Min.	Max.	Units
R/$\overline{W}$:	R/$\overline{W}$ to Write	Delay to 90% of Write Current	—	1.0	μS
	R/$\overline{W}$ to Read	Delay to 90% of 100mV 10MHz Read Signal Envelope or to 90% Decay of Write Current	—	1.0	μS
$\overline{CS}$:	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope	—	1.0	μS
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current	—	1.0	μS

(cont.)

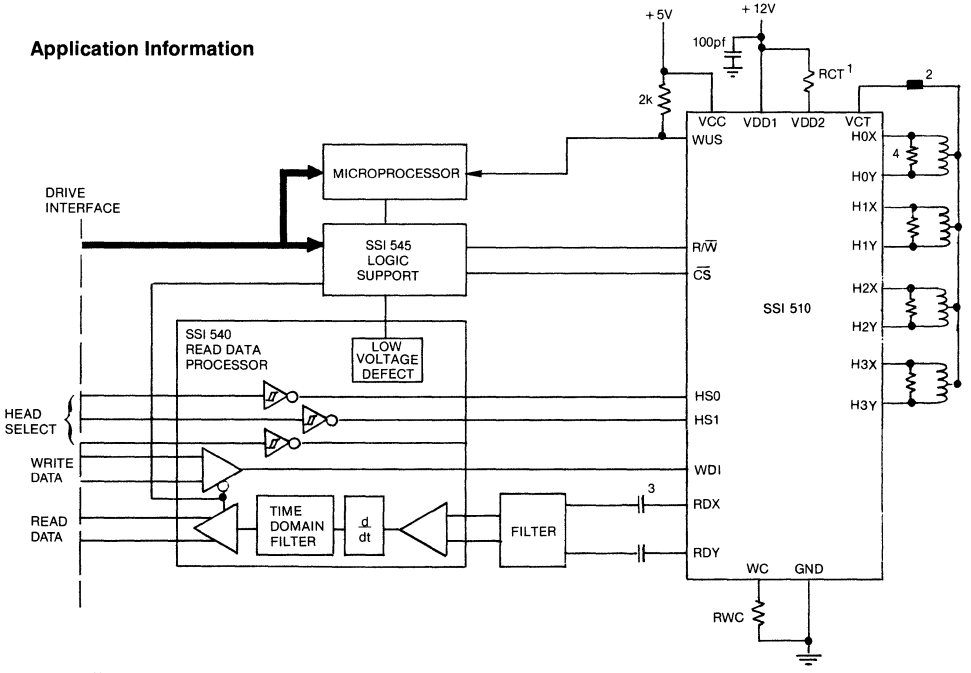
SWITCHING CHARACTERISTICS (cont'd)

Parameter		Test Conditions	Min.	Max.	Units
HS0 HS1 HS2	to any Head	Delay to 90% of 100mV 10MHz Read Signal Envelope	—	1.0	μS
WUS:	Safe to Unsafe – TD1 Unsafe to Safe – TD2	Iw = 35mA	1.6 —	8.0 1.0	μS μS
Head Current: Prop. Delay – TD3 Asymmetry Rise/Fall Time		Lh = 0μH, Rh = 0Ω From 50% Points WDI has 50% Duty Cycle and 1ns Rise/Fall Time 10% — 90% Points	— — —	25 2 20	nS nS nS



WRITE MODE TIMING DIAGRAM

Application Information



Note 1 An external 1/2 watt resistor, RCT, given by

RCT = 130(55/Iw) ohms, where Iw is in mA

can be used to limit internal power dissipation Otherwise connect VDD2 to VDD1

Note 2 A ferrite bead (Ferroxcube 5659065/4A6) can be used to suppress write current overshoot and ringing induced by flex cable parasitics

Note 3 Limit DC current from RDX and RDY to 100uA and load capacitance to 20pF

Note 4 Damping resistors not required on SSI 510R version

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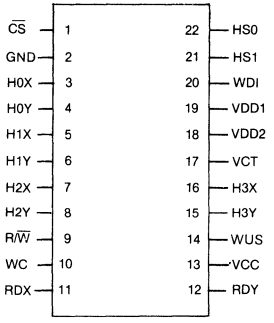
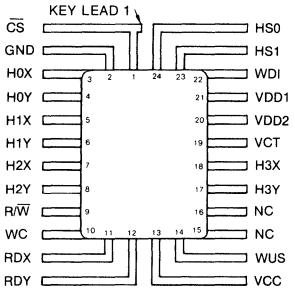
SSI 510 Pin Assignments



22-LEAD PDIP



24-LEAD FLAT PACK

THERMAL CHARACTERISTICS: θ_{JA}

24-LEAD FLAT PACK	60°C/W
22-LEAD PDIP	90°C/W

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SSI 520/520R
Thin Film - 4-Channel Read/Write Circuit

Preliminary Data Sheet

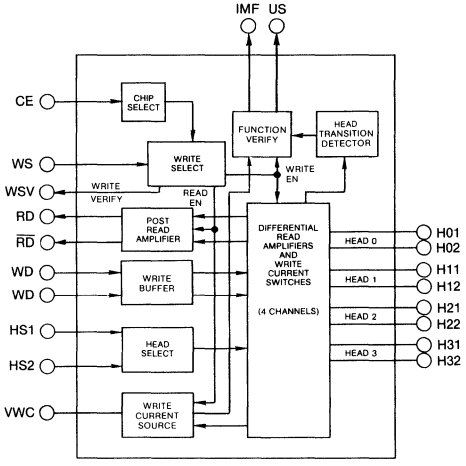
DESCRIPTION

The SSI 520 is an integrated read/write circuit designed for use with non-center tapped thin film heads in disk drive systems. Each chip controls four heads and has three modes of operation: read, write, and idle. The circuit contains four channels of read amplifiers and write drivers and also has an internal write current source.

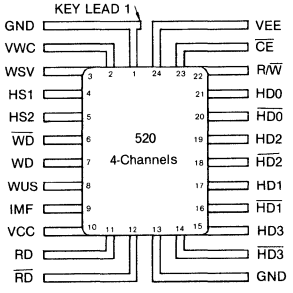
A current monitor (IMF) output is provided that allows a multichip enable fault to be detected. An enabled chip's output will produce one unit of current. An open collector output, write select verify (WSV), will go low if the write current source transistor is forward biased. The circuit operates on +5 volt, and −5 volt power and is available in a 24 pin flatpack. The SSI 520R differs from the SSI 520 by having internal damping resistors.

FEATURES

- **Thin film head compatible performance**
- **Four Read/Write Channels**
- **TTL - compatible logic levels**
- **Operates on standard +5 volt and −5 volt power supplies**



SSI 520 Block Diagram



SSI 520 Pin Out

CAUTION: Use handling procedures necessary for a static sensitive component

SSI 520/520R
Thin Film - 4-Channel
Read/Write Circuit

CIRCUIT DESCRIPTION

WRITE MODE

In the write mode (R/$\overline{W}$ and CE low) the circuit functions as a differential current switch. The Head Select inputs (HS1 and HS2) determine the selected head. The Write Data Inputs (WD, $\overline{WD}$) determine the polarity of the head current. The write current magnitude is adjustable by an external 1% resistor, R_{we}, to V_{EE}, where:

$$I_w = \frac{V_{wc}}{R_{wc}\left(1 + \frac{R_h}{R_d}\right)}$$

Where V_{wc} = Write Current Pin Voltage = 1.65 ± 5%
R_h = Head plus External Wire Resistance
R_d = Damping Resistance

READ MODE

In the Read Mode, (R/$\overline{W}$ high and CD low), the circuit functions as a differential amplifier. The amplifier input terminals are determined by the Head Select inputs.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage, V_{CC} 6V
Negative Supply Voltage, V_{EE} . . . . . – 6V
Operating Junction Temperature . . . . . 25 °C to 125 °C
Storage Temperature . . . . . – 65 °C to 150 °C
Lead Temperature (Soldering, 10 sec) . . . . . 260 °C
Input Voltages
Head Select (HS) . . . . . – 0.4V to V_{CC} + 0.3V
Chip Enable ($\overline{CE}$) . . . . . – 0.4V to V_{CC} + 0.3V
Read Select (R/$\overline{W}$) . . . . . – 0.4V or – 2mA to V_{CC} + 0.3V
Write Data (WD, $\overline{WD}$) . . . . . V_{EE} to 0.3V
Head Inputs (Read Mode) . . . . . – 0.6V to + 0.4V
Outputs
Read Data (RD, $\overline{RD}$) . . . . . 0.5V to V_{CC} + 0.3V
Write Unsafe (WUS), ... – 0.4V to V_{CC} + 0.3V and 20mA
Write Select Verify (WSV) . . . . . – 0.4V to V_{CC} + 0.3V and 20mA
Current Monitor (IMF) . . . . . – 0.4V to V_{CC} + 0.3V
Current Reference (VWC) . . . . . V_{EE} to V_{CC} + 0.3V and 8mA
Head Outputs (Write Mode) . . . . . I_w max = 150 mA
Thermal Characteristics
Flatpack Package . . . . . ΘJA = 144 °C/W(still air)
ΘJA = 30 °C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75 ≤ VCC ≤ 5.25, – 5.5 ≤ VEE ≤ – 4.95V, 25 ° ≤ T (junction) ≤ 125 °C.

POWER SUPPLY

Parameter	Test Conditions	Min.	Max.	Units
Power Dissipation	All modes, 25 ≤ T_j ≤ 100 100 ° ≤ T_j ≤ 125 °C	— —	612 + 6.7 Iw 563 + 6.7 Iw	mW mW
Positive Supply Current (ICC)	Idle Mode	—	10 + Iw/19	mA
Positive Supply Current (ICC)	Read Mode	—	40 + Iw/19	mA
Positive Supply Current (ICC)	Write Mode	—	38 + Iw/19	mA
Negative Supply Current (IEE)	Idle Mode	– 12 – Iw/19	—	mA
Negative Supply Current (IEE)	Read Mode	– 66 – Iw/19	—	mA
Negative Supply Current (IEE)	Write Mode	– 75 – 1.16Iw	—	mA

LOGIC SIGNALS

Parameter	Test Conditions	Min.	Max.	Units
Chip Enable Low Voltage (VLCE)	Read or Write Mode	—	0.8	V
Chip Enable High Voltage (VHCE)	Idle Mode	2.0	—	V
Chip Enable Low Current (ILCE)	VLCE = 0V	– 1.60	—	mA
Chip Enable High Current (IHCE)	VHCE = 2.0V	—	– 0.3	mA
Read Select High Voltage (VHR/W)	Read or Idle Mode	2.0	—	V
Read Select Low Voltage (VLR/W)	Write or Idle Mode	—	0.8	V
Read Select High Current (IHR/W)	VHR/W = 2.0V	—	0.015	mA
Read Select Low Current (ILR/W)	VLR/W = 0V	– 0.15	—	mA
Head Select High Voltage (VHHS)		2.0	—	V
Head Select Low Voltage (VLHS)		—	0.8	V

Head Selected	HS1	HS2
0	0	0
1	1	0
2	0	1
3	1	1

LOGIC SIGNALS

Parameter	Test Conditions	Min.	Max.	Units
Head Select High Current (IHHS)	VHHS = VCC	—	0.25	mA
Head Select Low Current (ILHS)	VLHS = 0V	−0.1	0.25	mA
WUS, WSV Low Level Voltage	ILUS = 8mA (denotes safe condition)	—	0.5	V
WUS, WSV High Level Current	VHUS = 5.0V (denotes unsafe condition)	—	100	μA
IMF ON Current		2.20	3.70	mA
IMF OFF Current		—	0.02	mA
IMF Voltage Range		0	VCC + 0.3	V

READ MODE Tests performed with 100Ω load resistors from RD and $\overline{RD}$ through series isolation diodes to VCC.

Parameter	Test Conditions		Min.	Max.	Units
Differential Voltage Gain	Vin = 1mVpp, f = 300kHz; 25°C ≤ Tj ≤ 125°C		75	170	V/V
	Tj = 70°C		85	150	
Voltage Bandwidth (−3dB)	Zs < 5Ω, Vin = 1mVpp f midband = 300kHz		45	—	MHz
Input Noise Voltage	Zs = 0Ω, Vin = 0V, Power Bandwidth = 15MHz		—	0.9	nV/√Hz
Differential Input Capacitance	Vin = 1mVpp, f = 5 MHz		—	65	pF
Differential Input Resistance	Vin = 1mVpp, f = 5 MHz	520	1K	—	Ω
		520R	130	270	
Input Bias Current (per side)	Vin = 0V		—	0.17	mA
Dynamic Range	DC input voltage where AC gain falls to 90% of the gain with .5mVpp input signal		−3.0	3.0	mV
CMRR	Vin = 100mVpp, 0V DC 1MHz ≤ f ≤ 10MHz 10MHz ≤ f ≤ 20MHz		 54 48	 — —	 dB dB
Power Supply Rejection Ratio	VCC or VEE = 100mVpp 1MHz ≤ f ≤ 10MHz 10MHz ≤ f ≤ 20MHz		 54 40	 — —	 dB dB
Channel Separation	The 3 unselected channels are driven with Vin = 100mVpp 1MHz ≤ f ≤ 10MHz 10MHz ≤ f ≤ 20MHz		 43 37	 — —	 dB dB
Output Offset Voltage			−360	360	mV
Output Leakage Current	Idle Mode		—	0.01	mA
Output Common Mode Voltage	(Without series isolation diodes)		VCC − 1.1	VCC − 0.3	V
Single Ended Output Resistance			10	—	KΩ
Single Ended Output Capacitance			—	10	pF

WRITE MODE

Parameter	Test Conditions	Min.	Max.	Units
Current Range (Iw)		30	75	mA
Current Tolerance	Current set to nominal value by Rx, Rh = 15Ω ± 10%, Tj = 50°C, Rd = 200Ω	−8	+8	%
(Iw) (Rh) Product		0.24	1.30	V
Differential Head Voltage Swing	Iw = 40 mA, Lh = 0.3μH, Rh = 15Ω	3.8	—	Vpp

WRITE MODE

Parameter	Test Conditions	Min.	Max.	Units
Unselected Head Transient Current	Iw = 40 mA, Lh = 0.3μH, Rh = 15Ω Non adjacent heads tested to minimize external coupling effects	—	2	mAp
Head Differential Load Resistance, Rd	520	1K	—	Ω
	520R 25°C ≤ Tj ≤ 125°C	130	270	Ω
	60°C ≤ Tj ≤ 120°C	140	260	
	Tj = 70°C	150	250	
Head Differential Load Capacitance		—	30	pF
Differential Data Voltage, (WD—$\overline{WD}$)		0.20	—	V
Data Input Voltage Range		−1.87	+0.1	V
Data Input Current (per side)	Chip Enabled	—	150	μA
Data Input Capacitance	per side to GND	—	10	pF

SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min.	Max.	Units
Idle to Read/Write Transition Time		—	1.0	μS
Read/Write to Idle Transition Time		—	1.0	μS
Read to Write Transition Time	VLCE = 0.8V, Delay to 90% of Iw	—	0.6	μS
Write to Read Transition Time	VLCE = 0.8V, Delay to 90% of 20MHz Read Signal envelope, Iw decay to 10%	—	0.6	μS
Head Select Switching Delay	Read or Write Mode	—	0.40	μS
Shorted Head Current Transition Time	Iw = 40mA, Lh < 0.05 μH, Rh = 0	—	13	nS
Shorted Head Current Switching Delay Time	Iw = 40mA, Lh < 0.05 μH, Rh = 0, measured from 50% of input to 50% of current change	—	18	nS
Head Current Switching Time Symmetry	Iw = 40mA, Lh = 0.2 μH, Rh = 10Ω, WD & $\overline{WD}$ transitions 2nS, switching time symmetry 0.2nS	—	1.0	nS
WSV Transition Time	Delay from 50% of write select swing to 90% of final WSV voltage, Load = 2KΩ // 20pF	—	1.0	μS
Unsafe to Safe Delay After Write Data Begins (WUS)	f(data) = 10MHz	—	1.0	μS
Safe to Unsafe Delay, (WUS)	Non-switching write data, no write current	0.6	3.6	μS
Safe to Unsafe Delay, (WUS)	Head open or head select input open	—	0.6	μS
IMF Switching Time	Delay from 50% of CE to 90% of final IMF current	—	1.0	μS

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SSI 521R
Thin Film-6-Channel Read/Write Circuit

Data Sheet

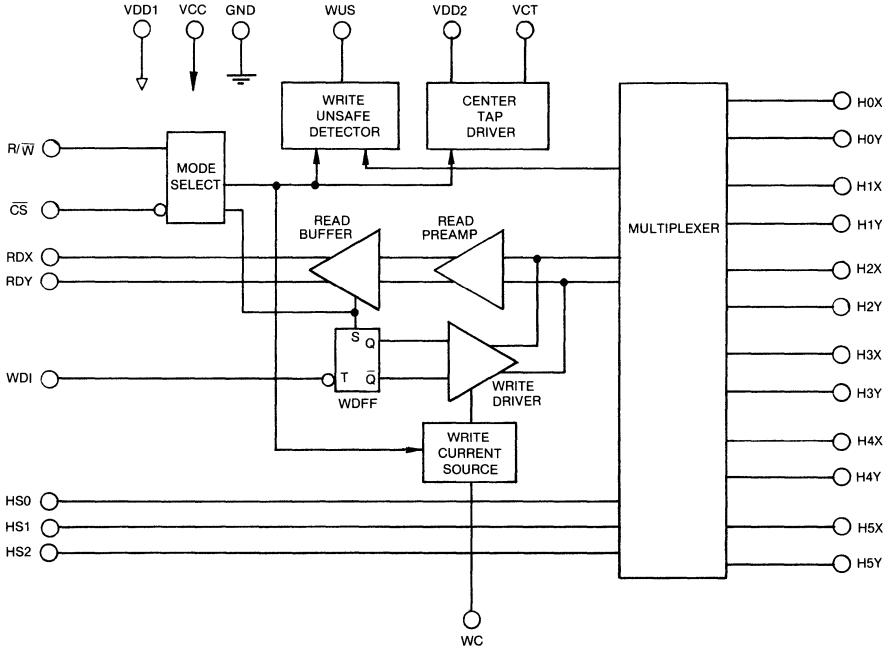
GENERAL DESCRIPTION

The SSI 521R is a bipolar monolithic integrated circuit designed for use with non-center tapped thin film recording heads. It provides a low noise read path, write current control, and data protection circuitry for up to six channels. The SSI 521R requires +5v and +12v power supplies and is available in a variety of packages.

FEATURES

- **Designed for thin film heads**
- **+5V, +12V power supplies**
- **Ideal for multi-platter Winchester applications**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **LSTTL compatible control signals**

SSI 521R Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

CIRCUIT OPERATION

The SSI 521R functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables 2 & 3. The inputs R/W, CS and WP have internal pull up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the SSI 521R as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-direction of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data flip flop to pass current in the X-direction of the head. The magnitude of the write current, given by

$$Iw = \frac{Vwc}{Rwc}$$

is controlled by an external resistor, Rwc, connected from pin WC to GND.

$$\text{Head Current } Ix, y = \frac{Iw}{1+Rh/Rd}$$

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open-only when Iw $\geq$ = 30ma
- WDI frequency too low
- Device in Read mode
- Chip disabled
- No write current

After fault condition is removed, two negative transitions on WDI are required to clear WUS. The current monitor output (IMF) sinks one unit of current when the device is selected. This allows a multichip enable fault to be detected.

READ MODE

In the Read mode, the SSI 521R is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip flop is set. The RDX and RDY outputs are driven by emitter followers. They should be AC coupled to the load.

Note that the internal write current source is deactivated for both the Read and the chip deselect mode.

TABLE 1: PIN DESCRIPTIONS

Symbol	Name - Description
HSO - HS2	Head Select: selects one of six heads
$\overline{CS}$	Chip Select: a high inhibits chip
R/$\overline{W}$	Read/Write: a high selects Read mode
WP	Write Protect: a low enables the write current source
WUS	Write Unsafe: a high indicates an unsafe writing condition
IMF	Current Monitor Function: allows multi-chip enable fault detection
WDI	Write Data In: changes the direction of the current in the recording head
HOX - H5X HOY - H5Y	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	X, Y Read Data: differential read data output
WC	Write Current: used to set the magnitude of the write current
VCC1	+5V Logic Circuit Supply
VCC2	+5V Write Current Supply
VDD	+12V
GND	Ground

TABLE 2: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 3: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	none
1	1	1	none

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD VCC	−0.3 to +14 −0.3 to +7	VDC VDC
Write Current	IW	100	ma
Digital Input Voltage	Vin	−0.3 to VCC+0.3	VDC
Head Port Voltage	VH	−0.3 to VDD+0.3	VDC
Output Current: RDX, RDY WUS	Io	−10 +12	ma ma
Storage Temperature	Tstg	−65 to +150	°C
Operating Temperature	Tj	+25 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Units
DC Supply Voltage	VDD	12 ±5%	VDC
	VCC1	5 ±5%	VDC
	VCC2	5 ±5%	VDC

DC CHARACTERISTICS Unless otherwise specified VDD=12V ±5% VCC1, 2=5V ±5%, +25° C<Tj< +125° C.

Parameter	Test Conditions	Min.	Max.	Units
VDD Supply Current	Read Mode	—	34	mA
	Write Mode	—	38	mA
	Idle Mode	—	9	mA
VCC Supply Current	Idle Mode	—	49	mA
	Read Mode	—	62	mA
	Write Mode	—	49 + IW	mA
Power Dissipation	Tj=+125 C	—		
	Idle Mode	—	400	mW
	Read Mode	—	800	mW
	Write Mode IW=50ma	—	1000	mW
DIGITAL INPUTS				
Input Low Voltage (VIL)		-0.3	0.8	VDC
Input High Voltage (VIH)		2.0	VCC+0.3	VDC
Input Low Current	VIL= 0.8v	-0.4		mA
Input High Current	VIH=2.0v	—	100	μA
RDX, RDY Common Mode Output Voltage		3	5	VDC
WUS Output VOL	Iol=8mA	—	0.5	VDC
IMF Output on		.72	1.5	mA
off		—	0.02	mA

WRITE CHARACTERISTICS Unless otherwise specified VDD=12V ±5%, VCC1,2=5V ±5%, IW=40mA, Lh=200nH, Rh=16Ω, f(Data)=5MHz, CL(RDX, RDY) <20pF, RL(RDX,RDY)=1KΩ. +25° C<Tj< +125° C.

Parameter	Test Conditions	Min.	Type	Max.	Units
Write Current Voltage Vwc	—		1.65 ±5%		V
Differential Head Voltage Swing	—	3.4	—	—	V (pk)
Unselected Head Current	—	—	—	2	mA (pk)
Differential Output Capacitance	—	—	—	30	pF
Differential Output Resistance	—	160	200	240	Ω
WDI Transition Frequency	WUS=low	1.7	—	—	MHz
Write Current Range	—	20	—	70	mA

READ CHARACTERISTICS Unless otherwise specified VDD=12V ±5%, VCC1,2=5V ±5%, +25° C<Tj< +125° C.

Parameter	Test Conditions	Min.	Max.	Units
Differential Voltage Gain	Vin=ImVpp @300kHz RL(RDX), RL (RDY)=1KΩ	75	125	V/V
Voltage BW -1db	|Zs|<5Ω, Vin=ImVpp @300kHz	25	—	MHz
-3db		45	—	MHz
Input Noise Voltage	BW=15MHz, Lh=0, Rh=0	—	0.9	$nV/\sqrt{Hz}$
Differential Input Capacitance	f=5MHz	—	.65	pF
Differential Input Resistance	f=5MHz	200 typ		Ω
Input Bias Current		—	170	μA

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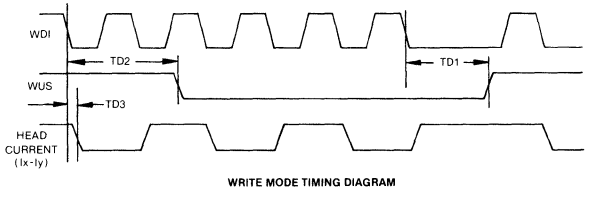
READ CHARACTERISTICS (cont.)

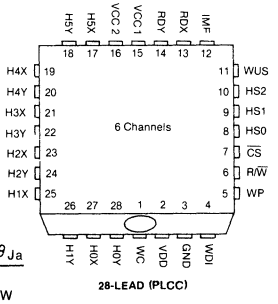
Parameter	Test Conditions	Min.	Max.	Units
Dynamic Range	DC input voltage where gain falls to 90% of its OVDC value. Vin=VDC +0.5 mVpp f=5 MHz	−3	3	mV
Common Mode Rejection Ratio	Vin=OVDC+100mVpp @5MHz	54	—	db
Power Supply Rejection Ratio	100mVpp @5MHz on VDD 100mVpp @ 5MHz on VCC	54	90 typ 49 typ	db
Channel Separation	Unselected channels driven with 100mVpp @5MHz Vin=OmVpp	45	—	db
Output Offset Voltage Single Ended Output Resistance	 f=5MHz	−360 —	360 30	mV Ω

SWITCHING CHARACTERISTICS Unless otherwise specified VDD=12V ±5% VCC1, 2=5V ±5%, TA=25° C, IW=40mA, Lh=200nH, Rh=16Ω, f(Data)=5MHz.

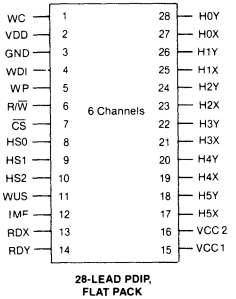
Parameter	Test Conditions	Min.	Max.	Units
R/W: R/W to Write R/W to Read	to 90% of write current to 90% of 100mV 10MHz Read signal envelope		0.6 0.6	μs μs
CS: CS to Select CS to Unselect	to 90% of write current or to 90% of 100mV 10MHz Read signal envelope		1 1	μs μs
HSO, 1,2 to any Head	to 90% of 100mV 10MHz Read signal envelope		0.4	μs
WUS: Safe to Unsafe TD1 Unsafe to Safe TD2		0.6	3.6 1	μs μs
IMF: Transition Time	delay from 50% point of CS to 90% of IMF current		0.6	μs
Head Current: WDI to (Ix-Iy) TD3 Asymmetry Rise/Fall Time	Lh=0, Rh=0 from 50% points WDI has 50% duty cycle and 1ns rise/fall time 10% - 90% points		 32 1.0 13	 ns ns ns



WRITE MODE TIMING DIAGRAM



28-LEAD (PLCC)



28-LEAD PDIP, FLAT PACK

THERMAL CHARACTERISTICS: θ_{Ja}

28-LEAD	
PDIP	80°C/W
FLAT PACK	90°C/W
(PLCC)	45°C/W

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SSI 101A Differential Amplifier

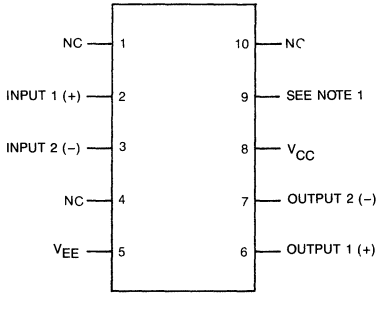
Data Sheet

GENERAL DESCRIPTION

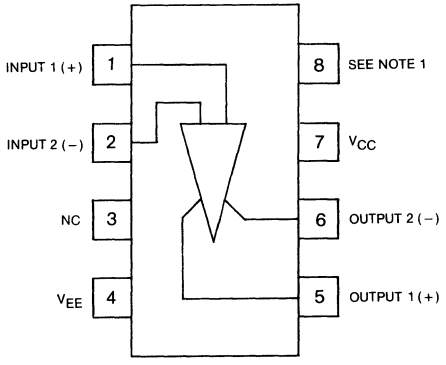
The SSI 101A is a two stage differential amplifier applicable for use as a preamplifier for the magnetic servo head circuit of Winchester technology disk drives.

FEATURES

- **Very narrow gain range**
- **30MHz bandwidth**
- **Electrically characterized at two power supply voltages: IBM Model 3340 compatible (8.3V) and standard OEM industry compatible (10V)**
- **Mechanically compatible with Model 3348 type head arm assembly**
- **SSI 101A-2 available to operate with a 12V power supply**
- **Packages include 8 pin DIP and custom 10-pin flatpack**



Flat Pack

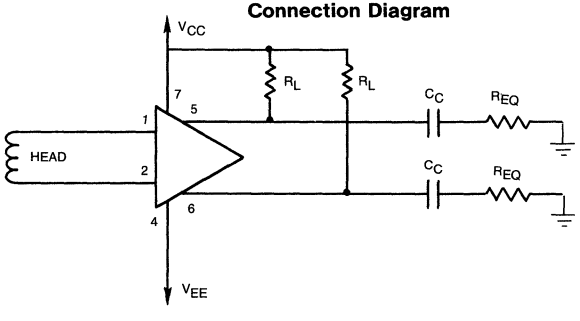


Plastic Dip

SSI 101A Pin Configuration (Top View)

NOTE 1 Pin must be left open and not connected to any circuit etch

Connection Diagram



Recommended Load Conditions

1. Input must be AC coupled
2. C_C's are AC coupling capacitors
3. R_L's are DC bias and termination resistors (recommended 130Ω)
4. R_{EQ} represents equivalent load resistance
5. For gain calculations $R_P = \frac{R_L \cdot R_{EQ}}{R_L + R_{EQ}}$
6. Differential gain = 0.72 R_p (±18%) (R_p in Ω)
7. Ceramic capacitors (0.1μf) are recommended for good power supply noise filtering

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Absolute Maximum Ratings

Power Supply Voltage (V_{CC}-V_{EE})..... 12V
SSI 101A-2..... 14V
Differential Input Voltage..... ±1V
Storage Temperature Range..... −65 °C to 150 °C
Operating Temperature Range..... 0 °C to 70 °C

ELECTRICAL CHARACTERISTICS T_A = 25 °C, (V_{CC}-V_{EE}) = 8.3V to 10V ±10% (12V ±10% for 101A-2)

Characteristics	Test Conditions	Min.	Typ.	Max.	Units
Gain (differential)	Rp = 130Ω	77	93	110	—
Bandwidth (3dB)	Vi = 2mVpp	10	20	—	MHz
Input Resistance		800	1000	1250	Ω
Input Capacitance		—	3	—	pF
Input Dynamic Range (Differential)	R_L = 130Ω	3	—	—	mVpp
Power Supply Current	(V_{CC}-V_{EE}) = 9.15V (V_{CC}-V_{EE}) = 11V (V_{CC}-V_{EE}) = 13.2V (101A-2)	—	26 30 35	35 40 45	mA
Output Offset (Differential)	Rs = O, R_L = 130Ω	—	—	600	mV
Equivalent Input Noise	Rs = O, R_L = 130Ω, BW = 4MHz	—	8	14	μV
PSRR, Input Referred	Rs = O, f ≤ 5MHz	50	65	—	dB
Gain Sensitivity (Supply)	△ (V_{CC}-V_{EE}) = ±10%, R_L = 130Ω	—	±1.3	—	%
Gain Sensitivity (Temp.)	T_A = 25 °C to 70 °C, R_L = 130Ω	—	−0.2	—	%/C
CMRR, Input Referred	f ≤ 5MHz	55	70	—	dB

Recommended Operating Conditions	Min.	Type	Max.	Units
Supply Voltage (V_{CC}-V_{EE})	7.45	8.3	9.15	V
	9.0	10.0	11.0	V
101A-2 only	10.8	12.0	13.2	V
Input Signal Vi	—	2	—	mVpp
Ambient Temp. T_A	0	—	70	C

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SSI 116 Differential Amplifier

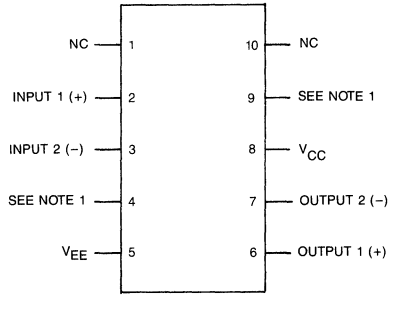
Data Sheet

GENERAL DESCRIPTION

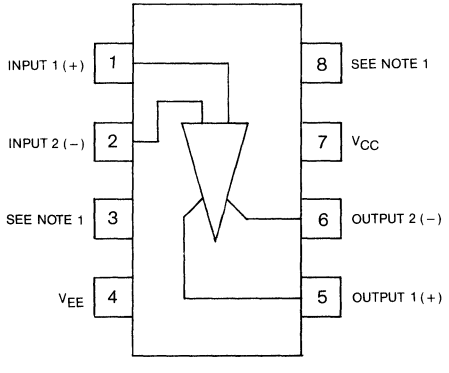
The SSI 116 is a high performance differential amplifier applicable for use as a preamplifier for the magnetic servo thin film head in Winchester disk drives.

FEATURES

- **Narrow gain range**
- **50MHz bandwidth**
- **IBM 3370/3380-compatible performance**
- **Operates on either IBM-compatible voltages (8.3V) or OEM-compatible (10V)**
- **Packages include 8-pin CERDIP or Plastic DIP and custom 10-pin flatpack.**
- **SSI 116-2 available to operate with a 12V power supply**



Flat Pack

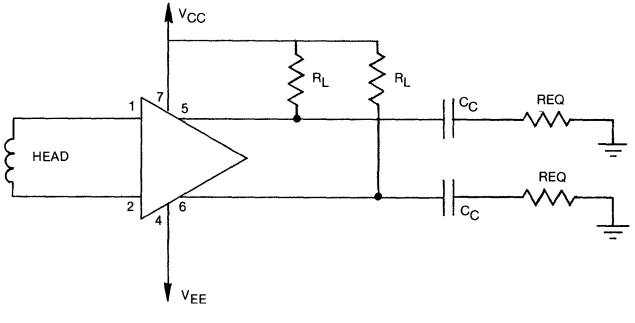


Cerdip
Plastic Dip

SSI 116 Pin Configuration (Top View)

NOTE 1 Pin must be left open and not connected to any circuit etch

Connection Diagram



Recommended Load Conditions

1. Input must be AC coupled
2. Cc's are AC coupling capacitors
3. R_L's are DC bias and termination resistors, 100 Ω recommended
4. REQ. represents equivalent load resistance
5. Ceramic capacitors (0.1 μF) are recommended for good power supply noise filtering

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Absolute Maximum Ratings

Power Supply Voltage (V_{CC}-V_{EE}).....12V
SSI 116-2.....14V
Operating Power Supply Range.....7.9V to 10.5V
SSI 116-2.....7.9V to 13.2V
Differential Input Voltage ..... ±1V
Storage Temperature Range..... −65 °C to 150 °C
Operating Ambient Temperature (T_A) .....15 °C to 60 °C
Operating Junction Temperature (T_J).....15 °C to 125 °C
Output Voltage.....V_{CC}−2.0V to V_{CC} +0.4V

ELECTRICAL CHARACTERISTICS Tj = 15 °C to 125 °C, (V_{CC}-V_{EE}) = 7.9V to 10.5V (to 13.2V for 116-2)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Gain (Differential)	Vin = 1mVpp, T_A = 25 °C, F = 1MHz	200	250	310	mV/mV
Bandwidth (3dB)	Vin = 1mVpp, C_L = 15pF	20	50	—	MHz
Gain Sensitivity (Supply)	—	—	—	1.0	%/V
Gain Sensitivity (Temp.)	15 °C < T_A < 55 °C	—	−0.16	—	%/C
Input Noise Voltage	Input Referred, R_S = 0	—	0.7	0.94	$nV/\sqrt{Hz}$
Input Capacitance (Differential)	Vin = 0, f = 5MHz	—	40	60	pF
Input Resistance (Differential)	—	—	200	—	Ω
Common Mode Rejection Ratio Input Referred	Vin = 100mVpp, f = 1MHz	60	70	—	dB
Input Signal Level	Common Mode	—	—	300	mVpp
Power Supply Rejection Ratio Input Referred	Vee + 100mVpp, f = 1MHz	46	52	—	dB
Input Dynamic Range (Differential	DC input voltage where AC gain is 90% of gain with 0.2mVpp input signal	—	—	±0.75	mV
Output Offset Voltage (Differential)	Vin = 0	−600	—	600	mV
Output Voltage (Common Mode)	Inputs shorted together and Outputs shorted together	V_{CC}−0.45	V_{CC}−0.6	V_{CC}−1.0	V
Single Ended Output Resistance	—	10	—	—	Ω
Single Ended Output Capacitance	—	—	—	10	pF
Power Supply Current	V_{CC}-V_{EE} = 9.15V V_{CC}-V_{EE} = 11V V_{CC}-V_{EE} = 13.2V 116-2 only	— — —	28 29 39	40 42 50	mA
Input DC Voltage	Common Mode	—	V_{EE}+2.6	—	V
Input Resistance	Common Mode	—	80	—	Ω

Recommended Operating Conditions	Min.	Type	Max.	Units
Supply Voltage (V_{CC}-V_{EE})	7.45	8.3	9.15	V
	9.0	10.0	11.0	V
116-2 only	10.8	12.0	13.2	V
Input Signal Vin	—	1	—	mVpp
Ambient Temp. T_A	15	—	65	°C

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SSI 531
Data Separator and Write Precompensation Circuit

Preliminary Data Sheet

GENERAL DESCRIPTION

The SSI 531 Data Separator performs data synchronization and write precompensation of encoded data. The interface of the SSI 531 is optimum for use with Western Digital's WD1010/WD2010 controller family.

The SSI 531 contains a high performance Phase Locked Loop for read data synchronization, a crystal controlled reference oscillator for write data synchronization, and write precompensation circuitry.

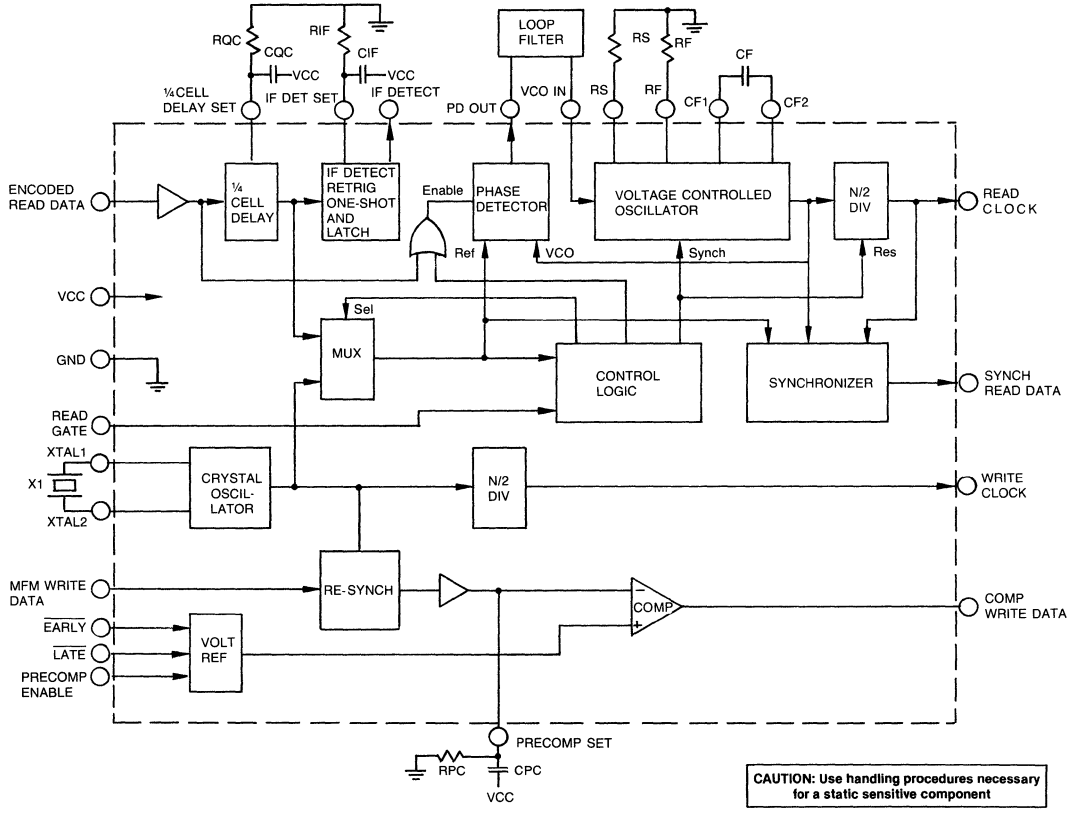
The SSI 531 employs an advanced bipolar technology which affords precise bit cell control without the need for external active components.

The SSI 531 requires a single +5V power supply and is available in 24-pin DIP and 28-pin PLCC packages.

FEATURES

- **MFM & RLL Data Synchronization.**
- **Optimized for use with the WD1010/WD2010 controller family.**
- **Fast acquisition Phase Locked Loop.**
- **1F detection.**
- **Write precompensation.**
- **Write data resynchronized for reduced jitter.**
- **No external delay line or varactor diode required.**
- **Single +5V power supply.**

SSI 531 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

SSI 531
Data Separator and Write Precompensation Circuit

CIRCUIT DESCRIPTION

Data Synchronization

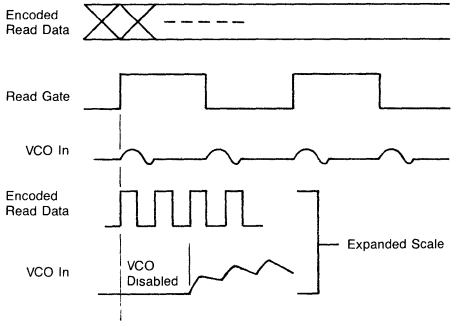
Read Data synchronization is accomplished with a high performance, fast acquisition Phase Locked Loop (PLL). The input from the disk drive, ENCODED READ DATA, is phase locked with the VCO clock. The synchronized Read Data and the VCO clock divided by two are made available for external data extraction at the SYNCH READ DATA and READ CLOCK pins respectively.

The synchronized Read Data is synchronized in a jitter-free manner such that leading edge transitions occur at the center of READ CLOCK half cycles. This is accomplished by internally decoding and re-encoding using the READ CLOCK as a reference.

When READ GATE changes state, the VCO is stopped and restarted in phase with the PLL input which can be either the internal Crystal Oscillator or ENCODED READ DATA. In this manner the lock time is reduced due to small angles of phase error. Limiting the phase error by restarting the VCO in phase with the input prevents the PLL from locking to harmonics and short lock times are assured. The correct phase of READ CLOCK is also ensured by resetting the N/2 Divider at the same time as the VCO restart.

When READ GATE is high, the 1/4 CELL DELAY allows the Phase Detector to be enabled prior to when an edge of the encoded input is to occur This updates the PLL on a sampled basis and corrects for any phase error with each subsequent input pulse. When READ GATE is low the Phase Detector is continuously enabled and the PLL is both phase and frequency locked to the reference oscillator. By locking the VCO to the reference oscillator it is virtually at the correct frequency when the PLL is switched to track ENCODED READ DATA

The following waveforms are a graphic representation of the PLL alternately locking to ENCODED READ DATA and the Crystal Oscillator.



With an ENCODED READ DATA input of 5 MHz, the final DC level of the VCO waveform is constant as shown with transients occurring at each edge of the READ GATE. The amplitude and duration of the VCO locking transient is dependent on the initial phase error on switching (max is 0.5 rad.) as well as the damping factor and natural frequency of the loop. The lower two waveforms are an expansion of the ENCODED READ DATA and VCO IN signals showing the effect of disabling the VCO during reference switching and the subsequent stairstep characteristic of the VCO waveform as the PLL locks to the new input.

The synchronizer circuit separates the data and clock pulses using windows derived from the VCO output. The window edges are aligned with the opposite edge from that used to phase lock the VCO. Using a VCO running at twice the expected input frequency allows accurate centering of these windows about the expected bit positions.

1F Data Detection

The 531 provides a flag, 1F DETECT, that indicates a continuous stream of "1's" or "0's".

The period of the 1F Detect Retriggerable One-Shot is set so that the sum of the 1/4 Cell Delay and the One-Shot is nominally 1-1/4 times the 2F frequency data period. This results in the 1F DETECT output remaining high during a continuous high frequency input representing a field of "1's" and "0's". External components R1F and C1F at the 1F DETECT SET pin are used to set the One-Shot delay.

A Latch operates in conjunction with the One-Shot to guarantee a minimum 1F DETECT output pulse width of one data period.

Write Precompensation

Write precompensation reduces the effect of intersymbol interference caused by magnetic transition proximity in the disk media. Compensation consists of shifting written data pulses in time to counteract the read back bit shifting caused by such interaction. The severity of the intersymbol interference is a function of radial velocity of the media, the magnitude of the write pulse and the data pattern. Typically, write precompensation is enabled at the same time as the write current level is reduced.

The COMP WRITE DATA output is a re-synchronized version of the MFM WRITE DATA input that has been time shifted, if needed, to reduce intersymbol interference. Re-synchronization, to the internal crystal oscillator, is performed to minimize bit jitter in the output waveform. The magnitude of the time shift, TC, is determined by the RC network at the PRECOMP SET pin and is applied as noted in Table 1 according to the states of $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$ and PRECOMP ENABLE. Figure 2 is a further illustration of these timing relationships.

Table 1: Write Precompensation Truth Table

PRECOMP Enable	$\overline{\text{EARLY}}$	$\overline{\text{LATE}}$	Delay
0	X	X	Constant
1	0	0	Illegal State
1	0	1	TN–TC
1	1	0	TN+TC
1	1	1	TN

TN=Nominal Pulse Delay
TC=Magnitude of Time Shift

Reference Oscillator

The crystal controlled oscillator serves as the system master clock for the write functions. Its frequency divided by two provides a WRITE CLOCK for an external MFM encoder. It is also used to re-synchronize the MFM WRITE DATA for precise timing control when writing data to the disk. A series resonant crystal should be used.

Additionally, the oscillator output is used as a standby reference for the PLL when READ GATE is low. This enables the PLL to lock rapidly to incoming data when required.

When an external system clock, is available it may be connected to XTAL1 and XTAL2 should be left open.

Pin Name	Description
Input Pins	
MFM WRITE DATA	Write data to be resynchronized and precompensated. Synchronous with WRITE CLOCK.
PRECOMP ENABLE	Enables precompensation to be controlled by –EARLY or –LATE.
$\overline{\text{EARLY}}$	When low causes the MFM WRITE DATA pulses to be written early.
$\overline{\text{LATE}}$	When low causes the MFM WRITE DATA pulses to be written late.
ENCODED READ DATA	MFM encoded read data pulses from the read amplifier circuits.
READ GATE	Selects the reference input to the PLL. Selects ENCODED READ DATA when high, crystal oscillator when low.
VCC	+5V
GND	Power and signal ground connection.
Output Pins	
WRITE CLOCK	Crystal-controlled reference oscillator frequency divided by two. Used by the controller to generate MFM WRITE DATA.
COMP WRITE DATA	Re-synchronized and precompensated write data.
READ CLOCK	Voltage-controlled oscillator output divided by two. SYNC READ DATA is synchronized to this signal.
SYNC READ DATA	Synchronized read data output. Leading-edge transitions occur at center of READ CLOCK half cycles.
1F DETECT	Flag used to locate strings of MFM-encoded 1's or 0's in the ENCODED READ DATA input.
External Component Connection Pins	
XTAL1, XTAL2	Connections for oscillator crystal. If oscillator is not required, XTAL1 may be driven by TTL logic signal at twice the data rate and XTAL2 left open.
PRECOMP SET	Pin for R-C network to control write precompensation early and late times.
1F DETECT SET	Pin for R-C network to control the 1F detect period. Component values are dependent on the minimum data period that will keep 1F DETECT high.
1/4 CELL DELAY SET	Pin for R-C network to control the 1/4 CELL DELAY. This allows the Phase Detector to be enabled 1/4 of the data period prior to receiving an MFM data input.
CF1, CF2	Pins for the capacitor used in conjunction with RF and RS to set the VCO center frequency.
RF, RS	Pin for resistors used in conjunction with capacitor to set the VCO center frequency.
PD OUT	Output of phase detector, input to loop filter
VCO IN	Control input of the VCO, for connection of the loop filter output.

Absolute Maximum Ratings*

Characteristics	Rating
Storage Temperature	–65°C to +130°C
Ambient Operating Temperature, TA	0°C to +70°C
Junction Operating Temperature	0°C to +130°C
Supply Voltage, V_{CC}	–0.5 Vdc to +7.0 Vdc
Voltage Applied to Logic Inputs	–0.5 Vdc to V_{CC} +0.5 Vdc
Maximum Power Dissipation	800 mW

*Operation above the absolute max, min ratings may damage the device

Electrical Characteristics Unless otherwise specified 4.75V < V_{CC} < 6.25V, Ta = 0° to 50°C, RPC = 3.3K, CPC = 24pF, R1F = 16K, C1F = 120pF, RQC = 8.2K, CQC = 56pF, RF = 499, RS = 499, CF = 56pF, and X1 = 8MHz to 10.5MHz crystal conforming to military type HC19A/U.

DC Characteristics

Parameter	Test Conditions	Min	Max	Units
High Level Input Voltage, VIH		2.0	—	V
Low Level Input Voltage, VIL		—	0.8	V
High Level Input Current, IIH	VIH = 2.7V	—	20	mA
Low Level Input Current IIL	VIL = 0.4V	—	−0.36	mA
High Level Output Voltage, VOH		—	—	—
Comp Write Data	IOH = −400 μA	2.7	—	V
All Others	IOH = −50 μA	4.6	—	V
Low Level Output Voltage, VOL		—	—	—
Comp Write Data	IOL = 4mA	—	0.4	V
All Others	IOL = 1mA	—	0.4	—
Power Supply Current, Icc	All Outputs Open	—	100	mA

Data Detection Characteristics (Ref Figure 1)

ENCODED READ DATA Pulse Width, TERD			40	$\frac{TRCF + 10}{2}$	ns
ENCODED READ DATA Positive Transition Time, TERDPT		0.8V to 2.0V, CL = 15pF	—	20	ns
READ CLOCK Repetition Period Range, TRCF			0.85TWCF	1.15TWCF	ns
READ CLOCK Pulse Width, TRC			$\frac{TRCF - 15}{2}$	$\frac{TRCF + 10}{2}$	ns
READ CLOCK Positive Transition Time, TRCPT		0.9V to 4.2V, CL = 15pF	—	15	ns
READ CLOCK Negative Transition Time, TRCNT		4.2V to 0.9V, CL = 15pF	—	10	ns
SYNC READ DATA Delay	TSRDD1		0	TRCF − 20	ns
	TSRDD2		0	TRCF − TRC − 20	ns
SYNC READ DATA Pulse Width, TSRD1, 2			40	$\frac{TRCF}{2}$	ns
SYNC READ DATA Positive Transition Time, TSRDPT		0.9V to 4.2V, CL = 15pF	—	15	ns
1F DETECT Delay T1FD Accuracy		TD = 0.95(RIF)(CIF + 7pF) + TQC C1F = 100pF to 180pF	0.9TD	1.1TD	sec
¼ CELL DELAY, TQC Accuracy		TDQ = 0.095 (RQC)(CQC + 7pF) CQC = 43pF to 82pF	0.85TDQ	1.15TDQ	sec

Parameter	Test Conditionss	Min	Max	Units
Phase Locked Loop Characteristics				
VCO Period Accuracy, TVCO	Oscillator period, TO = 1.7(RF + RS)CF CF = 43pF to 82pF	0.9TO	1.1TO	sec
VCO Frequency Range	VCO IN = 0.85V to V_{CC} − 85V, V_{CC} = 5.0V	±20	±30	%
Phase Detector Gain, KD	w/respect to 5 Mbit/sec data rate, V_{CC} = 5.0V	30	45	μA/rad
VCO Control Gain, KVCO	W_o = Vco radian center frequency V = VCO IN voltage change VCO IN = 0.85V to V_{CC} − 0.85V	$\frac{0.12W_o}{V}$	$\frac{0.18W_o}{V}$	rad/ (sec.V)
VCO Phase Preset Error		—	+0.5	rad
Data Detection Window Centering Accuracy		±0.02 TRCF ± 4	—	ns
Number of Read Clock Period Delay From ENC RD DATA Input to SYNC RD DATA Output		—	2	—
Number of READ CLOCK periods that VCO may be disabled during reference switching		—	3	—
Write Precompensation Switching Characteristics (Ref Fig 2)				
WRITE CLOCK Repetition Period, TWCF	Controlled by X1 Freq.	190	250	ns
WRITE CLOCK Pulse, Width, TWC		$\frac{TWCF}{2}$ − 15	$\frac{TWCF}{2}$ + 10	ns
WRITE CLOCK Positive Transition Time, TWCPT	0.9V to 4.2V, CL = 15pF	—	15	ns
WRITE CLOCK Negative Transition Time, TWCNT	4.2V to 0.9V, CL = 15pF	—	10	ns
MFM WRITE DATA Set Up Time, TWDS1, 2		15	—	ns
MFM WRITE DATA Hold Time, TWDH1, 2		10	—	ns
MFM WRITE DATA Release Time, TWDR1, 2		15	—	ns
$\overline{EARLY}$ or $\overline{LATE}$ Set Up Time TELS1, 2		125	—	ns
$\overline{EARLY}$ or $\overline{LATE}$ Hold Time TELH1, 2		10	—	ns
COMPENSATED WRITE DATA, Pulse Width, TCWD	CL = 15pF	40	$\frac{TWCF}{2}$	ns
COMPENSATED WRITE DATA "Nom" Pulse Width Delay, TN		—	$\frac{TWCF}{2}$	ns
COMPENSATION WRITE DATA Compensation Accuracy, TE, TL	TC = 0.15 (RCP)(CPC) CPC = 15pF to 36pF	0.8TC	1.2TC	sec
COMPENSATED WRITE DATA Positive Transition Time, TCWDPT	0.8V to 2.0V, CL = 15pF	—	10	ns

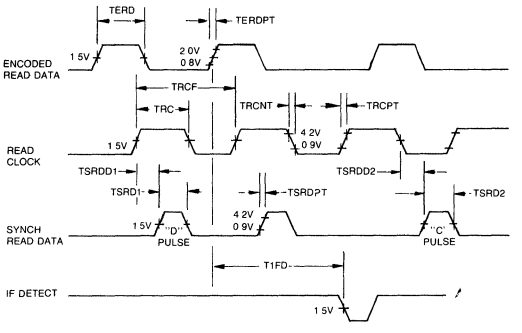


Figure 1 - Data Detection and Synchronizing Waveforms

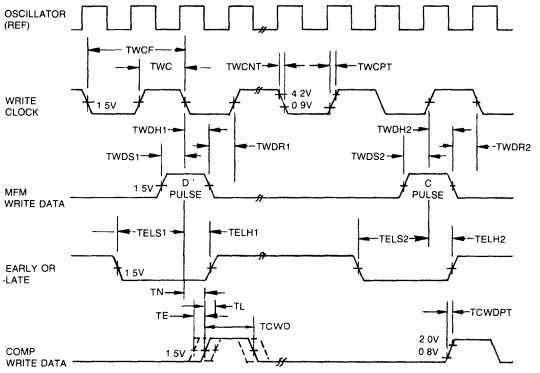


Figure 2 - Write Precompensation Waveforms

Applications Information

In a typical application the, SSI 531 is used with a Western Digital WD1010-05 Winchester Disk Controller as shown in Figure 3.

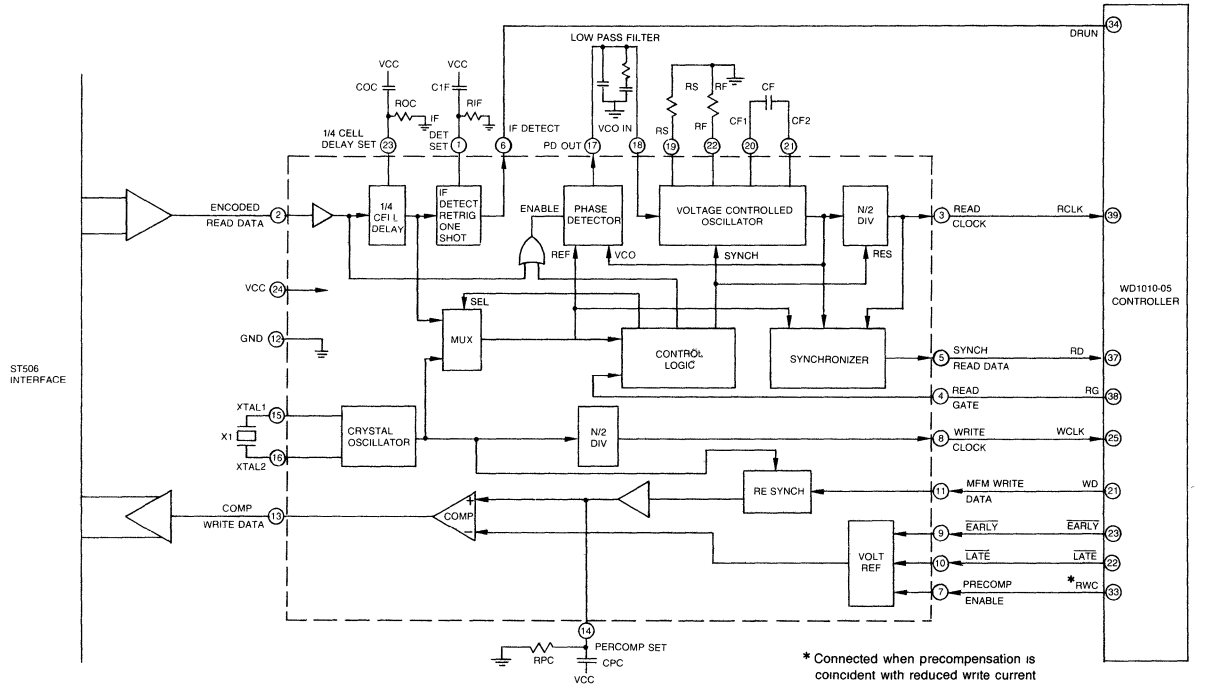


Fig. 3 — Typical System Connections

Interface to the disk drive consists of the Read data input signal from the drive and the Write data output signal from the SSI 531. All the other connections are with the WD1010 and external components.

Loop Filter

The low pass filter serves several purposes, it attentuates high frequency components of the phase error signal from the phase detector and modifies the dynamics of the PLL.

In lock mode, the PLL can be approximately by the linear model shown in Figure 4.

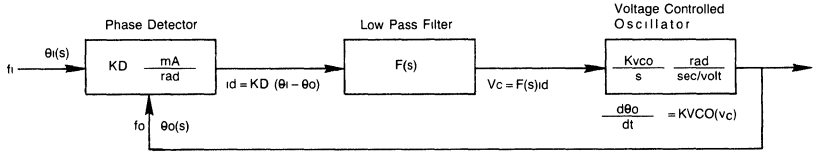


Fig. 4 — Phase Locked Loop

Standard linear system analysis methods can then be used for analysis. The transfer functions of each of the blocks is as follows:

KD = conversion factor for phase detector in μA/radian
KVCO = VCO gain factor in radians/second volt
F(s) = Low pass filter transfer function

Thus the closed loop transfer function is

$$H(s) = \frac{\frac{KDKVCO}{N} F(s)}{S + \frac{KDKVCO}{N} F(s)}$$

where N = ratio between 5M bit/sec and f_{in} (i.e. for preamble N = 1, for crystal reference N = 0.5)

The transient performance and frequency response is highly dependent on the filter transfer function F(s).

To obtain a zero phase error, a type 2 or higher system must be used. This necessitates the use of a filter transfer function with at least one pole at the origin to obtain two poles at the loop gain origin. A detailed analysis supporting this choice can be found in Phase-lock Techniques by Gardner[1]. The filter shown in Figure 5 can be used which will give independent control of the damping factor and natural frequency of the closed loop function. Proper choice of capacitors C1 and C2 will effect loop settling time and stability. More complex filters can be used that give finer control over loop parameters and enhance performance even further.

1 Gardner FM Phaselock Techniques, Wiley NY, Second Ed , 1967

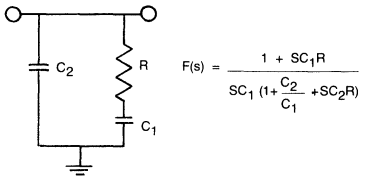


Fig. 5 — Loop Filter Example

V_{CO} Free Running Frequency

The external components RF, RS and CF, are chosen to set the VCO frequency at twice the ENCODED READ DATA bit rate. For a symmetrical window, equal values of RF and RS are used. Increasing the ratio RF/RS causes the detection window to occur earlier in time with respect to ENCODED READ DATA. Decreasing the ratio has the opposite effect, the value of the time shift is:

$$T = TVCO\ (RF - RS)/(RF + RS)$$

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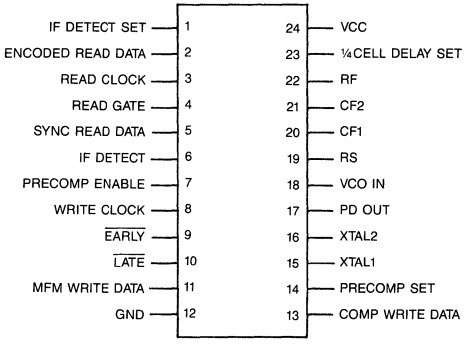
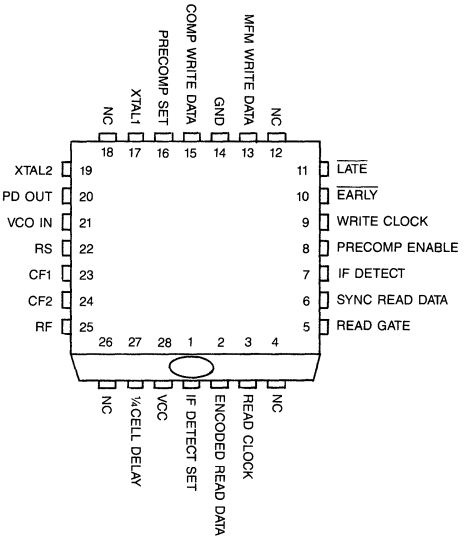
SSI 531 Pin Assignments



24-Lead Dip Pin Out



28-Lead PLCC (Quad) Pin Out

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INNOVATORS IN INTEGRATION

SSI 540 Series
Read Data Processor

Preliminary Data Sheet

GENERAL DESCRIPTION

The SSI 540 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM read signals from rigid media. ST506 compatible interfacing is provided for write data signals, head select lines and recovered read data as applicable.

In read mode the SSI 540 provides amplification, differentiation and time domain qualification of head preamplifier outputs. The recovered data is available at the output of a differential line driver that conforms to the ST506 interface specification. In write mode the SSI 540 provides a differential line receiver conforming with ST506 requirements. Schmitt Trigger inputs on head select lines and an open collector output for voltage fault indication are provided for interface compatibility. All other logic inputs and outputs are TTL compatible.

The SSI 540-2 is a dual ground version for use in noisier environments. In order to provide this feature the number of head select lines is reduced to 2.

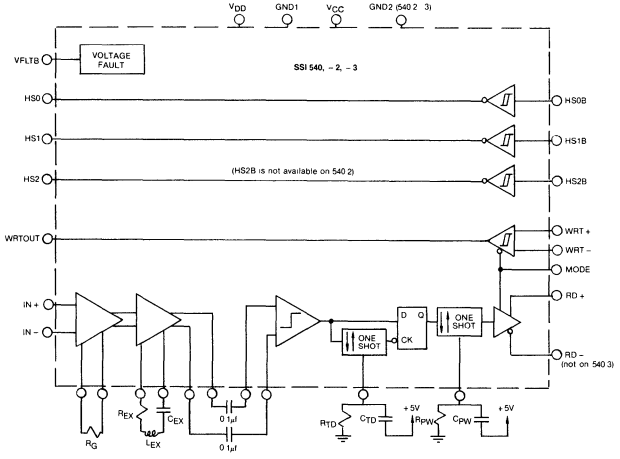
Two other versions of the SSI 540 are available that offer subsets of the above configurations. The SSI 540-3 has dual grounds and an open-collector RD output instead of a differential line-driver output. The SSI 540-4 has the same features as the SSI 540-3 but also deletes the head select buffers. The SSI 540-4 is available in a 22-Pin dip.

When used with a read/write preamplifier (i.e. SSI 117 or SSI 501), the SSI 540 or SSI 540-2 and required external passive components perform all read/write signal processing necessary between the heads and the interface connector of an ST506 compatible Winchester disk drive. With the SSI 540-3 and SSI 540-4 a line driver is required.

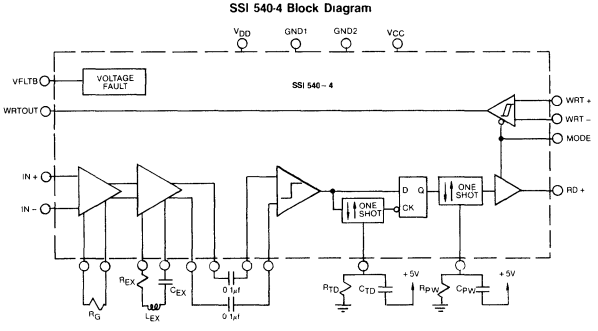
FEATURES

- **Differential Read and Write Ports**
- **Schmitt Trigger Head Select Inputs for Higher Noise Immunity**
- **Programmable Gain**
- **Time Domain Pulse Qualification Supports MFM Encoded Data Retrieval**
- **Supply Voltage Fault Detection**
- **+12 Volt and +5 Volt Power Supplies**
- **I/O Meets ST506 Requirements**
- **Dual-In-Line and Surface Mount Packages Available**
- **Adjustible Time Domain Filter and Output Pulse Width Settings**

SS1 540-1, -2, -3 Block Diagram



SSI 540-4 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

Circuit Operation

In both read and write modes, Schmitt Trigger inputs are used to buffer the three head select lines providing the increased noise immunity required of a ST506 interface. A power supply monitoring function, VFLTB, is provided to flag a low voltage fault condition if either supply is low. A low voltage fault condition results in a low level output on the VFLTB pin.

READ MODE

In the read mode (MODE input high) the read signal is detected, time domain qualified and made available at RD+ and RD− as differential MFM encoded data, or at the RD+ open collector output. This is accomplished by the on-board Amplifier, Differentiator, Zero Crossing Detector, Time Domain Filter, Output One Shot and Line Driver circuits.

The amplified and filtered read back signal, which contains pulses corresponding to magnetic transitions in the media is AC coupled into the input amplifier. A resistor, Rg, connected between pins G+ and G− is used to adjust the 1st stage amplifier gain according to the following expression

$$Av_1 = \frac{680}{17 + Rx} \quad \text{Where } Rx = \frac{94 \times (Rg + 42)}{230 + Rg}$$

First stage gain can be monitored at the DIF+ and DIF− pins.

The amplifier is followed by an active differentiator whose external network serves to transform peaks in the input signal into zero-crossings while maintaining the time relationship of the original input peaks. Differentiator response is set by an external capacitor or more complex series LRC network between the DIF+ and DIF− pins. The transfer function with such a network is:

$$Av_2 = \frac{-1420\,Cex\,s}{Lex Cex\,s^2 + (Rex + 46)\,Cex\,s + 1}$$

where: Cex = external capacitor (50 pf to 250 pf)
Rex = external resistor
Lex = external inductor
$s = jw = j2\pi f$

Total gain from IN+ and IN− to OUT+ and OUT− is:
$Av = Av_1 \times Av_2$

To reduce pulse pairing (bit shift), it is essential that the input to the zero-crossing detector be maximized to reduce the effect of any comparator offset. This means that the above gains should be chosen such that the differential voltage at OUT+ and OUT− approaches 5 Vpp at max input and frequency.

The Differentiator output is AC coupled into a zero-crossing detector that provides an output level change at each positive or negative zero transition on its input. The zero-crossing detector output is coupled to a Time Domain Filter that eliminates false triggering of the output one-shot by spurious zero-crossings. The validity decision is based on a minimum duration between zero crossings that can be set externally by an RC network on the TD pin.

The output of the Time Domain Filter triggers a one-shot that defines the output pulsewidth based on an external RC network on the PW pin. These output pulses are fed into a line driver that provides a high-current differential output at RD+ and RD−, or are made available as an open-collector output at RD+.

Write Mode

In the write mode (MODE input low) the differential line receiver is enabled. This receiver accepts the differential data from the ST506 interface and outputs a TTL signal for the write data input of an external R/W amplifier. A low on the MODE input also puts the read outputs in a high impedance state, allowing several 540's to be multiplexed on a bus.

Layout Considerations

The SSI 540 is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and balanced. Analog test points should be provided with a probe ground in the immediate vicinity. Do not run digital signals under the chip or next to analog inputs. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 540 ground from other circuits on the disk drive PCB.

Absolute Maximum Ratings*

5 V Supply Voltage, Vcc ..... 6 V
12 V Supply Voltage, Vdd ..... 14 V
Storage Temperature ..... −65 to +150 °C
Operating Temperature, Tj ..... +25 to +135 °C
Lead Temperature (soldering 10 sec) ..... 260 °C
Pin Voltages
IN+,IN−,G+,G−,DIF+,DIF−,
OUT+,OUT−,DIN+ DIN− ..... 0.3V to Vdd + 0.3V
RD+,RD−,WRTOUT,HSO,
HS1,HS2,VFLTB ..... −0.3V to Vcc + 0.3V or 100 mA
TD,PW,MODE,WRT+,WRT−,
HS0B,HS1B,HS2B ..... −0.3V to Vcc + 0.3V

*Operation above absolute maximum ratings may damage the device.

ELECTRICAL CHARACTERISTICS Unless otherwise specified, 4.5V < Vcc < 5.5V, 10.8V < Vdd < 13.2V, 25 °C < T(junction) < 135 °C.

Power Supply

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Icc—Vcc Supply Current	Read mode, no TTL or RD ± loads	—	35.0	46	mA
	Write/Disable mode, no TTL loads	—	36.5	43	mA
Idd—Vdd Supply Current	Read mode	—	33.5	43	mA
	Write/Disable mode	—	34.5	50	mA
Pd—Power Dissipation	Tj = 125 °C Read/Write modes	—	—	820	mW

Logic Signals — Mode

Input Low Voltage (V_{IL})		−0.3	—	+0.8	V
Input Low Current (I_{IL})	V_{IL} = 0.4V	—	—	−0.8	mA
Input High Voltage (V_{IH})		2.0	—	Vcc + 0.3	V
Input High Current (I_{IH})	V_{IH} = 2.4V	—	—	100	μA

Logic Signals — HSnB

Parameter	Test Conditions	Min.	Max.	Units
Threshold Voltage, V_T + Positive-Going	Vcc = 5.0V	1.4	2.0	V
Threshold Voltage, V_T − Negative-Going	Vcc = 5.0V	0.6	1.15	V
Input Low Current (I_{IL})	V_{IL} = 0.4V	—	−0.4	mA
Input High Current (I_{IH})	V_{IH} = 2.4V	—	100	μA

Logic Signals — WRTOUT, HSn

Output Low Voltage (V_{OL})	I_{OL} = 1.6mA	—	0.4	V
Output High Voltage (V_{OH})	I_{OH} = −500uA	2.4	—	V

Logic Signals — VFLTB & RD Open Collector Output

Output Low Voltage (V_{OL})	I_{OL} = 1.6mA 4.5 < Vcc < 5.5 I_{OL} = 0.5mA, 1.0 < Vcc < 4.5V (VFLTB Only)	—	0.4	V
Output High Current (I_{OH})		—	25	μA

Mode Control

Read to Write Transition Time		—	1.0	μs
Write to Read Transition Time		—	1.0	μs

Supply Voltage Fault Detect

Vdd Fault Threshold	VFLTB transition from high to low	9.5	10.8	V
Vcc Fault Threshold	VFLTB transition from high to low	4.3	4.6	V

Parameter	Test Conditions	Min.	Max.	Units
Write Mode				
Differential Input Voltage		±0.4	—	V
Input Hysteresis		±40 typ		mV
Single Ended Input Resistance		4.0	—	kΩ
Input Common Mode Voltage Range		0.0	5.0	V
Input Pulse Width		20	—	ns
Propagation Delay (WRT+ & WRT− TO WRTOUT)	V(WRT+ − WRT−) = 0 to WRTOUT = 1.3V[1] see Fig. 1 T_{PD}	—	40	ns
Output Rise and Fall times	WRTOUT transition from 0.7 to 1.9V[1], see Fig 1	—	15	ns

1. WRTOUT load is 30pf to GND and 2.5 kΩ to Vcc

Read Mode Unless otherwise specified RD+ and RD− are loaded with 100Ω differentially and 30pf per side to GND, IN+ and IN− are AC coupled, G+ and G− are open. An 800Ω resistor is tied between the DIF+ and DIF− pins with each pin loaded to GND with <3pf. The OUT+ and OUT− pins are loaded with <3pf in parallel with >5kΩ AC coupled (i.e. no DC current).

Parameter	Test Conditions	Min.	Max.	Units
Amplifier & Active Differentiator				
Differential Voltage Gain (IN ± to OUT ±)	Rg = ∞ , Rex = 800Ω	7.2	12.6	V/V
	Rg = 0Ω , Rex = 200Ω	72	155	V/V
Bandwidth	−3dB point	30	—	MHz
Common Mode Input Impedance (IN ±)		3.5 typ		kΩ
Differential Input Resistance (IN ±)	V(IN+ − IN−) = 100mVpp, 2.5 MHz, AC coupled	6.0 typ		kΩ
Differential Input Capacitance (IN ±)	V(IN+ − IN−) = 100mVpp, 2.5 Mhz, AC coupled	—	8	pf
Input Noise (IN ±)	Inputs shorted together Rg = 0Ω, Rex = 200Ω	—	10	$nV/\sqrt{Hz}$
V(DIF+ DIF−) Output Swing	Set by Rg	—	3.2	Vpp
V(OUT+ − OUT−) Output Swing	Set by Rex, Lex, Cex Impedance	—	5	Vpp
Dynamic Range	Common mode DC input where gain falls to 90% of 0.0V DC common mode input. 10mVpp AC input, Rg = ∞, Rex = 1200Ω	−240	−240	mV
DIF+ to DIF− pin Current		±1.9	—	mA
OUT+ to OUT− pin Current		±3.8	—	mA
CMRR (input referred)	V(IN+) = V(IN−) = 100mVpp, 5MHz, Rg = 0Ω , Rex = 200Ω	40	—	dB
PSRR (input referred)	Vdd or Vcc = 100mVpp, 5Mhz, Rg = 0Ω , Rex = 200Ω	40	—	dB

Parameter	Test Conditions	Min.	Max.	Units
Zero Crossing Detector				
Input Offset Voltage		—	5.0	mV
Input Signal Range		—	5.0	Vpp
Differential Input Impedance (DIN ±)		4.4 typ		kΩ
Line Driver (SSI 540 & 540-2 only)				
Output Sink Current	V_{OL} = 0.5V, V(MODE) = 2.0V	20	—	mA
Output Source Current	V_{OH} = 2.5V, V(MODE) = 2.0V	−2	—	mA
Output Current	Vo = 0V to Vcc, V(MODE) = 0V	−50	50	μA
Output Rise Time	Vo = 0.7V to 1.9V 100Ω between RD+ and RD−, 30pf to GND	2	30	ns
Output Fall Time	Vo = 1.9V to 0.7V 100Ω between RD+ and RD−, 30pf to GND	2	30	ns
Time Domain Filter				
Delay Range	$T_{TD1} = 0.184 \times R_{TD} \times C_{TD}$, R_{TD} = 1.5kΩ to 3.1kΩ, C_{TD} = 50pf to 200pf, V(DIN+ − DIN−) = 100mVpp, 5MHz, AC coupled square wave See Fig 2	13.8	114	ns
Delay Range Accuracy	Vcc = 5.0V, Tj = 60°C	—	±15	ns
	Variation with supply and temperature	—	12	ns
Propagation Delay	Delay = $T_{D2} - T_{D1}$ See Fig 2	—	80	ns
Data Pulse				
Pulse Width	$T_{PW} = 0.184 \times R_{PW} \times C_{PW}$ R_{PW} = 2kΩ, C_{PW} = 150pf See Fig 2	30	80	ns
Skew	V(DIN+ − DIN−) = 100mVpp, 5MHz, AC coupled square wave w/2nsec rise & fall times.	—	5	ns

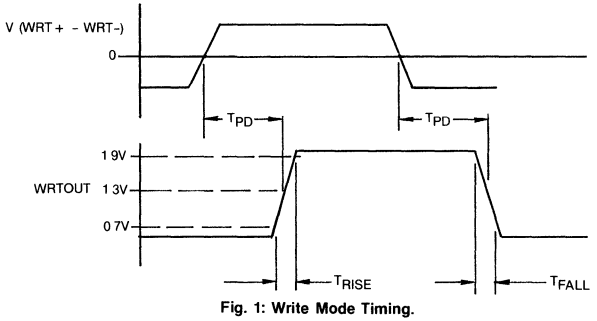


Fig. 1: Write Mode Timing.

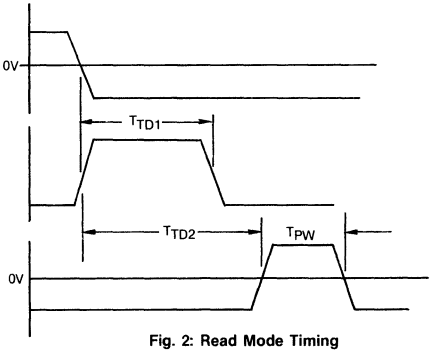
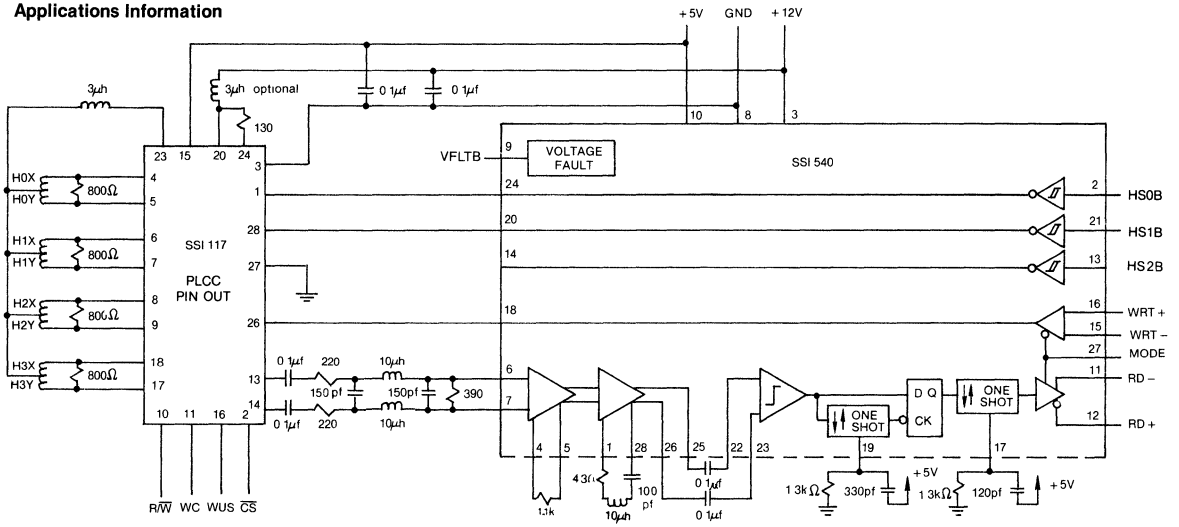


Fig. 2: Read Mode Timing

Applications Information



Design Example

As a design example a system using a 4-channel SSI 117 Read/Write preamplifier will be used.

Assumptions—coding scheme is MFM
—data rate is 5 Mbits/second
—Ferrite head output is 1 mVpp min. and 2 mVpp max.

The output from the SSI 117 is 80 mVpp to 240 mVpp. Assuming a 6 dB loss through the external low pass filter the input to the SSI 540 at IN+, IN− is:

40mVpp to 120 mVpp differential voltage.

For this analysis the ±37% tolerance on gain from IN+, IN− to OUT+, OUT− will be equally divided between the gain stage and the differentiator, so each will contribute a ±17% variance from nominal values. The objective is to get a 5 Vpp signal at OUT+,OUT− at max input and max frequency. For MFM the 2f frequency in a 5 Mbit/sec data rate is 2.5 MHz, 1f is 1.25 MHz.

Gain Setting

Maximum gain from the amplifier occurs when Rg = 0. So calculating for nominal gain:

$$Rx = \frac{94 \times 42}{230} = 17.17$$

$$Av_1 = \frac{680}{17 + 17.17} = 19.9 \text{ nominal or } 16.52 \text{ min to } 23.28 \text{ max}$$

The voltage swing at the DIF+, DIF− pins is:

120 mVpp x 22.25 = 2.79 Vpp max
40 mVpp x 17.55 = 0.661 Vpp min

This is within the 3.2 Vpp max guaranteed by this specification, so max gain will be used.

Differentiator Design

The differentiator can be as simple as a capacitor or as complex as a series RLC network. In order not to violate the 5 Vpp max spec at OUT+,OUT− the maximum differential voltage gain is:

$$\frac{5}{2.79} = 1.79 \text{ max gain}$$

which is nominally a gain of 1.53

For Cex only:

$$Cex = \frac{1.53}{2\pi f \sqrt{(1420)^2 - (1.53 \times 46)^2}} = 68pf$$

check for current saturation:

Ic = Cex x Vp x 2πf must be less than 1.9 mA

For Cex, Rex network:

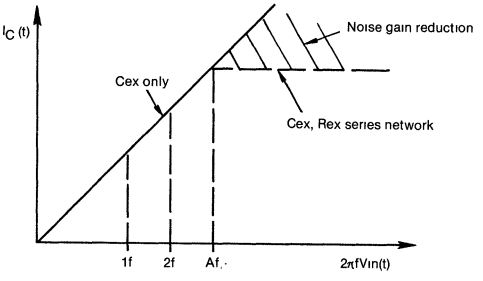
The following two formulas are used:

$$1.53 = \frac{j\,1420\,Cex\,2\pi f}{j(Rex + 46)\,Cex\,2\pi f + 1}$$

$$Rex + 46 = \frac{1}{Cex\,A\,2\pi f\,max}$$

where A is chosen for position of corner frequency to reduce high frequency noise gain from the single capacitor network.

Graphically the method is as follows:



Check for current saturation using the following formula.

$$Ip = \frac{jVp2\pi fCex}{1 + j\ 2\pi f\ Cex\ (R+46)}$$

For R_{ex}, C_{ex}, L_{ex} networks, the following formulae are used·

$$\text{Gain } G = \frac{-j\ 1420\ C_{ex}\ 2\pi f}{1 - L_{ex}C_{ex}\ (2\pi f)^2 + j\ (R_{ex} + 46)\ C_{ex}\ 2\pi f}$$

$$= \frac{1420\ C_{ex}\ 2\pi f}{\sqrt{[1 - L_{ex}C_{ex}\ (2\pi f)^2]^2 + [(R_{ex} + 46)\ C_{ex}\ 2\pi f]^2}}$$

$$\left[-\frac{\pi}{2} - \tan^{-1}\left[\frac{(R_{ex} + 46)\ (C_{ex}\ 2\pi f}{1 - L_{ex}C_{ex}\ (2\pi f)^2} \right] \right]$$

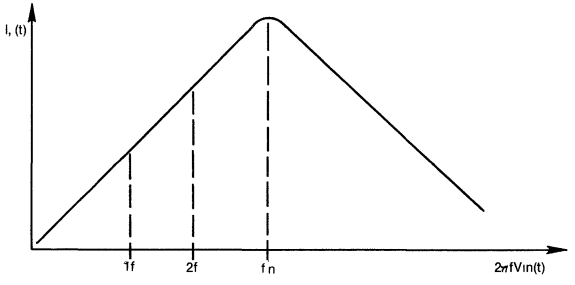
$$\text{Center Freq } f_n = \frac{1}{2\pi\sqrt{L_{ex}C_{ex}}}$$

$$\text{Damping Factor } \zeta = \frac{(R_{ex} + 46)\ C_{ex}}{2\sqrt{L_{ex}C_{ex}}}$$

$$\text{Group Delay } \frac{dQ}{df} = \frac{2\zeta}{2\pi f_n}\left[\frac{1 + \left(\frac{f}{f_n}\right)^2}{1 + (4\zeta^2 - 2)\left(\frac{f}{f_n}\right)^2 + \left(\frac{f}{f_n}\right)^4} \right]$$

This technique adds another pole to the differentiator response to attenuate high frequency noise. The center frequency damping ratio and group delay are chosen to meet system requirements. Values for the center frequency are usually from 2 to 10fmax and the damping factor may be from 0 3 to 1.

Graphically the method is as follows



As with the previous Rex, Cex example, care must be taken to insure a 90° phase shift at the frequencies of interest (1f and 2f or 1.25 MHz and 2.5 MHz). This requirement is modified by any need to compensate for phase distortion caused by preceeding signal processing.

Effect of Gain Tolerance

At minimum gain the 1_mVpp input at 1.25 MHz frequency has the following effects:

Using the capacitor only results with C_{ex} = 68pf

$$\text{Diff gain} = \frac{1420\ C_{ex}\ 2\pi f}{\sqrt{1 + (46\ C_{ex}\ 2\pi f)^2}} = 0.758 \text{ nominal}$$

Using ±17% tolerance, min gain = 0.629

so with a 661 mVpp input the min voltage @ OUT + /OUT – is 416 mVpp.

Thus, with all tolerances considered, a 1_m Vpp to 2_m Vpp input to the SSI 117 will result in a 5 Vpp to 416 mVpp input to the zero-crossing detector.

ONE-SHOT CONSIDERATIONS

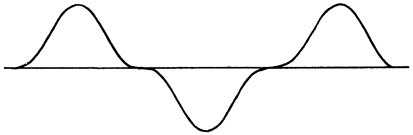
The timing for both one shots conform to the same equation: t = 0.184 x C x R

Setting of the time domain one-shot reflects the expected base line shouldering effect at the 1f frequecy and is set accordingly. In this example the output pulse width has been set at approximately 30 nsec and the time domain filter at approximately 80 nsec.

EXTERNAL FILTER

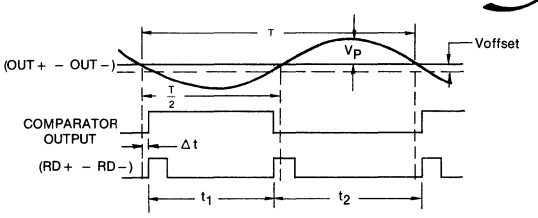
The filter on the output of the read/write amplifier, limits the bandwidth of the input to the SSI 540. This reduces the noise input to the differentiator which can produce spurious zero-crossings. The design of this filter is not discussed here, but general aspects of its transfer function will be discussed.

On the outer tracks of an ST506 compatible drive using a MFM coding technique, the output pulses return to baseline or exhibit shouldering.



Outer Track Waveform

This waveform has a high third harmonic content. In order to preserve this waveform the filter must not add any distortion to this harmonic. For this reason, the most common filter type used is a Bessel Filter which has a constant group delay ($\frac{d\Phi}{df}$) or linear phase shift. Thus for a 5 Mbit/sec MFM waveform a Bessel Filter with constant group delay and a –3 dB point of 3.75 MHz is required. This is the type of filter used in the design example.



Effect of Comparator Offset on output waveform

Bit Shift or Pulse Pairing

Theoretical consideration of this aspect of pulse replication relative solely to the SSI 540 indicates that comparator offset is the major contributing parameter. For sinusoidal inputs the offset produces a non-symetric waveform as shown.

The RD+,RD– output pulses have been offset from true position (zero-crossing) by an amount Δt, that is dependent on Voffset and OUT+,OUT– amplitude.

This relationship is

$$\Delta t = \frac{1}{w} \sin^{-1} \left(\frac{Voff}{Vp} \right) \text{ (radians)}$$

So, referring to previous results:

when OUT+,OUT– = 5Vpp @ 2.5 MHz

Δt = 0.13 nsec

when OUT+,OUT– = 416 mVpp @ 1.25 MHz

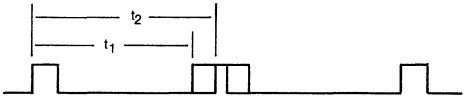
Δt = 3.1nsec

As can be seen above the center pulse has been shifted from its true position by 2 Δt. So for this example the Bit Shift contributed by the SSI 540 is:

0.26 nsec at maximum input and frequency

6.2 nsec at minimum input and frequency

In some literature this effect is called Pulse Pairing. If the RD+,RD– waveform is displayed on an oscilloscope with the trigger holdoff adjusted to fire on succeeding pulses the following waveform is observed:



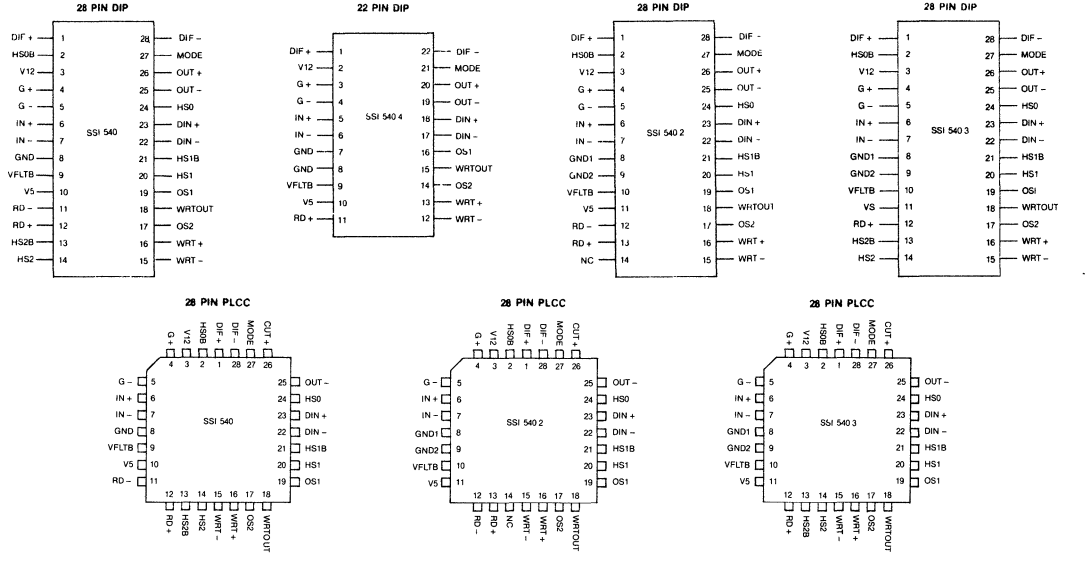
Pulse Pairing

where $t_2 - t_1$, = 4 Δt or 2 x (Bit Shift)

Using this technique and a sinusoidal input to D_{IN} ± of varying amplitude at 1.25 MHz and 2.5 MHz, the following results were obtained.

D_{IN} ± Input V_{p-p}	RD ± Pulse Jitter (4Δt) nsec	
	1.25 MHz	2.5 MHz
5	06	10
3	06	08
1	06	00
7	14	00
3	16	05
1	38	12
07	56	24
06	62	32
05	70	35
04	96	45
03	118	60

SSI 540 Pin Assignments



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SSI 541 Read Data Processor

Preliminary Data Sheet

DESCRIPTION

The SSI 541 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals. The circuit will handle data rates up to 15 Megabits/sec.

In read mode the SSI 541 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry.

The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

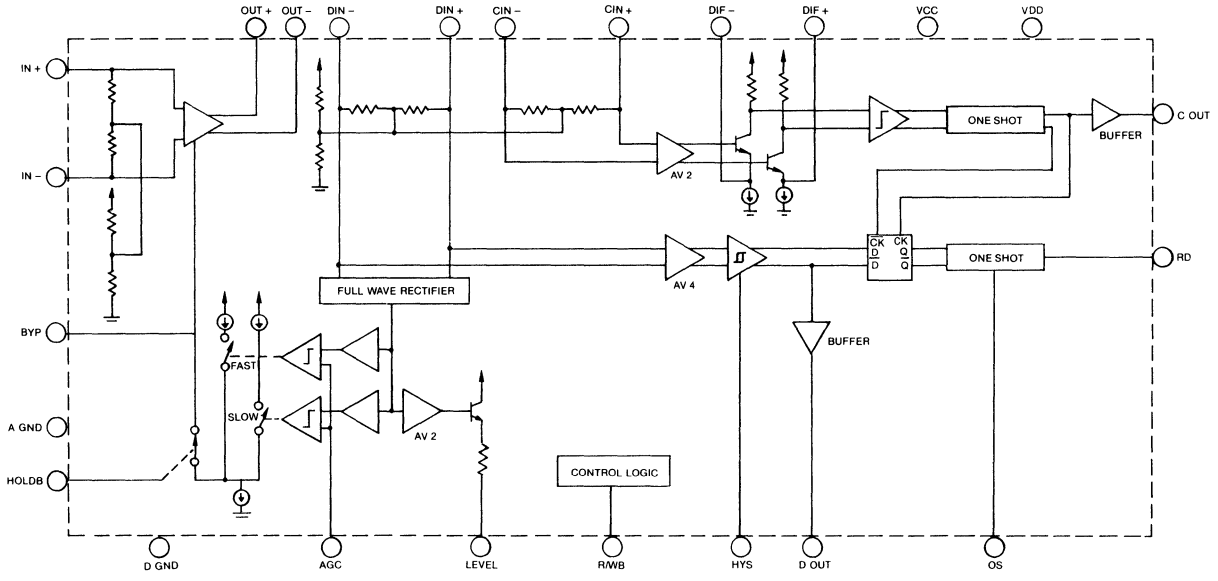
In write mode the circuitry is disabled and the AGC gain stage input impedance switched to a lower level to allow fast setting of the input coupling capacitors during a write to read transition.

The SSI 541 requires +5V and +12V power supplies and is available in a 24 pin DIP and 28 pin PLCC.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Supports data rates up to 15 megabits/sec**
- **Standard 12V ±10% and 5V ±10% supplies**
- **Supports embedded servo pattern decoding**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**

SSI 541 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

CIRCUIT OPERATION

Read Mode

In the read mode (R/WB input high or open) the input read signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

The amplified head signals are AC coupled to the IN+ and IN− pins of the AGC amplifier that is gain controlled by full wave rectifying and amplifying the (DIN+ — DIN−) voltage level and comparing it to a reference level at the AGC pin. A fast attack mode, which supplies a 1.5mA charging current for the capacitor at the BYP pin, is entered whenever the instantaneous DIN± level is more than 125% of set level. Between 100% and 125% the slow attack mode is invoked, providing 0.17mA of charging current. The two attack modes allow rapid AGC recovery from a write to read transition while reducing zero crossing distortion once the amplifier is in range.

The level at the AGC pin should be set such that the differential voltage level at the DIN+, DIN− pins is 1.00Vpp at nominal conditions. The circuit can swing 3.0Vpp at the OUT+, OUT− pins which allows for up to 6dB loss in any external filter connected between the OUT+, OUT− outputs and the DIN+, DIN− inputs.

Gain of the AGC section is nominally

$$\frac{Av2}{Av1} = \exp \frac{V2 - V1}{5.8 \times Vt}$$

Where: Av1 and Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

$Vt = (K \times T)/q = 26mV$ at room temperature.

One filter for both data (DIN+, DIN− input) and clock (CIN+, CIN− input) paths, or a separate filter for each path may be used. If two filters are used, care must be exercised to control time delays so that each path is timed properly. A multi-pole Bessell filter is typically used for its linear phase or constant group delay characteristics.

The filtered data path signal is fed into a hysteresis comparator that is set at a fraction of the input signal level by using an external filter/network between the LEVEL and Hys pins. Using this approach allows setting the AGC slow attack and decay times slow enough to minimize distortion of the clock path signal. This "feed-forward" technique, utilizing a fraction of the rectified data path input available at the LEVEL pin as the hysteresis threshold, is especially useful in the slow decay mode of the AGC loop. By using a short time constant for the hysteresis level, the qualification method can continue as the AGC amplifier gain is slowly ramped up. This level will also shorten the write to read transient recovery time without affecting data timing as the circuit will be properly decoding before the AGC gain has settled to its final value. The comparator output is the "D" input of a D type flip-flop. The DOUT pin provides a buffered test point for monitoring this function.

The filtered clock path signal is differentiated to transform signal peaks to zero-crossings which clock an edge-trigger circuit to provide output pulses at each zero-crossing. The pulses are used to clock the D type flip-flop. The COUT pin is a buffered test point for monitoring this function.

The differentiator function is set by an external network between the DIF+, DIF− pins. The transfer function is:

$$AV = \frac{-2000Cs}{LCs^2 + (R+92)\,Cs + 1}$$

Where: C= external capacitor (20pf to 150pf)
L = external inductor
R = external resistor
$s = jw = j2\pi f$

During normal operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to CIN+, CIN−. The D input to the flip-flop only changes state when the signal applied to the DIN+, DIN− inputs exceeds the hysteresis comparator threshold opposite in polarity to the previous peak that exceeded the threshold.

The clocking path, then, determines signal timing and the data path determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold.

The delays from CIN+, CIN− inputs to the flip-flop clock input and from the DIN+, DIN− inputs to the flip-flop D input are well matched.

WRITE (DISABLED) MODE

In the write or disabled mode (R/WB input low) the digital circuitry is disabled and the AGC amplifier input impedance is reduced. In addition the AGC amplifier gain is set to maximum so that the loop is in its fast attack mode when changing back to Read Mode. The lowered input impedance facilitates more rapid settling of the write to read transient by reducing the time constant of the network between the SSI 541 and a read/write preamplifier, such as the SSI 510.

Internal SSI 541 timing is such that this settling is accomplished before the AGC loop is activated when going to read mode. Coupling capacitors should be chosen with as low a value as possible, consistant with bandwidth requirements, to allow more rapid settling.

LAYOUT CONSIDERATIONS

The SSI 541 is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 541 and associated circuitry grounds from other circuits on the disk drive PCB.

PIN DESCRIPTION

Pin Name	Description
VCC	5 volt power supply
VDD	12 volt power supply
AGND, DGND	Analog and Digital ground pins
R/WB	TTL compatible read/write control pin
IN+, IN–	Analog signal input pins
OUT+, OUT–	AGC Amplifier output pins
BYP	The AGC timing capacitor is tied between this pin and AGND
HOLDB	TTL compatible pin that holds the AGC gain when pulled low
AGC	Reference input voltage level for the AGC circuit
DIN+, DIN–	Analog input to the hysteresis comparator

Pin Name	Description
HYS	Hysteresis level setting input to the hysteresis comparator
LEVEL	Provides rectified signal level for input to the hysteresis comparator
DOUT	Buffered test point for monitoring the flip-flop D input
CIN+, CIN–	Analog input to the differentiator
DIF+, DIF–	Pins for extrenal differentiating network
COUT	Buffered test point for monitoring the clock input to the flip-flop
OS	Connection for read output pulse width setting capacitor
RD	TTL compatible read output

Absolute Maximum Ratings*

5V Supply Voltage, VCC 6V
12V Supply Voltage, VDD 14V
Storage Temperature ..... –65° to 150°C
Lead Temperature ..... 260°C
R/$\overline{W}$, IN+, IN–, HOLD ..... –0.3V to VCC + 0.3V
RD ..... –0.3 to VCC + 0.3V or + 12mA
All others ..... –0.3V to VDD + 0.3V

*Operation above these rating may cause permanent damage to device

R/WB	HOLDB	Mode
1	1	READ — Read amp on, AGC active, Digital section active
1	0	HOLD — Read amp on, AGC gain held constant Digital section active
O	X	WRITE — AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced

Electrical Characteristics Unless otherwise specified 4.5V≤ VCC≤ 5.5V, 10.8V≤ VDD≤ 13.2V, 25C≤ Tj≤ 135C

Parameter	Test Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY					
ICC — VCC Supply Current	Outputs unloaded	—	—	14	mA
IDD — VDD Supply Current	Outputs unloaded	—	—	70	mA
Pd — Power Dissipation	Outputs unloaded, Tj = 135C	—	—	730	mW
LOGIC SIGNALS					
VIL — Input Low Voltage	—	–0.3	—	0.8	V
VIH — Input High Voltage	—	2.0	—	—	V
IIL — Input Low Current	VIL = 0.4V	0.0	—	–0.4	mA
IIH — Input High Current	VIH = 2.4V	—	—	100	μA
VOL — Output Low Voltage	IOL = 4.0mA	—	—	0.4	V
VOH — Output High Voltage	IOH = 400μA	2.4	—	—	V
MODE CONTROL					
Read to Write Transition Time	—	—	—	1.0	μS
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2	—	3.0	μS
Read to Hold Transition Time	—	—	—	1.0	μS
WRITE MODE					
Common Mode Input Impedance (both sides)	R/WB pin = low	—	250	—	Ω

Parameter	Test Conditions	Min.	Typ.	Max.	Units
READ MODE					
AGC Amplifier	Unless otherwise specified IN+ and IN− are AC coupled, OUT+ and OUT− are loaded differentially with $>600\Omega$ and each side is loaded with <10pf to GND, a 2000pf capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT− is AC coupled to DIN−, AGC pin voltage is 3.0VDC.				
Differential Input Resistance	V(IN+ — IN−) = 100mVpp@ 2.5MHz	—	5K	—	Ω
Differential Input Capacitance	V(IN+ — IN−) = 100mVpp@ 2.5MHz	—	—	10	pF
Common Mode Input Impedance (both sides)	R/WB pin high	—	1.8	—	KΩ
	R/WB pin low	—	0.25	—	KΩ
Gain Range	$1.0\text{Vpp} \leqslant \text{V(OUT+ — OUT−)} = 2.5\text{Vpp}$	4.0	—	83	V/V
Input Noise Voltage	Gain set to maximum	—	—	15	$\text{nV}/\sqrt{\text{Hz}}$
Bandwidth	Gain set to maximum −3dB point	25	—	—	MHz
Maximum Output Voltage Swing	Set by AGC pin voltage	3.0	—	—	Vpp
OUT+ to OUT− Pin Current	See Note 1, No DC path to GND	±3.2	—	—	mA
Output Resistance	—	—	20	30	Ω
Output Capacitance		—	—	15	pF
(DIN+ — DIN−) Input Voltage Swing VS AGC Input Level	$30\text{ mVpp} \leqslant \text{V(IN+ — IN−)} = 550\text{mVpp}$ $1.5 \leqslant \text{V(AGC)} \leqslant 3.75\text{V}$	—	0.48	—	Vpp/V
(DIN+ — DIN−) Input Voltage Swing Variation	$30\text{mVpp} \leqslant \text{(IN+ — IN−)} \leqslant 550\text{mVpp}$, AGC Fixed, Over supply and temperature	—	—	±4	%
Gain Decay Time (Td)	Vin=300mVpp— $>$150mVpp at 2.5MHz, Vout to 90% of final value. See Fig. 1a	—	50	—	μS
Gain Attack Time (Ta)	From Write to Read transition to Vout at 110% of final value Vin=400mVpp @ 2.5MHz. See Fig. 1b	—	4	—	μS
Fast AGC Capacitor Charge Current	V(DIN+ = DIN−)= 1.6V V(AGC) = 3.0V	—	1.5	—	mA
Slow AGC Capacitor Charge Current	V(DIN+ — DIN−)= 1.6V Vary V(AGC) until slow discharge begins	—	0.17	—	mA
Fast to Slow Attack Switchover Point	$\frac{\text{V(DIN+ — DIN−)}}{\text{V(DIN+ — DIN−) Final}}$	—	1.25	—	—
AGC Capacitor Discharge Current	V(DIN+ — DIN−)= 0.0V Read Mode Hold Mode	— −0.2	4.5 —	— +0.2	μA μA
CMRR (Input Referred)	V(IN+)=V(IN−)= 100mVpp @5MHz, gain at max.	40	—	—	dB
PSRR (Input Referred)	VCC or VDD = 100mVpp @5MHz, gain at max.	30	—	—	dB

Note 1 AGC amplifier output current may be increased as in Fig. 4

HYSTERESIS COMPARATOR					
Input Signal Range	—	—	—	1.5	Vpp
Differential Input Resistance	V(DIN+ — DIN−)= 100mVpp@2.5MHz	5	—	11	KΩ
Differential Input Capacitance	V(DIN+ — DIN−)= 100mVpp@2.5MHz	—	—	6.0	pF
Common Mode Input Impedance	(both sides)	—	2.0	—	KΩ
Comparator Offset Voltage	HYS pin at GND $\leqslant$1.5KΩ across DIN+, DIN−	—	—	10	mV
Peak Hysteresis Voltage vs HYS pin voltage (input referred)	$1\text{V} < \text{V (HYS)} < 3\text{V}$	—	0.21	—	V/V
HYS Pin Input Current	$1\text{V} < \text{V (HYS)} < 3\text{V}$	0.0	—	−20	μA
LEVEL Pin Max Output Current	—	3.0	—	—	mA
LEVEL Pin Output Resistance	I (LEVEL)= 0.5mA	—	180	—	Ω

Parameter	Test Conditions	Min.	Typ.	Max.	Units
HYSTERESIS COMPARATOR (cont.)					
DOUT Pin Output Low Voltage	0.0≤ IOL≤ 0.5mA	VDD-4.0	—	VDD-2.8	V
DOUT Pin Output High Voltage	0.0≤ IOH≤ 0.5mA	VDD-2.5	—	VDD-1.8	V
ACTIVE DIFFERENTIATOR					
Input Signal Range	—	—	—	1.5	Vpp
Differential Input Resistance	V(CIN+ — CIN−)= 100mVpp @ 2.5 MHz	5.8	—	11.0	KΩ
Differential Input Capacitance	V(CIN+ — CIN−)= 100mVpp@ 2.5 MHz	—	—	6.0	pF
Common Mode Input Impedance	(both sides)	—	2.0	—	KΩ
DIF+ to DIF− Pin Current	Differentiator Impedance must be set so as not to clip signal at this current level.	±1.3	—	—	mA
Comparator Offset Voltage	DIF+, DIF− AC Coupled	—	—	10.0	mV
COUT Pin Output Low Voltage	0.0 ≤ IOH≤ 0.5mA	—	VDD-3.0	—	V
COUT Pin Output Pulse Voltage V(high)-V(low)	0.0≤ IOH≤ 0.5mA	—	+0.4	—	V
COUT Pin Output Pulse Width	0.0≤ IOH≤ 0.5mA	—	30	—	nS

OUTPUT DATA CHARACTERISTICS (REF. FIG. 2) Unless otherwise specified V(CIN+ − CIN−) = V(DIN+ − DIN−) = 1.0Vpp AC coupled since wave at 2.5MHz differentiating network between DIF+ and DIF− is 100Ω in series with 65pF, V (Hys) = 1.8DC, a 60pF capacitor is connected between OS and VCC, RD- is loaded with a 4Ω resistor to VCC and a 10pF capacitor to GND.

Parameter	Test Conditions	Min.	Typ.	Max.	Units
D-Flip-Flop Set Up Time (Td1)	Min delay from V(DIN+ DIN−) exceeding threshold to V(DIF+ — DIF−) reaching a peak	0	—	—	nS
Propagation Delay (Td3)	—	—	—	110	nS
Output Data Pulse Width Variation	Td5 = 670 Cos, 50 pF ≤Cos ≤ 200 pF	—	—	±15	%
Logic Skew Td3 — Td4	—	—	—	3	nS
Output Rise Time	VOH = 2.4V	—	—	14	nS
Output Fall Time	VOL = 0.4V	—	—	18	nS

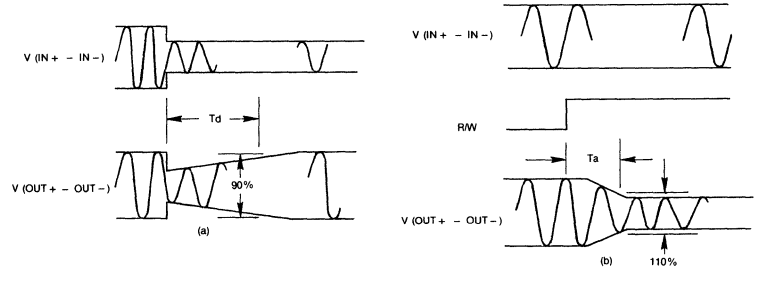


Fig. 1: AGC Timing Diagram

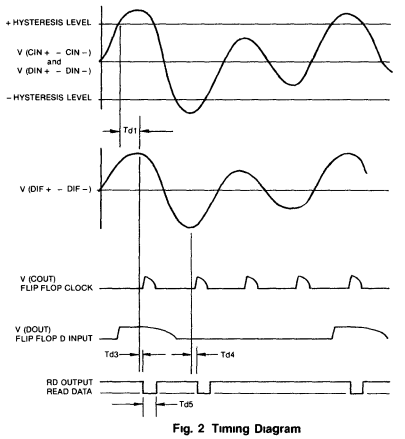


Fig. 2 Timing Diagram

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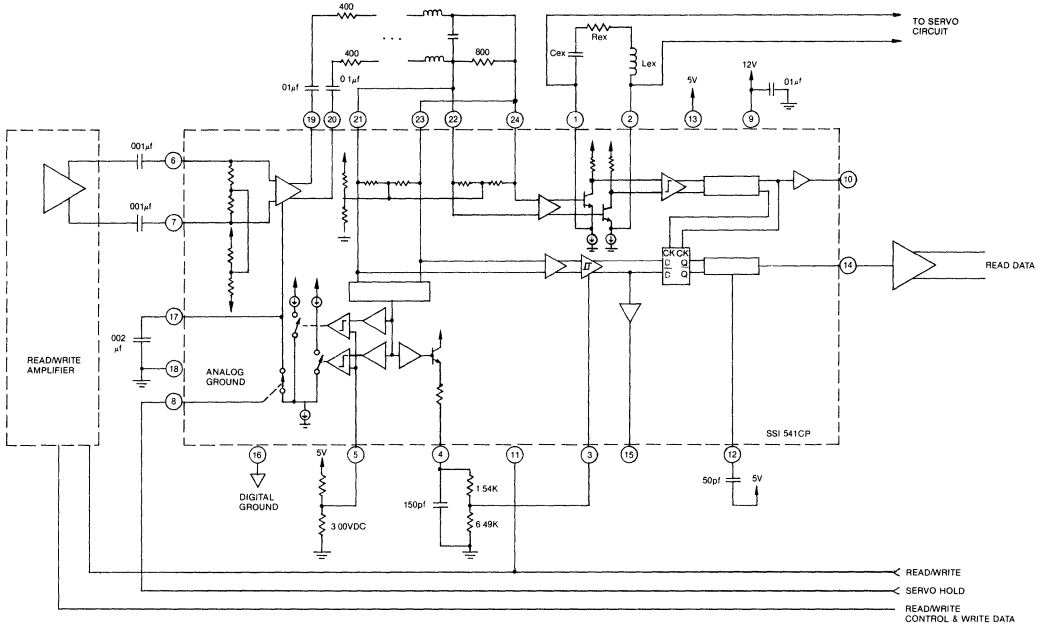
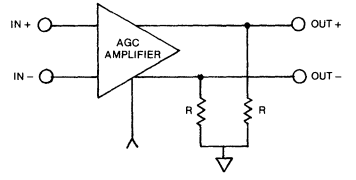


NOTE Circuit traces for the 12V bypass capacitor and the AGC hold capacitor should be as short as possible with both capacitors returned to the Analog Ground pin

Fig. 3: TYPICAL READ/WRITE ELECTRONICS SET UP
(component values, where given, are for a 5MB/sec system)

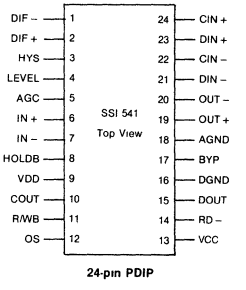
Fig. 4: Modification of AGC Amplifier Output Current to drive low impedance filters.



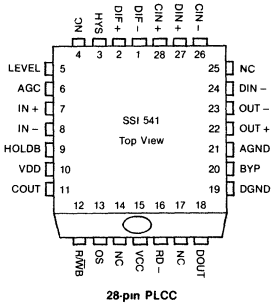
$$\text{OUT + to OUT – Pin Current Change} = \pm 3.2\ \text{mA} \frac{R}{\text{Rint}}$$

where Rint = 800Ω

SSI 541 Pin Assignments



24-pin PDIP



28-pin PLCC

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SSI 545
Winchester Disk Drive Support Logic

Preliminary Data Sheet

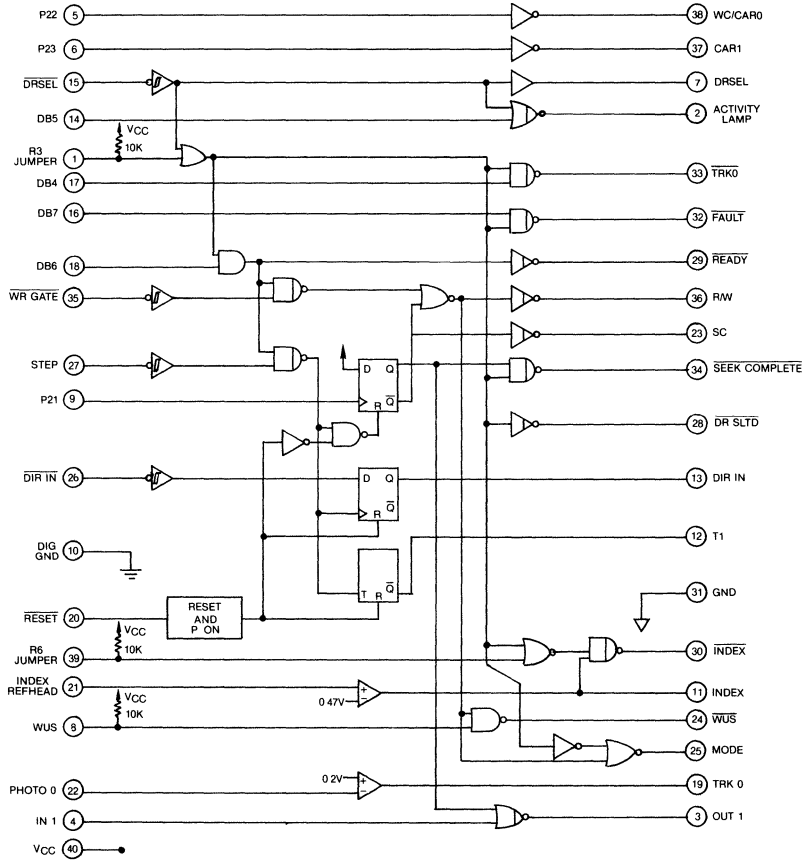
DESCRIPTION

The SSi 545 is an integrated circuit which consolidates functions in a Winchester Disk Drive normally performed by a variety of LSTTL SSI and MSI devices. Various gates, comparators and flip-flops are used to format signals compatible with the ST 506 interface requirements. All ST 506 connections have the necessary output drive or input hysteresis consistent with bus signal needs. The SSi 545 uses a single +5 volt supply and is available in 40 pin DIP and 44 pin QUAD packages.

FEATURES

- **Reduces package count in 5¼" and smaller Winchester Disk Drives.**
- **Replaces bus interface and combinatorial logic devices between the ST 506 bus and on board processor and mechanical interfaces.**
- **Surface mount package available for further real estate reduction.**

SSI 545 LOGIC DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component

ABSOLUTE MAXIMUM RATINGS

Characteristic ..... Rating
VCC supply voltage ..... 7 volts
Storage temperature ..... -65°C to +150°C
Ambient operating temperature ..... 0°C to +70°C
Logic input voltage ..... -0.5 VDC to 7.0 VDC
Lead temperature (soldering 10 sec) ..... 260°C

ELECTRICAL CHARACTERISTICS Unless otherwise specified: 4.5 < Vcc < 5.5V; 0 deg C < Ta < 70 deg C

Parameter	Test Condition	Min.	Max.	Units
LOGIC OUTPUTS Refer to table 1 for output type, pin number cross reference				
TYPE 01 (OPEN COLLECTOR) OUTPUTS				
Output High Current	V_{OH} = 5.5V	–	250	μA
Output Low Voltage	I_{OL} = 16mA	–	0.5	V
TYPE 02 (TOTEM POLE) OUTPUTS				
Output High Voltage	I_{OH} = −400 μA	2.5	–	V
Output Low Voltage	I_{OL} = 8mA	–	0.5	V
Short Circuit Current		–	−100	mA
TYPE 03 (OPEN COLLECTOR) OUTPUTS				
Output High Current	V_{OH} = VCC	–	50	μA
Output Low Voltage	I_{OL} = 30mA	–	0.8	V
TYPE O4 (OPEN COLLECTOR) OUTPUTS				
Output High Current	V_{OH} = 5.5V	–	250	μA
Output Low Voltage	I_{OL} = 48mA	–	0.5	V
LOGIC INPUTS				
TYPE I1 INPUTS				
Input High Voltage		2.0	–	V
Input Low Voltage		–	0.8	V
Input Low Current	V_{IL} = 0.5V	–	−0.8	mA
Input High Current	V_{IH} = 2 4V	–	400	μA
TYPE I2 (SCHMIDT TRIGGER) INPUTS				
Threshold Voltage	Positive going, VCC = 5V	1.3	2.0	V
	Negative going, VCC = 5V	0.6	1.1	V
Hysteresis	VCC = 5V	0.4	–	V
Input High Current	V_{IH} = 2.4V	–	40	μA
Input Low Current	V_{IL} = 0.5V	–	−0.8	mA
TYPE I3 (INTERNAL PULLUP) INPUTS				
Input High Voltage		2.0	–	V
Input Low Voltage		–	0.8	V
Input Low Current	V_{IL} = 0.5V	–	−1.2	V

Parameter	Test Condition	Min.	Max.	Units
COMPARATOR INPUTS				
Threshold Voltage	Index Ref Positive going	–	580	mV
	Negative going	370	–	mV
	Photo 0 Positive going	–	280	mV
	Negative going	120	–	mV
Hysteresis		30 typ	–	mV
Input Resistance	VCC = 5.0V, 0<Vin<VCC	10	–	kΩ
TIMING CHARACTERISTICS Ta = 25°C, CL = 25 pF				
Propogation Delay Time, Input to Output	P22 to WC/CAR0	–	40	nS
	P23 to CAR0	–	40	nS
	DB5 to ACTIVITY LAMP	–	40	nS
	DB4 to TRCK0 –	–	40	nS
	DB7 to FAULT–	–	40	nS
	DRSEL– to DRSEL	–	55	nS
	DRSEL– to ACTIVITY LAMP	–	55	nS
	WUS to WUS–	–	55	nS
	DB6 to READY–	–	55	nS
	WRGATE– to R/W–	–	60	nS
	STEP– to SC, DIR IN, to T1	–	100	nS
	P21 to SC	–	100	nS
	P21 to R/W–	–	120	nS
Data Setup Time	DIRIN– reference to STEP	–	50	nS
Data Hold Time	DIRIN– to STEP	–	5	nS
Delay Time	INDEX REF HEAD to INDEX, with 500 mV input step	–	250	nS
	PHOTO0 to TRK0 with 500mV input step	–	250	nS

TABLE 1

Pin Number		I/O Type	Pin Name
40 PIN DIP	44 PIN QUAD*		
1	1	I3	R3JUMPER
2	2	03	ACTIVITYLAMP
3	3	01	OUT1
4	4	I1	IN1
5	5	I1	P22
6	7	I1	P23
7	8	02	DRSEL
8	9	I3	WUS
9	10	I1	P21
10	11		GROUND
11	12	02	INDEX
12	13	02	T1
13	14	02	DIRIN
14	15	I1	DB5
15	16	I2	DRSEL
16	18	I1	DB7
17	19	I1	DB4
18	20	I1	DB6
19	21	02	TRK0
20	22	I1	RESET

Pin Number		I/O Type	Pin Name
40 PIN DIP	44 PIN QUAD*		
21	23	COMPARATOR	INDEXREFHEAD
22	24	COMPARATOR	PHOTO0
23	25	02	SC
24	26	02	WUS
25	27		MODE
26	29	I2	DIRIN
27	30	I2	STEP
28	31	04	DR SLTD
29	32	04	READY
30	33	04	INDEX
31	34		GROUND
32	35	04	FAULT
33	36	04	TRK0
34	37	04	SEEKCOMPLETE
35	38	I2	WRGATE
36	40	01	R/W
37	41	01	CAR1
38	42	01	WC/CAR0
39	43	I3	R6JUMPER
40	44		+VCC

*PINS 6, 17, 28, and 39 are not connected in the 44 Pin QUAD package

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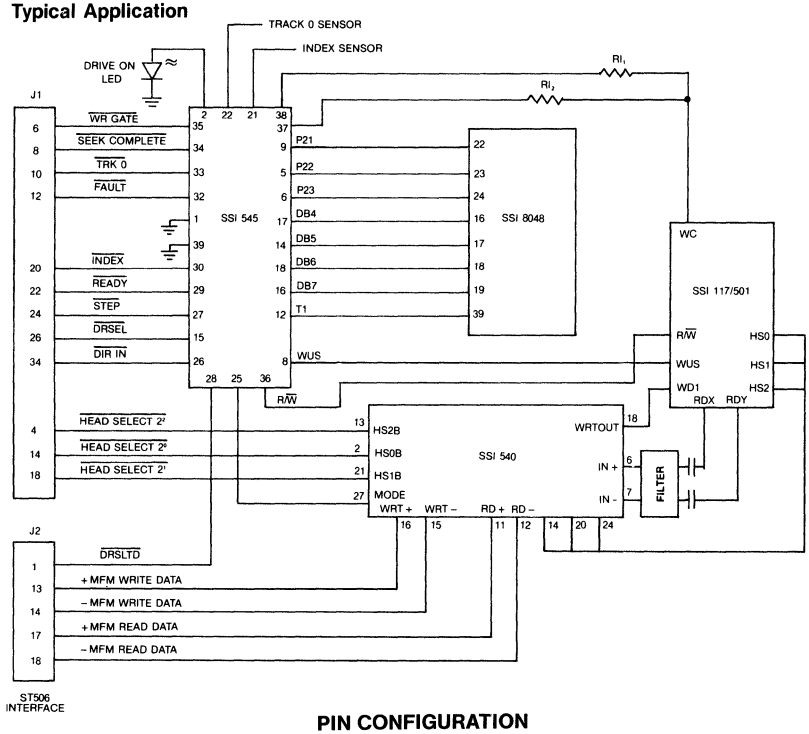
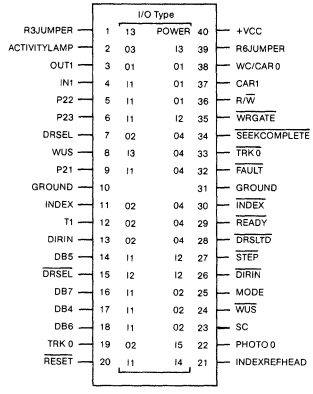
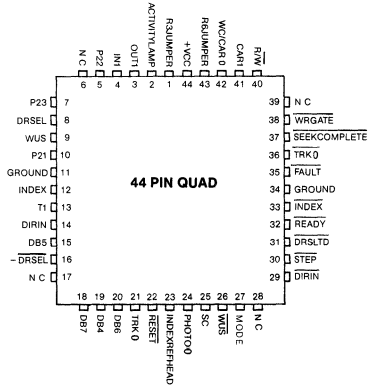
Typical Application



PIN CONFIGURATION



40 PIN DIP



Note 1 Pins named N C have no internal interconnect and may be used for cross unders

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SSI 590
5-1/4 Inch
Motor Speed Control

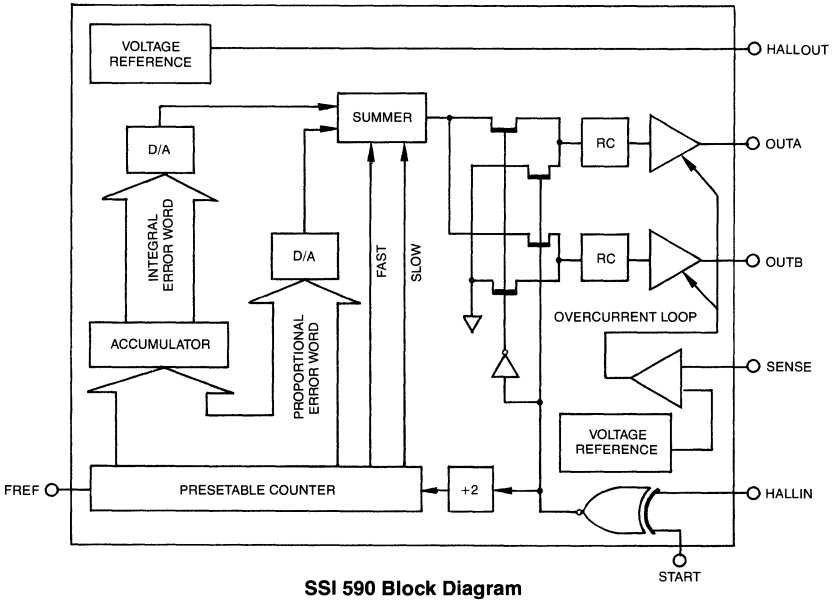
Preliminary Data Sheet

GENERAL DESCRIPTION:

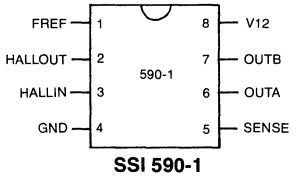
The SSI 590 is a motor controller IC designed to provide all timing and control functions necessary to start, drive and brake a two-phase, four-pole, brushless DC spindle motor. The IC requires two external power transistors (such as Darlington power transistors), three external resistors, and an external frequency reference. The motor Hall sensor is directly driven and decoded by the device. The controller is optimized for a 3600 rpm disc drive motor using a 2 Mega-Hertz clock. Motor protection features include stuck rotor shutdown, coil over-current detection and control, and supply fault detection. The device's linear control loop controls the power drivers using Pulse Amplitude Modulation.

FEATURES:

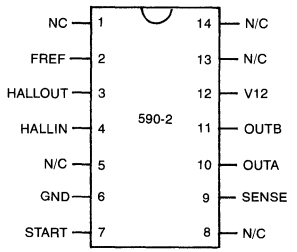
- **Available in 8 pin DIP (SSI 590-1) or 14 pin DIP (SSI 590-2).**
- **CMOS with single + 12 volt power supply.**
- **All motor START, DRIVE, AND STOP timing and control.**
- **Includes Hall-Effect sensor drive and input pins.**
- **Highly accurate speed regulation of +/− .035%.**
- **Active braking function (590-2 only).**
- **On-chip digital filtering requires no external compensation or adjustments.**
- **Provides protection against stuck rotor, coil over-current, and supply fault.**
- **Regenerative braking with shutdown.**



SSI 590 Block Diagram



SSI 590-1



SSI 590-2

Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.

CONTROL LOOP DESCRIPTION:
The device incorporates both analog and digital circuit techniques to utilize the advantages of each. The analog portion of the loop uses switched capacitor filter technology to eliminate external components. The control loop uses a Pulse Amplitude Modulation (PAM) control scheme to avoid the switching transients and torque ripple inherent in Pulse Width Modulation (PWM) schemes.

A binary counter is preset once per motor revolution by an index signal generated by the hall position sensor. On the next index pulse, the remaining least significant bits are loaded into the proportional D/A and accumulated by a saturating accumulator. The most significant bits are loaded into the integral D/A. The size of the accumulator and the bit locations determine the major scaling (within a factor of two) for the gain and zero location of the filter. To prevent overflow in the proportional D/A the counter is decoded to detect overflow, and the proportional D/A is saturated as needed. The overflow also generates a boost signal used in the summer. The range of the accumulator is larger than the linear range of the proportional channel to help filter small load disturbances that tend to saturate the proportional channel. The entire counter is also used to provide a time-out feature to protect the motor and external circuitry.

INPUT/OUTPUT PIN DESCRIPTION:

* **FREF (frequency reference input)**
A TTL compatible input used by the device to set and maintain the desired motor speed and operate circuit blocks.

* **HALLOUT**
Provides a regulated bias voltage for the Hall effect sensor inside the motor.

* **HALLIN (Hall sensor input)**
The TTL open-collector type output of the motor's Hall switch feeds this input which has a resistor pullup to the HALLOUT bias voltage. Refer to figure 1 for input timing.

* **OUTA, OUTB (driver outputs)**
These two driver outputs drive the external power transistors, such as TIP120 NPN darlington power transistors as shown in the typical application. The power transistors control the motor current through the current setting resistor Re. The motor current is V(sense)/Re. During normal operation, the drive voltages are adjusted as necessary to maintain the proper motor speed and drive current. Regenerative braking is accomplished with self biasing of the power transistors thru resistors Rb with power shutdown. Refer to figure 1 for output timing.

* **SENSE (coil current sense line)**
Senses the coil current and limits the sense voltage to the threshold by limiting the drive to the external power transistors.

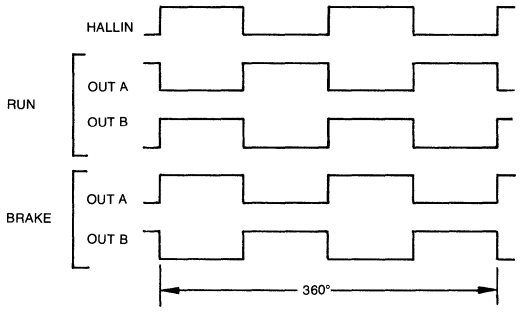


FIGURE 1 = SSI 590 Firing Order

* **START (active brake control, only available on 14 pin package)**
The active brake is enabled by applying a logic "0" to the START pin. During active braking the output phasing is reversed to apply a reverse torque to the motor until the motor period drops below the reverse shutdown speed at which time the drivers turn off the external power transistors to deny power to the motor. Active braking is shown in figure 1.

* **N/C (no connection, 14 pin package only)**
These pins must remain unconnected and floating.

PROTECTION FEATURES:

* **LOW VOLTAGE DETECTION**

If the supply drops below the detect threshold the device will turn off all of the external power transistors to prevent damage to the motor and the power devices.

* **STUCK ROTOR SHUTDOWN**
If the delay from power onset to a positive Index transition or the time interval between successive Index transitions is greater than the prescribed time, the device interprets this delay as a stuck rotor and reduces the motor current to zero until such time as one positive HALLIN transition is detected or until power is removed and reapplied.

* **MOTOR COIL OVER-CURRENT**
Refer to SENSE input description. Sense voltage is generated by current through Re shown in the typical application. The SENSE input threshold limits the maximum coil current.

ABSOLUTE MAXIMUM RATINGS:

Positive Supply Voltage, V_{DD} 14V
Storage Temperature ..... −65 deg. C to +125 deg. C
Ambient Operating Temperature ...0 deg. C to +70 deg. C
HALLIN, FREF, START, and SENSE input voltages. .....
−0.3V to V_{DD}+0.3V
HALLOUT Current 10mA
Lead Temperature (soldering, 10 sec.) ..... 260 deg. C
Power Dissipation 400mW

ELECTRICAL CHARACTERISTICS Unless otherwise specified, 10.8V ≤ V12 ≤ 13.2V; 0 deg. C ≤ TA ≤ 70 deg. C; FREF = 2.00MHz; Re = 0.4 Ohms ±10% (2 watt); Rb = 4.7 Kohm±10% (¼ WATT); 0.8 ≤ Darlington Vbe ≤ 1.8

Motor Parameters: (1 to 3 platters)

KT Torque constant = 0.015 Nt-m/amp ±10%
J Inertia = 0.000489 Nt-m/s/s ±33%
KD Damping factor = 0.0000318 Nt-m/rad/sec ±33%

where: $\frac{\text{Motor frequency(s)}}{\text{Motor Current(s)}} = \frac{KT}{J \times s + KD}$

Characteristic	Test Condition	Min.	Max.	Unit
POWER SUPPLY CURRENT				
ICC (Includes Drive Outputs)		(17 typ)	30	mA
FREF AND START INPUTS				
Input Low Voltage	Iil = 500μA	—	0.8	V
Input High Voltage	Iih = 100μA	2.0	—	V
HALL SENSOR INTERFACE				
HALLOUT Bias Voltage	I = 5mA	5.0	6.8	V
HALLOUT Pullup Resistance	To HALLOUT Pin	5	20	Kohms
Input Low Voltage		—	1.0	V
Input High Voltage		4.0	—	V
DRIVER OUTPUTS				
Sink Capability	VOUTA or VOUTB = 0.5 Volts	5.0	—	mA
Source Capability	VOUTA or VOUTB = 3.0 Volts	−5.0	—	mA
Capacity Load Drive Capability		—	50.0	pF
SENSE INPUT				
Threshold Voltage		0.9	1.1	V
Input Current		−100	100	μA
Input Capacitance		—	25.0	pF
STUCK ROTOR DETECTION				
Shutdown Time	Power on To Driver	0.815	0.935	sec
LOW VOLTAGE DETECTION				
Detect Threshold		6.0	9.0	V
CONTROL LOOP—DESCRIPTION*				
Divider Ratio	FREF/Avg. Motor Frequency	16664	16672	—
Index to Index Jitter	Total Jitter	—	8.0	μsec
Loop Gain H (2 × π × f)	f = 2Hz	0 Typical		dB
Loop Zero	Kp/Ki	0.97	1.03	Hz

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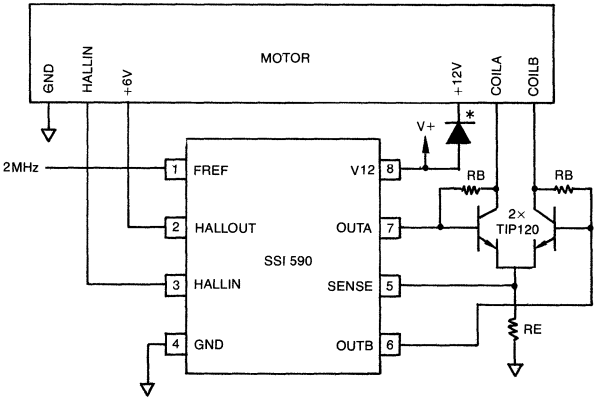
Characteristic	Test Condition	Min.	Max.	Unit
CONTROL LOOP Vs SUPPLY VARIATION				
Kp(V12 = 13.2V) / Kp(V12 = 10.8V)		0.96	1.04	—
Ki(V12 = 13.2V) / Ki(V12 = 10.8V)		0.96	1.04	—

Characteristic	Test Condition	Typ.	Max.	Unit
START/STOP VELOCITY PROFILES				
Power on Delay to FHALL Greater than FREF/16668	1 Platter 2 Platters 3 Platters	7.0 9.0 11.0	11.0 13.0 15.0	sec sec sec
Speed Overshoot FHALL—(FREF/16668) / (FREF/16668)	1 Platter 2 Platters 3 Platters	0.5 0.5 0.5	2.0 2.0 2.0	% % %
Settling Time: Motor Frequency Settles to 0.05%	1 Platter 2 Platters 3 Platters	9.0 11.0 13.0	13.0 15.0 17.0	sec sec sec
Stop Time (Regenerative): Motor Frequency Slows to 30% after Power is Removed	1 Platter 2 Platters 3 Platters	7.0 8.0 9.0	13.0 15.0 17.0	sec sec sec
Stop Time (Active):		4.0		sec

*The continuous Time Transfer Function of the On Chip Control can be modeled as follows $H(s) = \frac{Vc(s)}{F(s)} = K_I \times \frac{(1 + s/(2 \times \pi \times (K_p/K_I)))}{s}$ K_I = Integral gain, K_p = Proportional gain

TYPICAL APPLICATION



*NOTE DIODE REQUIRED FOR REGENERATIVE BRAKING (THREE AMP MINIMUM RATING)

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SSI 591
Three-Phase 5¼ Inch Winchester Motor Speed Control

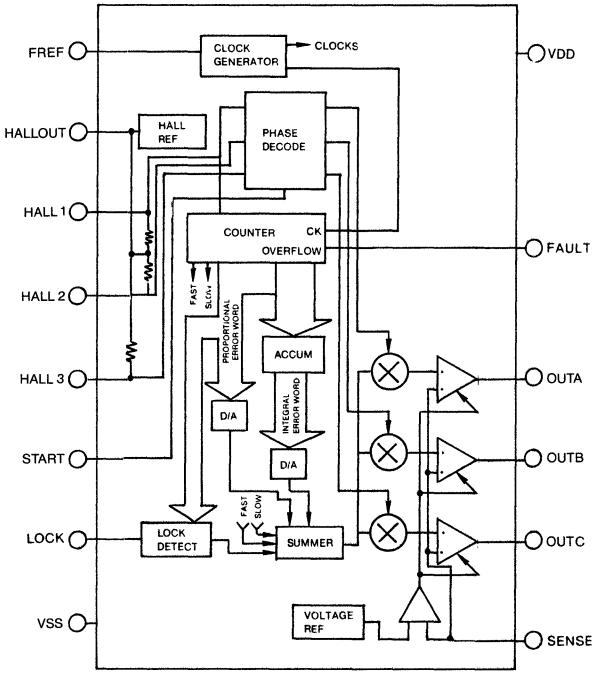
Preliminary Data Sheet

General Description

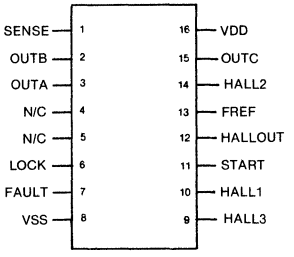
The SSI 591 is a motor controller IC designed to provide all timing and control functions necessary to start, drive and brake a three-phase brushless DC spindle motor. The IC requires three external power transistors (such as Darlington power transistors), one external power resistor, and an external frequency reference. The three motor Hall sensors are directly driven and decoded by the device. The controller is optimized for a 3600 rpm disc drive motor using a 2 Mega-Hertz clock. Motor protection features include stuck rotor shutdown, supply and clock fault detection, all of which are indicated by a FAULT signal, and coil over-current detection and control. A LOCK signal is provided to indicate that the motor is at speed. The device's linear control loop controls the power drivers using Pulse Amplitude Modulation.

FEATURES:

- **CMOS with TTL/LSTTL compatible control functions**
- **Single + 12 volt power supply**
- **All motor START, DRIVE, AND STOP timing and control.**
- **Includes Hall-Effect sensor drive and input pins.**
- **Highly accurate speed regulation of +/— .05%.**
- **Active braking function.**
- **On-chip digital filtering requires no external compensation of adjustments.**
- **Provides protection against stuck rotor, motor coil over-current, supply fault, or clock fault.**
- **At speed indication provided.**

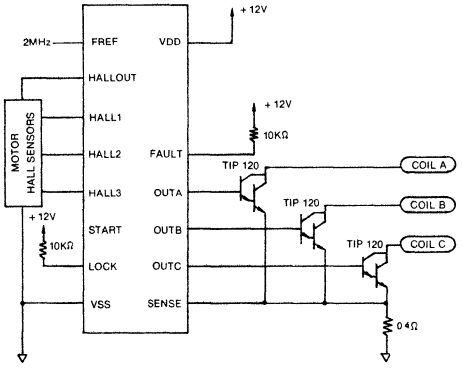


SSI 591 Block Diagram



SSI 591 Pin Out
(Top View)

TYPICAL APPLICATION



CAUTION: Use handling procedures necessary for a static sensitive component.

CONTROL LOOP DESCRIPTION

The device incorporates both analog and digital circuit techniques to utilize the advantages of each. The analog portion of the loop uses switched capacitor filter technology to eliminate external components. The control loop uses a Pulse Amplitude Modulation (PAM) control scheme to avoid the switching transients and torque ripple inherent in Pulse Width Modulation (PWM) schemes.

A binary counter is preset once per motor revolution by an index signal generated by Hall position sensor 1. On the next index pulse, the remaining least significant bits are loaded into the proportional D/A and accumulated by a saturating accumulator. The most significant bits are loaded into the integral D/A. The size of the accumulator and the bit locations determine the major scaling (within a factor of two) for the gain and zero location of the filter. To prevent overflow in the proportional D/A, the counter is decoded to detect overflow and the proportional D/A is saturated as needed. The overflow also generates a boost signal used in the summer. The range of the accumulator is larger than the linear range of the proportional channel to help filter small load disturbances that tend to saturate the proportional channel. The entire counter is also used to provide a time-out feature to protect the motor and external circuitry.

INPUT/OUTPUT PIN DESCRIPTION

* **FREF (frequency reference input)**
  A TTL compatible input used by the device to set and maintain the desired motor speed and operate circuit blocks.
* **HALLOUT (Hall sensor bias output)**
  Provides a regulated bias voltage for the Hall effect sensors inside the motor.
* **HALL1, HALL2, HALL3 (Hall sensor inputs)**
  The TTL open-collector type outputs of the motor's Hall switches feed these inputs which have a resistor pullup to the HALLOUT bias voltage. The HALL1 input is used to index the control loop counter. Refer to figure 1 for input timing.
* **OUTA, OUTB, OUTC (driver outputs)**
  These three driver outputs drive the external power transistors, such as TIP120 NPN darlington power transistors shown in typical application. The power transistors control the motor current through the current setting resistor Re. The motor current is V(sense)/Re. During normal operation, the drive voltages are adjusted as necessary to maintain the proper motor speed and drive current. Refer to figure 1 for output timing.

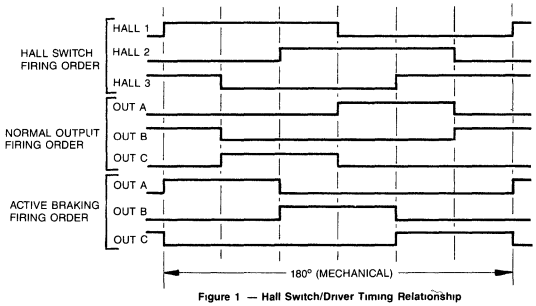


Figure 1 — Hall Switch/Driver Timing Relationship

* **SENSE (coil current sense input)**
  Senses the coil current and limits the sense voltage to the threshold by limiting the drive to the external power transistors.
* **LOCK (at speed indicator output)**
  An open drain LSTTL compatible output that indicates with an active low that the period of the motor is within the controllers linear range. Because of the accuracy of the loop, the LOCK pin is a good "at speed" indicator.
* **START (active brake control input)**
  The active brake is enabled by appling a logic "0" to the START pin. During active braking the Hall sensor's phasing is changed to apply a reverse torque to the motor until the motor period drops below the reverse shutdown speed at which time the drivers turn off the external power transistors to deny power to the motor. Active braking is shown in figure 1.
* **FAULT (fault indicator output)**
  Goes high when the motor is determined to be stalled, V_{DD} is low, or FREF clock is too slow.
* **N/C (no connection)**
  These pins must be left unconnected and floating.

PROTECTION FEATURES:

* **LOW VOLTAGE DETECTION**
  If the supply drops below the detect threshold, the device will turn off all of the external power transistors to prevent damage to the motor and the power devices. The FAULT pin goes high in this condition.
* **STALLED ROTOR SHUTDOWN**
  If the delay from power onset to a positive Index transition or the time interval between successive Index transitions is greater than the prescribed time, the device interprets this delay as a stalled rotor and reduces the motor current to zero until such time as one positive Index transition is detected or until power is removed and reapplied. The FAULT output goes high when the motor is determined to be stalled.

* **MOTOR COIL OVER-CURRENT**
  Refer to SENSE input description. Senses voltage is generated by current through Re shown in the typical application. The SENSE input threshold limits the maximum coil current.

* **FREF CLOCK FAULT**
  If the FREF frequency drops below the specified minimum frequency, the driver will shut down and the FAULT pin will go high.

ABSOLUTE MAXIMUM RATINGS:

Positive Supply Voltage, V_{DD} 14V
Storage Temperature . . . . . —65 °C to + 125 °C
Ambient Operating Temperature . . . . . 0 °C to + 70 °C
Pin Voltage (except FAULT and LOCK) . . . . . —0.3V to V_{DD} + 0.3V
FAULT and LOCK Pin Voltage . . . —0.3V to V_{DD} + 5.0V
HALLOUT Current 20mA
Lead Temperature (soldering, 10 sec) . . . . . 260 °C
Power Dissipation 400mW

ELECTRICAL CHARACTERISTICS Unless otherwise specified, 10.8V ≤ V_{DD} ≤ 13.2V; 0 °C ≤ TA ≤ 70 °C; FREF = 2.000MHz; Re = 0.4 Ohms; Motor Configuration is 4-pole 3-phase center-tap "Y";

Motor parameters:

Torque constant (KT)	0.015 Nt-m/Amp	
Inertia (J)	0.000489 Nt-m-sec**2	where: [1]
Damping Factor (KD)	0.0000318 Nt-m/rad/sec	

$$\frac{\text{Motor Frequency (s)}}{\text{Motor Current (s)}} = \frac{KT}{J*s + KD}$$

Winding resistance [2] 2.0 Ohms
Winding inductance 2.0 mH
Back EMF [2] 0.0159 V/rad/sec

Characteristic	Test Condition	Min.	Max.	Unit
POWER SUPPLY CURRENT				
ICC	Clock Active I(HALLOUT) = 15mA 1 Driver loaded to = 5 mA 2 Drivers unloaded	—	30	mA
INPUT LOGIC SIGNALS — 'FREF' and 'START' INPUTS				
Vil, Input Low Voltage		—	0.8	V
Iil, Input Low Current	Vin = 0	—500	—	μA
Vih, Input High Voltage		2.0	—	V
IiH, Input High Current	Vin = 5	—	100	μA
Input Capacitance		—	25	pF
OUTPUT LOGIC SIGNALS — 'LOCK' and 'FAULT' PINS				
Vol	Isink = 2mA	—	0.4	V
Ioh	Vout = V_{DD}	—	10	μA
HALL SENSOR INTERFACE				
HALLOUT Bias Voltage	I = 0 to —15mA	5.0	6.8	V
HALL1, 2, 3 Pullup Resistance	to Hallout pin	5	20	KΩ
Input Low Voltage		—	1.0	V
Input High Voltage		4.0	—	V
Input Capacitance		—	25	pF

Notes [1] The motor parameters given are for a typical motor The device will work for a range of motors near this nominal motor

[2] The motor must have a back EMF less than 10 volts peak (measured from center tap to drive transistor collector/drain) at speed to insure linear operation of drive transistors and a coil resistance small enough to insure adequate start current

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Parameter	Test Conditions	Min.	Max.	Units
DRIVER OUTPUTS				
Sink Capability	Vol = 0.5V	1.0	—	mA
Source Capability	Voh = 3.0V	—5.0	—	mA
Capacitive Load Drive Capability		—	50.0	pF
SENSE INPUT AND OVER-CURRENT CONTROL				
Threshold Voltage		0.9	1.1	V
Input Current		—100	100	μA
Input Capacitance		—	25.0	pF
FAULT DETECTION				
Stalled Rotor Shutdown Time	Power On to driver	0.850	0.900	sec
Low Voltage Detect Threshold		6.8	9.0	V
Low FREF Shutdown Threshold		—	100	Hz
LOCK INDICATION				
Lock Range	Motor Speed	3585	3615	Hz

CONTROL LOOP PARAMETERS*

Parameter	Test Condition	Min.	Typ.	Max.	Units
Divider Ratio	FREF/Fmotor	—	33336	—	—
Instantaneous Speed Error	Referenced to 60Hz	—0.035	0.01	0.015	%
Index to Index Jitter [16/FREF]	Total jitter	—	—	8	μsec.
Loop Bandwidth	Nominal motor Re = 0.40Ω	—	2	—	Hz
Loop Zero	Ki/Kp	—	1.0	—	Hz
Maximum Running Current	Re = 0.40Ω	1.50	—	—	Amps
Minimum Running Current	Re = 0.40Ω	—	—	0	Amps
Start Current	Re = 0.40Ω	2.25	—	2.75	Amps

***CONTROL LOOP NOTES:**
Running current limits refer to capabilities during speed correction.

The motor control loop consists of counters, logic, and digital-to-analog converters that provide loop time constants The continuous time transfer function of the on chip control can be modeled as follows.

$$H(s) = \frac{Vc(s)}{Fm(s)} = \frac{Ki}{s} + Kp$$

Vc(s) is the voltage applied to the external current setting resistor (RE) by the modulator. By adjusting the value of Re the gain the motor sees can be adjusted, as can the starting current

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SSI 570
2-Channel Floppy Disk Read/Write Circuit

Preliminary Data Sheet

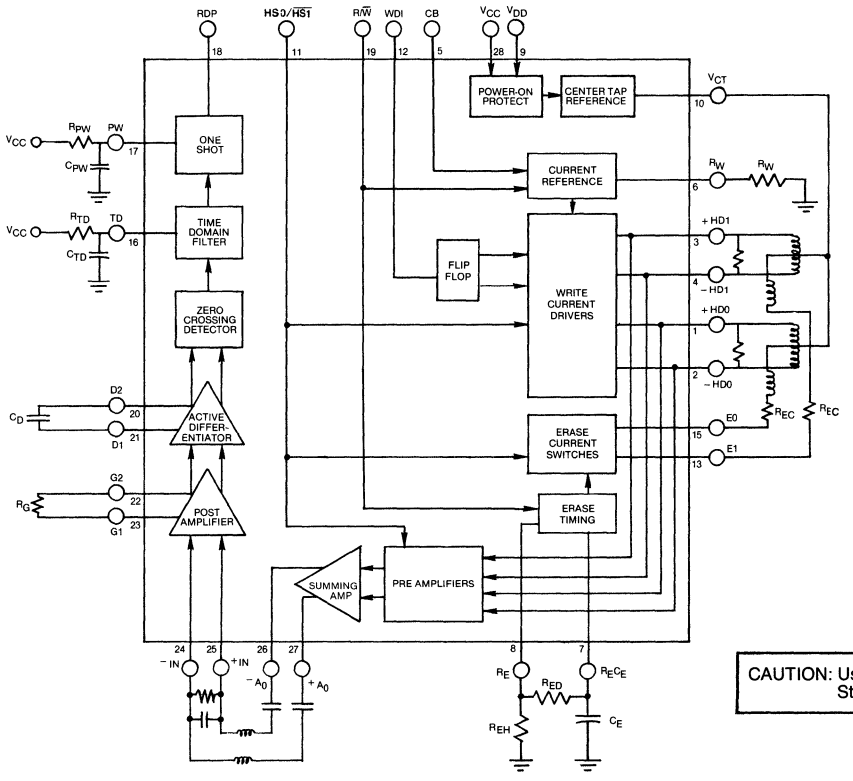
GENERAL DESCRIPTION

The SSI 570 is an integrated circuit which performs the functions of generating write signals and amplifying and processing read signals required for a double sided floppy disk drive. The write data circuitry includes switching differential current drivers and erase head drive with programmable delay and hold times. The read data circuitry includes low noise amplifiers for each channel as well as a programmable gain stage and necessary equalization and filtering capability using external passive components. All logic inputs and outputs are TTL compatible and all timing is externally programmable for maximum design flexibility. The circuit operates on +12 volt and +5 volt power supplies and is available in 28 pin plastic DIP and QUAD packages.

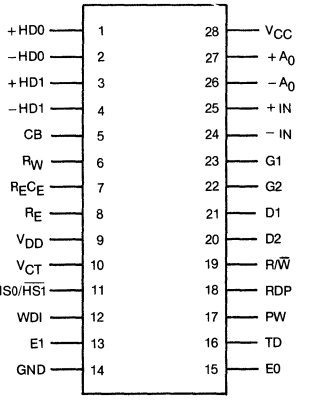
FEATURES

- **Single chip read/write amplifier and read data processing function.**
- **Compatible with 8", 5¼", and 3½" drives.**
- **Internal write and erase current sources, externally set.**
- **Internal center tap voltage source.**
- **Control signals are TTL compatible.**
- **Schmitt trigger inputs for higher noise immunity on bussed control signals.**
- **TTL selectable write current boost.**
- **Operates on +12 volt and +5 volt power supplies.**
- **High gain, low noise, low peak shift (0.3% Typ) read processing circuits.**

SSI 570 Block Diagram



SSI 570 Pin Out (Top View) (DIP & QUAD Pkgs)



CAUTION: Use handling procedures necessary for a Static Sensitive Component.

SSI 570
2-Channel
Floppy Disk
Read/Write Circuit

Circuit Operation

WRITE MODE CIRCUITRY

In Write Mode (R/$\overline{W}$ low), the circuit provides controlled write and erase currents to either of two magnetic heads. The Write-Erase circuitry consists of two differential Write Current Drivers, a Center Tap Voltage Reference, two Erase Current Switches and control circuits for head selection and erase timing.

Write current is toggled between opposing sides of the head on each negative transition of the Write Data Input (WDI) and is set externally by a single resistor, R_W, connected between the R_W terminal and ground. Since driver output impedance is large, proper damping resistors must be provided across each head. A signal at the CB terminal provides write current boost.

Erase current is also set externally through resistors R_{EC} connected in series with each erase coil. Erase can be activated by, but delayed from, selection of the write mode, and is held active after mode deselection. The turn-on delay is determined by the charging of C_E through R_{ED}, while the hold time is determined by the discharge of C_E through the series combination of R_{ED} and REH (see connection diagram). The R_EC_E node may be driven directly by a logic gate, with external resistors per fig. 4, if the erase period is to be controlled separately from the write mode selection. For applications where no delays are required, C_E is omitted.

The Center Tap Voltage Reference supplies both write and erase currents. A Power Turn-On protection circuit prevents undesired writing or erasure by holding the voltage reference off until the supply voltages are within their operating ranges.

READ MODE CIRCUITRY

In the Read Mode (R/$\overline{W}$ high), the circuit performs the functions of amplifying and detecting the selected head output pulses which correspond to magnetic transitions in the media. The Read circuitry consists of two differential Preamplifiers, a Summing Amplifier, a Postamplifier, an Active Differentiator, a Zero-Crossing Detector, a Time Domain Filter, and an Output One-Shot.

The selected Preamplifier drives the Summing Amplifier whose outputs are AC coupled to the Postamplifier through an external filter network. The Postamplifier adjusts signal amplitudes prior to application of signals to the Active Differentiator. Postamplifier gain is set as required by connecting a resistor across the gain terminals, G1 and G2. If desired, an additional frequency/phase compensation network may also be connected across these gain terminals.

The Differentiator, driven by the Postamplifier, provides zero-crossing output voltages in response to input signal peaks. Differentiator response characteristics are set by an external capacitor or more complex series network connected between the D1 and D2 terminals.

The Zero-Crossing Detector provides a unipolar output for each positive or negative zero-crossing of the Differentiator output. To enhance signal peak detection, the Time Domain Filter inhibits the detection of zero-crossings if they are not sufficiently separated in time. The filter period is set by an external RC network connected to the TD pin.

The Time Domain Filter drives the output One-Shot which generates uniform output data pulses. The pulse width is set by an external RC network connected to the PW pin. The Output One-Shot is inhibited while in the Write Mode.

ABSOLUTE MAXIMUM RATINGS

5V Supply Voltage, V_{CC} 7V
12V Supply Voltage, V_{DD} 14V
Storage Temperature . . . . . −65 °C to +130 °C
Ambient Operating Temperature . . . . . 0 °C to +70 °C
Junction Operating Temperature . . . . . 0 °C to +130 °C
Logic Input Voltage . . . . . $-0.5V_{dc}$ to $7.0V_{dc}$
Lead Temperature (soldering, 10 sec) . . . . . 260 °C
Power Dissipation 800mW

ELECTRICAL CHARACTERISTICS Unless otherwise specified, 4.75V ≤V_{CC} ≤5.25V; 11.4V ≤V_{DD} ≤12.6V; 0 °C ≤T_A ≤70 °C; R_W = 430Ω; R_{ED} = 62kΩ; C_E = 0.012μF; R_{EH} = 62kΩ; R_{EC} = 220Ω

POWER SUPPLY

Characteristic	Test Conditions	Min.	Max.	Units
POWER SUPPLY CURRENTS				
I_{CC} — 5V Supply Current	Read Mode	—	35	mA
	Write Mode	—	38	mA
I_{DD} — 12V Supply Current	Read Mode	—	26	mA
	Write Mode (excluding Write & Erase currents)	—	24	mA

Characteristic	Test Conditions	Min.	Max.	Units
LOGIC SIGNALS — READ/$\overline{\text{WRITE}}$ (R/$\overline{\text{W}}$), CURRENT BOOST (CB)				
Input Low Voltage (V_{IL})		—	0.8	V
Input Low Current (I_{IL})	V_{IL} = 0.4V	—	−0.4	mA
Input High Voltage (V_{IH})		2.0	—	V
Input High Current (I_{IH})	V_{IH} = 2.4V	—	20	μA
LOGIC SIGNALS — WRITE DATA INPUT (WDI), HEAD SELECT (HS0/$\overline{\text{HS1}}$)				
Threshold Voltage, V_T + Positive — going		1.4	1.9	V
Threshold Voltage, V_T − Negative — going		0.6	1.1	V
Hysteresis, V_T+ to V_T−		0.4	—	V
Input High Current, I_{IH}	V_{IH} = 2.4V	—	20	μA
Input Low Current, I_{IL}	V_{IL} = 0.4V	—	−0.4	mA
CENTER TAP VOLTAGE REFERENCE				
Output Voltage (V_{CT})	I_{WC} + I_E = 3mA to 60mA	V_{DD} − 1.5	V_{DD} − .5	V
V_{CC} Turn-Off Threshold	(See Note 1)	4.0	—	V
V_{DD} Turn-Off Threshold	(See Note 1)	9.6	—	V
V_{CT} Disabled Voltage		—	1.0	V
ERASE OUTPUTS (E1, E0)				
Unselected Head Leakage	V_{E0}, V_{E1} = 12.6V	—	100	μA
Output on Voltage (V_{E1}, V_{E0})	I_E = 50mA	—	0.5	V
WRITE CURRENT				
Unselected Head Leakage	V_{E1}, V_{E0} = 12.6V	—	25	μA
Write Current Range	R_W = 820Ω to 180Ω	3	10	mA
Current Reference Accuracy	I_{WC} = 2.3/R_W V_{CB} (current boost) = 0.5V	−5	+5	%
Write Current Unbalance	I_{WC} = 3mA to 10mA	—	1.0	%
Differential Head Voltage Swing	ΔI_{WC} ≤ 5%	12.8	—	Vpk
Current Boost	V_{CB} = 2.4V	1.25 I_{WC}	1.35 I_{WC}	—

Characteristic	Test Conditions	Min.	Max.	Units
ERASE TIMING				
Erase Delay Range	R_{ED} = 39kΩ to 82kΩ ; C_E = 0.0015μF to 0.043μF	0.1	1.0	msec
Erase Delay Accuracy $\frac{\Delta T_{ED}}{T_{ED}}$ x 100%	T_{ED} = 0.69 R_{ED} C_E R_{ED} = 39kΩ to 82kΩ; C_E = 0.0015μF to 0.043μF	−15	+15	%
Erase Hold Range	R_{EH} + R_{ED} = 78kΩ to 164kΩ; C_E = 0.0015μF to 0.043μF	0.2	2.0	msec
Erase Hold Accuracy $\frac{\Delta T_{EH}}{T_{EH}}$ x 100%	T_{EH} = 0.69 (R_{EH} + R_{ED}) C_E R_{EH} + R_{ED} = 78kΩ to 164kΩ ; C_E = 0.0015μF to 0.043μF	−15	+15	%

ELECTRICAL CHARACTERISTICS

READ MODE

Unless otherwise specified: V_{IN} (Preamplifier) = 10mVp-p sine wave, dc coupled to center tap. (See Figure 1). Summing Amplifier Load = 2kΩ line-line, ac coupled. V_{IN} (Postamplifier) = 0.2Vp-p sine wave, ac coupled; R_G = open; Data Pulse Load = 1kΩ to Vcc; C_D = 240pF; C_{TD} = 100pF; R_{TD} = 7.5kΩ ; C_{PW} = 47 pF; R_{PW} = 7.5kΩ .

Characteristic	Test Conditions	Min.	Max.	Units
PREAMPLIFIER — SUMMING AMPLIFIER				
Differential Voltage Gain	Freq. = 250kHz	85	115	V/V
Bandwidth (−3 dB)		3	—	MHz
Gain Flatness	Freq. = dc to 1.5MHz	—	±1.0	dB
Differential Input Impedance	Freq. = 250kHz	20	—	kΩ
Max. Differential Output Voltage Swing	V_{IN} = 250kHz sine wave, THD ≤ 5%	2.5	—	Vp-p
Small Signal Differential Output Resistance	I_O ≤ 1.0mAp-p	—	75	Ω
Common Mode Rejection Ratio	V_{IN} = 300mVp-p @ 500kHz. Inputs shorted.	50	—	dB
Power Supply Rejection Ratio	ΔV_{DD} = 300mVp-p @ 500kHz Inputs shorted to V_{CT}.	50	—	dB
Channel Isolation	Unselected Channel V_{IN} = 100mVp-p @ 500kHz. Selected channel input connected to V_{CT}.	40	—	dB
Equivalent Input Noise	Power BW = 10kHz to 1MHz Inputs shorted to V_{CT}.	—	10	μVrms
Center Tap Voltage, V_{CT}			1.5 (typ)	V
POSTAMPLIFIER — ACTIVE DIFFERENTIATOR				
Ao, Differential Voltage Gain +IN, −IN to D1, D2	Freq. = 250kHz (See Figure 2)	8.5	11.5	V/V
Bandwidth (−3 dB) +IN, −IN to D1, D2	C_D = 0.1μF, R_D = 2.5kΩ	3	—	MHz
Gain Flatness +IN, −IN to D1, D2	Freq. = dc to 1.5 MHz C_D = 0.1μF, R_D = 2.5kΩ	—	±1.0	dB

Characteristic	Test Conditions	Min.	Max.	Units
POSTAMPLIFIER — ACTIVE DIFFERENTIATOR (cont'd)				
Max. Differential Output Voltage Swing	V_{IN} = 250kHz sine wave, ac coupled. ≤5% THD in voltage across C_D. (See Figure 2)	5.0	—	Vp-p
Max. Differential Input Voltage	V_{IN} = 250kHz sine wave, ac coupled. ≤5% THD in voltage across C_D. R_G = 1.5kΩ	2.5	—	Vp-p
Differential Input Impedance		10	—	kΩ
Gain Control Accuracy $\frac{\Delta A_R}{A_R} \times 100\%$	$A_R = A_O R_G/(8 \times 10^3 + R_G)$ R_G = 2kΩ	−25	+25	%
Threshold Differential Input Voltage. (See Note 2)	Min. differential input voltage at post amp that results in a change of state at RDP. V_{IN} = 250kHz square wave, C_D = 0.1μF, R_D = 500Ω, T_R, T_F ≤0.2μsec. No overshoot; Data Pulse from each V_{IN} transition. (See Figure 3)	—	3.7	mVp-p
Peak Differentiator Network Current		1.0	—	mA
TIME DOMAIN FILTER				
Delay Accuracy $\frac{\Delta T_{TD}}{T_{TD}} \times 100\%$	$T_{TD} = 0.58\ R_{TD} \times (C_{TD} + 10^{-11}) + 50$nsec, R_{TD} = 5kΩ to 10kΩ, $C_{TD} \geq$ 56pF V_{IN} = 50m Vpp @ 250kHz square wave, T_R, $T_F \leq$ 20 nsec, ac coupled. Delay measured from 50% input amplitude to 1.5V Data Pulse.	−15	+15	%
Delay Range	$T_{TD} = 0.58\ R_{TD} \times (C_{TD} + 10^{-11}) + 50$ nsec R_{TD} = 5kΩ to 10kΩ C_{TD} = 56pF to 240pF	240	2370	ns
DATA PULSE				
Width Accuracy $\frac{\Delta T_{PW}}{T_{PW}} \times 100\%$	$T_{PW} = 0.58\ R_{PW} \times (C_{PW} + 8 \times 10^{-12}) + 20$ nsec R_{PW} = 5kΩ to 10kΩ $C_{PW} \geq$ 36pF width measured at 1.5V amplitudes	−20	+20	%
Active Level Output Voltage	I_{OH} = 400μA	2.7		V
Inactive Level Output Leakage	I_{OL} = 4mA	—	0.5	V
Pulse Width	$T_{PW} = 0.58\ R_{PW} \times (C_{PW} + 8 \times 10^{-12}) + 20$ nsec R_{PW} = 5kΩ to 10kΩ C_{PW} = 36pF to 200 pF	145	1225	nS

NOTES:
1 Voltage below which center tap voltage reference is disabled
2 Threshold Differential Input Voltage can be related to peak shift by the following formula

$$\text{Peak Shift} = \frac{3.7\text{mV}}{\pi V_{in}} \times 100\%$$

where V_{in} = peak to peak input voltage at post amplifier
Note that this formula demonstrates an inverse relationship between the input amplitude and the Peak Shift

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TEST SCHEMATICS:

FIGURE 1
Preamplifier Characteristics

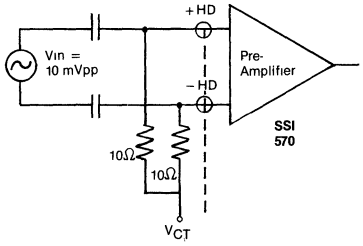


FIGURE 2
Postamplifier
Differential Output Voltage Swing and Voltage Gain

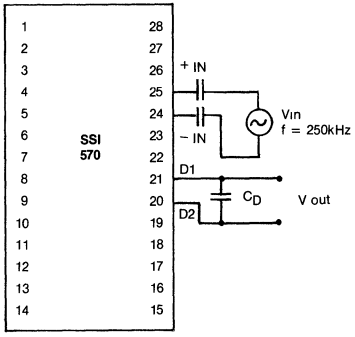


FIGURE 3
Postamplifier
Threshold Differential Input Voltage

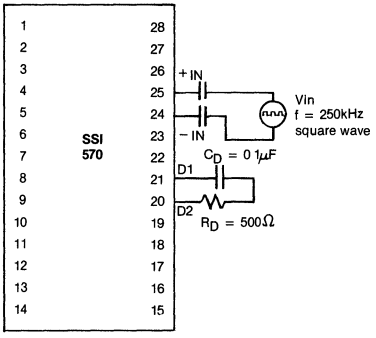
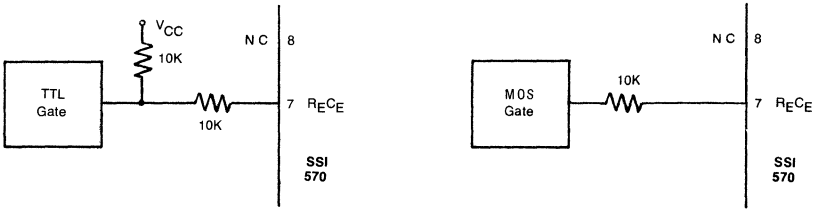


FIGURE 4
External Erase
Control Connections



Output HI = Erase Coil Active

SSI FLOPPY DISK CIRCUITS		
SSI 570	2-Channel	Floppy Read/Write Circuit
SSI 575	4-Channel	Floppy Read/Write Circuit
SSI 580	—	Floppy Support Circuit

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SSI 575
2 or 4-Channel Floppy Disk Read/Write Circuit

Preliminary Data Sheet

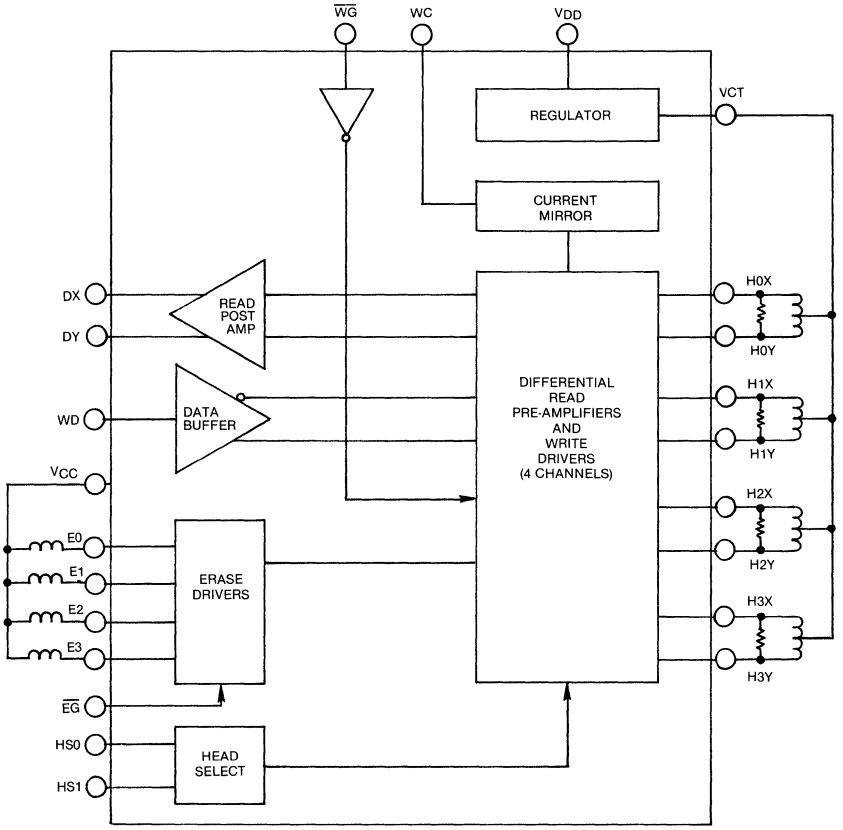
GENERAL

The SSI 575 device is a bipolar monolithic integrated circuit used in floppy disk systems for head control and write, erase, and read select functions. The device has either two or four discrete read, write, and erase channels. Channel select inputs are TTL compatible. The SSI 575 device requires +5V and +12 V power supplies and is available in 18-pin (2-channel version) or 24-pin (4-channel version) dual inline packages.

FEATURES

- **Operates on +5V, +12V power supplies**
- **Two or four channel capability**
- **TTL compatible control inputs**
- **Read/Write functions on one chip**
- **Internal center tap voltage source**
- **Supports all disk sizes**
- **Applicable to tape systems**

SSI 575 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

SSI 575
2 or 4-Channel Floppy Disk Read/Write Circuit

CIRCUIT OPERATION
The SSI 575 functions as a write and erase driver or as a read amplifier for the selected head. Two TTL compatible inputs are decoded to select the desired read/write and erase heads. Head select logic is indicated in Table 2. Both the erase gate ($\overline{EG}$) and write gate ($\overline{WG}$) lines have internal pull up resistors to prevent an accidental write or erase condition.

MODE SELECTION
The read or write mode is determined by the write gate ($\overline{WG}$) line. The input is open collector TTL compatible. With the input low, the circuit is in the write mode. With the input high (open), the circuit is in the read mode. In the read mode, or with the +5V supply off the circuit will not pass write current.

ERASE
The erase operation is controlled by an open collector TTL compatible input. With erase gate ($\overline{EG}$) input high (open) or the +5V supply off, the circuit will not pass erase current. With $\overline{EG}$ low, the selected open collector erase output will be low and current will be pulled through the erase heads.

READ MODE
With the $\overline{WG}$ line high, the read mode is enabled. In the read mode the circuit functions as a differential amplifier. The state of the head select input determines which amplifier is active. When the mode or head is switched, the read output will have a voltage level shift. External reactive elements must be allowed to recover before proper reading can commence. A current diverting circuit prevents any possible write current from appearing on a head line.

WRITE MODE
With the $\overline{WG}$ line low, externally generated write current is mirrored to the selected head and is switched between head windings by the state of the write data (WD) signal.

TABLE 1: PIN DESCRIPTION

Pin Name	Description
V_{CC}	+5V.
V_{DD}	+12V
H0X-H3X H0Y-H3X	X, Y head connections
DX, DY	X, Y Read Data: Differential read signal out
$\overline{WG}$	Write gate: sets write mode of operation
WC	Write current: current mirror used to drive floppy disk heads
WD	Write data line
$\overline{EG}$	Erase gate: allows erasure by selected head
E0-E3	Erase head driver connections
HS0-HS1	Head select inputs
GND	Ground
VCT	Center Tap Voltage Source

TABLE 2: HEAD SELECT LOGIC
4 CHANNELS

HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

2 CHANNELS

HS1	HEAD
0	0
1	1

ABSOLUTE MAXIMUM RATINGS*
DC Supply Voltage: Vcc ..... 6.0 V
Vdd ..... 14.0 V
Write Current ..... 10 mA
Head Port Voltage ..... 18.0 V
Digital Input Voltages:
$\overline{DX}$, $\overline{DY}$, HS0, HS1, WD ..... −0.3 to +10 V
$\overline{EG}$, $\overline{WG}$ ..... −0.3 to Vcc +0.3 V
DX, DY Output Current ..... −5 mA
VCT Output Current ..... −10 mA
Storage Temperature Range ..... −65 to +150 °C
Junction Temperature ..... 125 °C
Lead Temperature (10 sec solder) ..... 260 °C

*Operation above these ratings may cause permanent damage to the device

RECOMMENDED OPERATING CONDITIONS 0°C<Ta<50°C, 4.7V<Vcc<5.3V, 11V<Vdd<13V

Parameter	Conditions	Min.	Typ.	Max.	Unit
Vcc Supply Current:	Vcc MAX	—	—	—	—
Read mode		—	—	15	mA
Write mode		—	—	35	mA
Vdd Supply Current:	Vdd MAX	—	—	—	—
Read mode		—	—	25	mA
Write mode		—	—	15	mA
Write Current		—	5.5	—	mA

ERASE OUTPUT

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Erase on Voltage	IE = 80mA	0.7	—	1.3	VDC
Erase off Leakage		—	—	100	μA

LOGIC SIGNALS — HEAD SELECT (HS0, HS1) AND WRITE DATA (WD)

Low Level Voltage	—	−0.3	—	0.8	VDC
High Level Voltage	—	2.0	—	6.0	VDC
Low Level Current	V_{IN} = 0 volts	−1.6	—	—	mA
High Level Current	V_{IN} = 2.7 volts	—	—	40	μA

LOGIC SIGNALS — $\overline{\text{WRITE GATE}}$ ($\overline{\text{WG}}$) AND $\overline{\text{ERASE GATE}}$ ($\overline{\text{EG}}$)

Low Level Voltage	—	−0.3	—	0.81	VDC
High Level Input Current	—	−300	—	—	μA
Low Level Current	V_{IN} = 0 volts	−2.0	—	—	mA

READ MODE

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Differential Gain	f = 100kHz, Vin = 5 mV Rms R_L = 10 kΩ	80	100	120	V/V
Bandwidth	Vin = 5 m V Rms RL = 10 K CL = 15PF	9	—	—	MHz
Input Voltage Range for 95% Linearity	f = 100kHz, RL = 10k	25	—	—	mVpp
Differential Input Resistance	f = 1 MHz	100	—	—	kΩ
Differential Input Capacitance	f = 1 MHz	—	—	10	pF
Input Bias Current	—	—	—	25	μA
Input Offset Voltage	—	—	—	12	mV
Output Voltage, Common Mode	—	—	8	—	VDC
Output Resistance	—	—	—	35	Ω
Output Current Sink	—	2	—	—	mA
Output Current Source	—	3	—	—	mA
Common Mode Rejection Ratio	f = 1 MHz (input referred)	50	—	—	dB
Power Supply Rejection Ratio	f = 1 MHz (input referred)	50	—	—	dB
Channel Separation	f = 1 MHz (input referred)	50	—	—	dB
Input Noise	BW = 100 Hz to 1 MHz, Z Source = 0	—	7	—	μV RMS

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WRITE MODE

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Write Current Gain	IW = 5.5mA	.97	—	1.05	A/A
Write Current Voltage Level	IW = 5.5mA	1.2	—	2.1	VDC
Differential Head Voltage	IW = 5.5mA	12.5	—	—	VDC
Unselected Head Current	IW = 5.5mA DC Condition	—	—	0.1	mA
Write Current Unbalance	IW = 5.5mA	—	—	1	%
Write Current Time Symmetry	IW = 5.5mA	—	—	± 10	nS
Read Amplifier Output Level	—	—	10.5	—	VDC
Center Tap Voltage (Read and Write Modes)	—	—	8.5	—	VDC

SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Write and Erase Gate Switching Delay	Delay to 90% of Write Current	—	—	1	μsec
Head Select Switching Delay	—	—	—	1	μsec
Head Current Switching Delay	T1 in Fig. 1	—	10	—	nsec
Head Current Switching Time	IW = 5.5mA Shorted Head	—	10	30	nsec
Write to Read Recovery Time	—	—	—	2	μsec

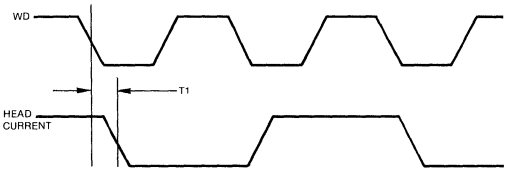
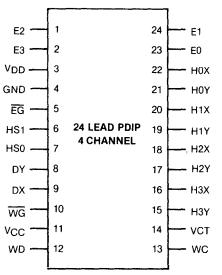
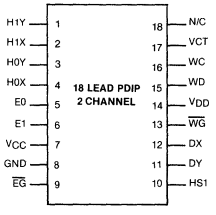


FIG 1

PIN CONFIGURATIONS



Top View
Pinout



Top View
Pinout

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SSI 580
Port Expander
Floppy Disk Drive

Preliminary Data Sheet

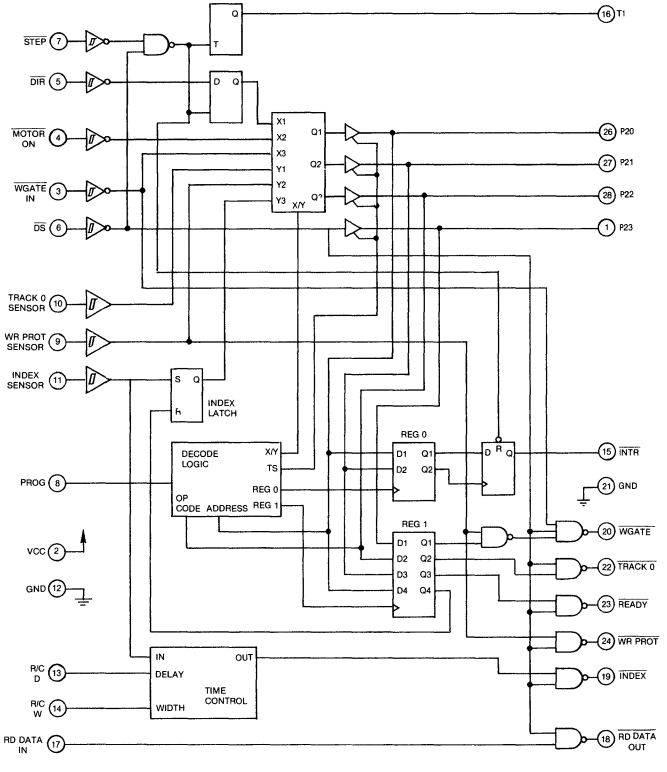
DESCRIPTION

The SSi 580 device is a bipolar integrated circuit that serves as an input/output port expander for an 8048 type microprocessor based floppy disk drive system. The device consolidates functions normally performed by a variety of LSTTL, SSI, and MSI devices. The combination of an SSI 570 (read, write, and erase device), an 8048 type microprocessor, and the SSI 580 provides the majority of electronics required for a SA400 type floppy disk drive system, including host interface bus driver and receiver. In addition to its port expansion function, the SSI 580 processes system data and provides both pulse width and delay control (adjustable by external elements) for the INDEX SENSOR input. The device requires a single +5 V power supply and is available in a 28-pin package.

FEATURES

- **Reduces package count in flexible disk drive systems**
- **Replaces bus interface and combinational logic devices between the SSI 570, on board microprocessor and mechanical interfaces.**
- **Surface mount available for further real estate reduction.**
- **Provides drive capability for mechanical and system interfaces**

SSI 580 Block Diagram



CAUTION: Use handling procedures necessary for a static sensitive component

PIN ASSIGNMENT DESCRIPTIONS

Pin Name	Description
P20-P23	4-bit bidirectional port, referred to as Port 2.
$\overline{\text{WGATE IN}}$	This input command to write is asserted by the host interface bus.
$\overline{\text{MOTOR ON}}$	This input command to turn on the spindle motor comes from the host interface bus.
$\overline{\text{DIR}}$	Input from the host interface bus selecting the direction in which the stepper motor should move the head.
$\overline{\text{DS}}$	Drive select
INDEX SENSOR	Input from the photodiode that indicates the index marker in the diskette.
WR PROT SENSOR	Input from the photodiode that indicates if the diskette is write protected.
TRACK 0 SENSOR	Input from the photodiode that detects when the head is positioned over track 0.
$\overline{\text{STEP}}$	Input from the host interface bus indicating that the head should be moved.
T1	This pin changes state when a $\overline{\text{STEP}}$ command is received from the host interface bus.
RD DATA IN and $\overline{\text{RD}}$ $\overline{\text{DATA OUT}}$	Read data path
$\overline{\text{WGATE}}$	Output to the disk drive's read/write circuitry.
$\overline{\text{INDEX}}$	Output to the host interface bus indicating index sensor status.
$\overline{\text{TRACK 0}}$	Output to the host interface bus indicating track 0 sensor status.
$\overline{\text{READY}}$	Output to the host interface bus indicating track 0 sensor status.
$\overline{\text{WR PROT}}$	Output to the host interface bus indicating write protect sensor status.
PROG	Input from the 8048 microprocessor for I/O control of the 580.
$\overline{\text{INTR}}$	Output to the interrupt pin of the 8048 microprocessor.
R/C D and R/C W	The external resistor and capacitor networks tied to these pins determines the delay and width of the output pulse to the $\overline{\text{INDEX}}$ pin.
Vcc	+5 V supply
GND	Ground

Table 1

CIRCUIT OPERATION

PORTS

The SSI 580 has two 4-bit input ports, Port A and Port B. Port a receives data from the host interface bus for conveyance to the drive's read/write circuitry and to the microprocessor. Three sensors report the status of the drive to the 580 via Port B. Common to both ports is a drive select ($\overline{\text{DS}}$) signal from the host interface bus. This allows the host to address separate disk drives. There is also a 4-bit bidirectional port on the SSI 580. This is port 2 and it can be used by the microprocessor to write to or read from the 580.

READ MODE

Ports A and B can be read by a microprocessor via Port 2. This allows the microprocessor to obtain data from the host interface bus and the status sensors. The PROG signal from the microprocessor provides the timing for the operation. First an OP code and a port address must be placed on Port 2 (see Table 2), then latched in on the falling edge of PROG. When the OP code and addresses have been decoded, the desired input port is selected and output on Port 2. The operation is terminated by the rising edge PROG, which returns Port 2 to the input mode.

WRITE MODE

In the write mode the microprocessor passes system parameters to the SSI 580 for logic processing and outputting. Table 3 shows how each bit of Port 2 affects the 580. A logic one on the zero bit of Port 2 will reset the index latch. P21, qualified by the $\overline{\text{DS}}$ signal, sends a "this drive ready" signal from the microprocessor to the host interface bus. Similarly P22 is $\overline{\text{DS}}$ qualified and sent to the host as a signal that the head is positioned over track 0. P23 is used in the logic that sends a R/$\overline{\text{W}}$ signal to the drive's read/write circuitry. The write mode occurs when the proper OP code and address is placed on Port 2 and latched in on the falling edge of PROG (see Table 3). The microprocessor writes in the data on PROG's rising edge.

INDEX PULSE

An optical sensor connected to the INDEX SENSOR pin detects the diskette's index marker. The state of the index sensor is latched into the 580 and is available to be read by the microprocessor on P22. The latch may be reset by writing a one to P20 from the microprocessor. The pulse received from the sensor also drives the host interface signal $\overline{\text{INDEX}}$, the width and delay of which can be controlled by external R/C circuits. The time constant attached to the R/C D pin determines the delay from the INDEX SENSOR input to the $\overline{\text{INDEX}}$ signal on the host interface bus. The equation for the delay is Td = 0.59Rd x Cd (seconds). The width of the $\overline{\text{INDEX}}$ signal is determined by the circuit attached to the R/C W pin and the equation Tw = 0.59Rw x Cw (seconds).

INTERRUPT

The $\overline{\text{INTR}}$ signal is asserted every time a step command is issued to the drive on the host interface bus. Thus when $\overline{\text{INTR}}$ is tied to the interrupt pin of 8048 type

microprocessor, an interrupt service routine will be executed on each step command. This routine typically obtains information on the direction the heads should move and the status of the track 0 sensor to use for generating the stepper motor control signals. The interrupt signal is cleared (set high) by first placing the proper OP code and address on Port 2 (see Table 3). This is latched in on the falling edge of PROG, then on its rising edge logic ones on P20 and P21 will be latched in to set $\overline{INTR}$ back to a high state. Note that an indeterminate operation will result from holding the INDEX SENSOR latch reset (holding P20 high).

T1 PIN

This signal changes state with the $\overline{STEP}$ command of the host interface bus when the drive is selected. It drives the T1 pin on an 8048 type microprocessor which is an input to a counter. The 8048 can use this count and the DIR signal read from Port 2 of the SSI 580 to monitor the head position and issue a CB (current boost) command to the SSI 570 when a specific track is reached.

TABLE 2. READ MODE

Input to Port 2		Read From Port 2				4-Bit Input Port
OP Code P22	Addr. P20	P23	P22	P21	P20	
0	0	$\overline{DS}$	Index Sensor Latch	WR Sensor	Track 0 Sensor	B
0	1	$\overline{DS}$	$\overline{WGATE}$ IN	$\overline{MOTOR}$ ON	$\overline{DIR}$	A

TABLE 3. WRITE MODE

Input to Port 2		Data processed from Port 2				
OP Code P22	Addr. P20	$\overline{WGATE}$	$\overline{TRACK0}$	$\overline{READY}$	$\overline{INTR}$	Index Latch Reset
1	0	Z	(P22*DS)	(P21*DS)	—	P20
1	1	—	—	—	See Text	—

Where Z = (P23 * WR PROT SENSOR) + ($\overline{DS}$ * $\overline{WGATE}$ IN)

Absolute Maximum Ratings (All voltages referred to GND)

Parameter	Symbol	Value	Units
DC Supply	Vcc	+7	VDC
Voltage Range (any pin to GND)	V_m	−0.4 to +7	VDC
Power Dissipation	P_{max}	700	mW
Storage Temperature	Tstg	−40 to +125	°C
Lead Temperature (10 sec soldering)	—	260	°C

ELECTRICAL CHARACTERISTICS Unless otherwise specified, 4.75 ≤ Vcc ≤ 5.25 VDC; 0 °C < Ta < 70 °C.

Parameter	Test Conditions	Min.	Max.	Units
Totem pole outputs (P20 – P23, $\overline{INTR}$, T1)				
Output High Voltage	104 = −400 A	2.5	—	V
Output Low Voltage	IoL = 2mA	—	0.5	V
Open collector outputs ($\overline{RD\ DATA\ OUT}$, $\overline{INDEX}$, $\overline{WGATE}$, $\overline{TRACK\ 0}$, $\overline{READY}$, $\overline{WR\ PROT}$)				
Output High Current	VOH = 5.25 V.	—	250	μA
Output Low Voltage	IoL = 48 mA	—	0.5 V	V
Inputs (P20 – P23, PROG, RD DATA IN)				
Input High Voltage	—	2.0	—	V
Input Low Voltage	—	—	0.8	V
Input Low Current	VIL = 0.5 V	—	−0.8	mA
Input High Current	VIL = 2.4 V	—	40	μA
Input Current	Vin = 7.0 V	—	0.1	mA
Schmitt - Trigger Inputs ($\overline{WGATE\ IN}$, $\overline{MOTOR\ ON}$, $\overline{DIR}$, $\overline{DS}$, $\overline{STEP}$)				
Threshold Voltage	Positive Going, Vcc = 5.0 V	1.3	2.0	V
	Negative Going, Vcc = 5.0 V	0.6	1.1	V

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Test Conditions	Min.	Max.	Units
Hysteresis	Vcc = 5.0 V	0.4	—	V
Input High Current	VIH = 2.4 V	—	40	μA
Input Low Current	VIL = 0.5 V	—	−0.4	mA
Input Current	VIN = 7.0 V	—	0.1	mA
HIgh Impedance Inputs with Hysteresis (WR PROT SENSOR, TRACK 0 SENSOR, INDEX SENSOR)				
Input High Voltage	—	—	2.0	V
Input Low Voltage	—	0.8	—	V
Hysteresis	—	0.2	—	V
Input Current	Vin = 0 to Vcc	—	−0.25	mA

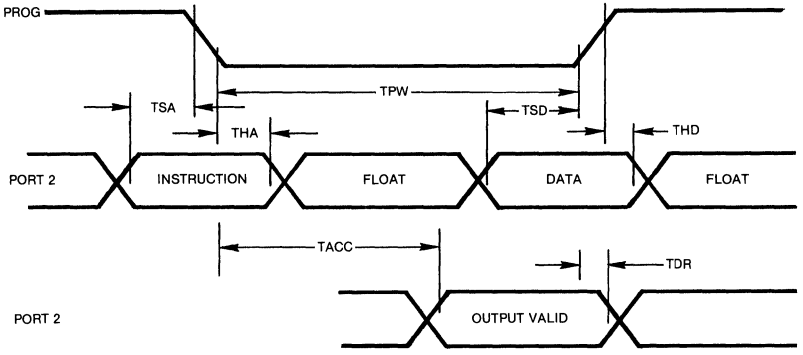
TIMING CHARACTERISTICS Unless otherwise specified; Ta = 25°C; 4.75 V ≤ Vcc ≤ 5.25 V; CL = 15 pf.

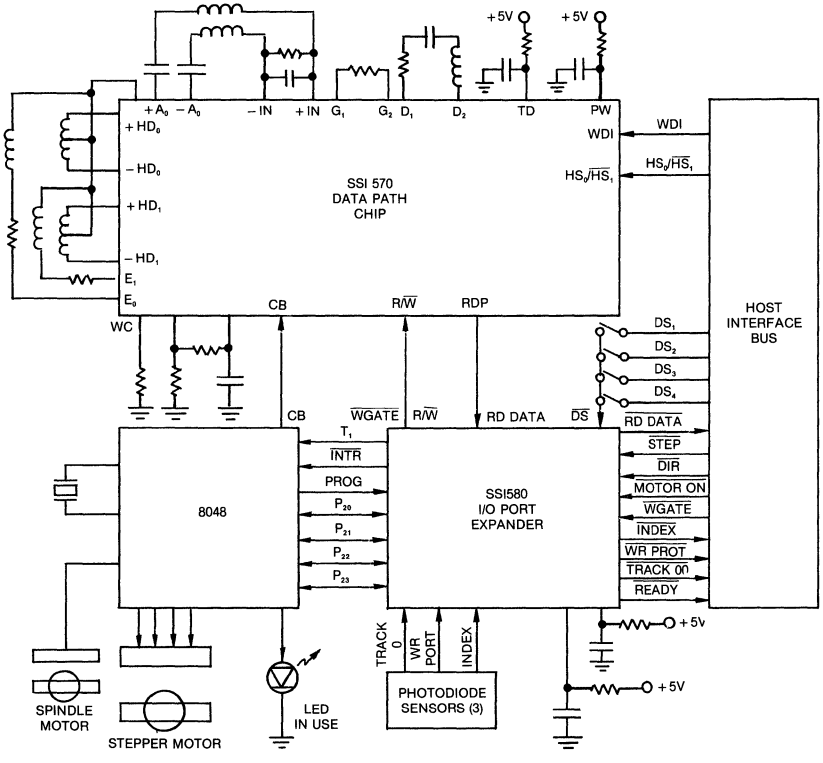
PARAMETER	CONDITION	MIN.	MAX.	UNITS
Propagation Delay Time	RD DATA IN to $\overline{\text{RD DATA OUT}}$	—	35	nS
	$\overline{\text{DS}}$ to $\overline{\text{WGATE}}$, $\overline{\text{TRACK 0}}$, $\overline{\text{READY}}$, $\overline{\text{WR PROT}}$, $\overline{\text{RD DATA}}$, $\overline{\text{INDEX}}$	—	80	nS
	PROG to $\overline{\text{INTR}}$, $\overline{\text{WGATE}}$, $\overline{\text{TRACK 0}}$ (Rising edge) $\overline{\text{READY}}$, $\overline{\text{WR PROT}}$	—	100	nS
	WR PROT to $\overline{\text{WGATE}}$, $\overline{\text{WR PROT SENSOR}}$	—	250	nS
	$\overline{\text{WGATE IN}}$ to $\overline{\text{WGATE}}$	—	80	nS
	$\overline{\text{STEP}}$ to T1, P20	—	80	nS
	TRACK 0 SENSOR WR PROT SENSOR to Port 2 INDEX SENSOR	—	250	nS
	$\overline{\text{MOTOR ON}}$ $\overline{\text{WGATE IN}}$ to Port 2 $\overline{\text{DS}}$	—	80	nS
Data Setup Time	$\overline{\text{DIR}}$ to $\overline{\text{STEP}}$	50	—	nS
Data Hold Time	$\overline{\text{DIR}}$ to $\overline{\text{STEP}}$	0	—	nS
Delay Accuracy (Pin 13)	$T_D = 0.59\ R_D \times C_D$ R_D = 3.9k to 10k C_D = 75pf to 300pf	0.8Td	1.2Td	sec
Pulse Width Accuracy (Pin 14)	$T_W = 0.59\ R_W \times C_W$ R_W = 3.9k to 10k C_W = 75pf to 300pf	0.8Tw	1.2Tw	sec

PORT 2 (P20 – P23) TIMING (Timing Referenced to PROG signal, Figure 2.)

Symbol	Name-Description	Min	Max	Units
TSA	Addr. setup time	100	—	nS
THA	Addr. hold time	80	—	nS
TSD	Data in setup time	100	—	nS
THD	Data-in hold time	80	—	nS
TACC	Data-out access time	—	700	nS
TDR	Data-out release time	—	200	nS
TPW	PROG pulse width	1500	—	nS

Figure 2. Timing Diagram





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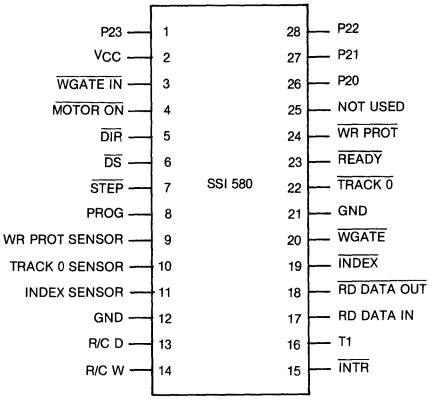
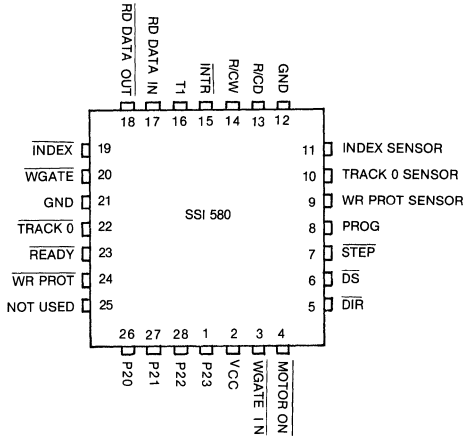
PIN CONFIGURATION



28-LEAD PDIP
(Top View)



28-Lead Quad
(Top View)

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INNOVATORS IN INTEGRATION

SSI 550
4-Channel Magnetic Tape Read Circuit

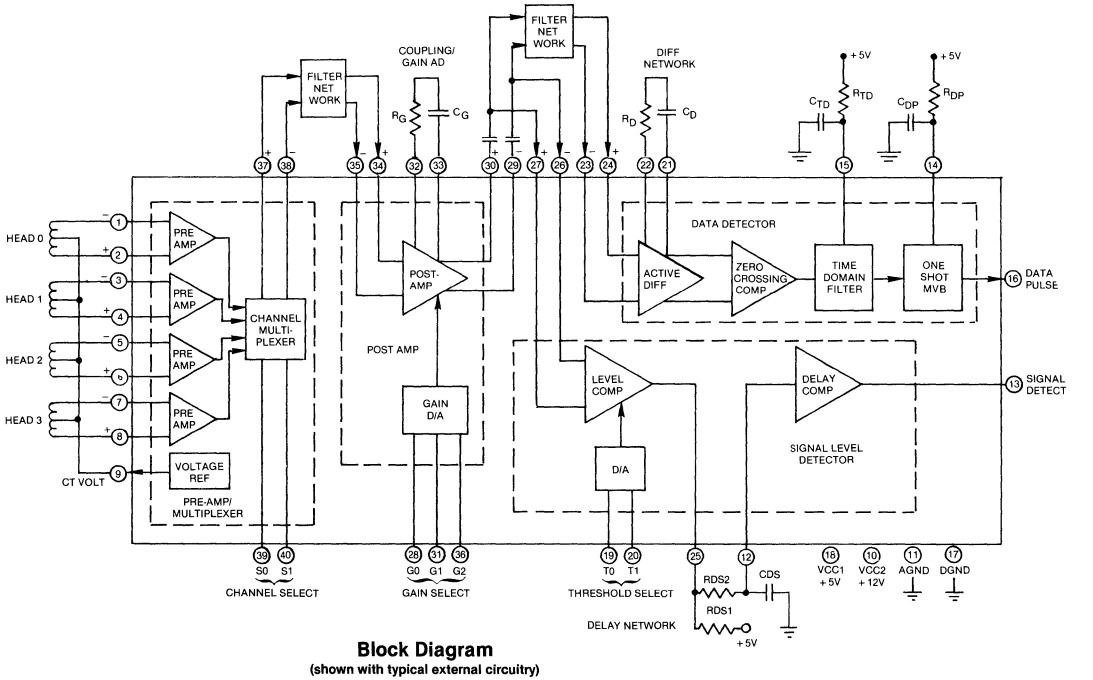
Preliminary Data Sheet

GENERAL DESCRIPTION

Silicon Systems' SSI 550 combines magnetic tape head read signal amplification and processing onto a single integrated circuit. The device accepts up to 4 center-tapped magnetic read heads connected directly to the head inputs; head center tap voltage is provided by an on-chip reference. The device architecture permits system design flexibility by providing the external connections between the Preamplifier/Multiplexer, Postamplifier, Signal Level Detector, and Data Detector; this allows the implementation of many suitable filtering combinations. Low noise amplifiers are used throughout the device. The SSI 550 operates on +5 and +12 Volt supplies and has TTL compatible control signals.

FEATURES

- **4-Channel Multiplexer with differential-input Preamplifiers**
- **Postamplifier has component-adjustable and programmable gain**
- **On-chip Signal Level Detector with programmable threshold and adjustable delay**
- **Data Detection Circuit includes spurious signal rejection (adjustable time domain filter) and provides an adjustable uniform Data Pulse output**
- **Available in 40 pin DIP or 44 pin Quad plastic packages**



Block Diagram
(shown with typical external circuitry)

CAUTION: Use handling procedures necessary for a Static Sensitive Component.

SSI 550
4-Channel Magnetic Tape Read Circuit

DEVICE DESCRIPTION AND OPERATION

4-Channel Preamplifier and Multiplexer

The device contains four low level differential-input Preamplifiers. The differential output of a single Preamplifier is selectively connected to the Preamplifier output terminals by means of two logical CHANNEL SELECT signals, S0 and S1. The selected Preamplifier number is the binary value of the logical SELECT signals for active high voltage levels.

The Preamplifier inputs are intended for connection to center-tapped magnetic read heads. An appropriate Preamplifier input bias voltage level is obtained by connecting the head center taps to the circuit C.T. VOLT terminal.

The C.T. VOLT terminal is the output of a voltage reference which has a value to center the Preamplifier inputs within their operating range.

Postamplifier

The Postamplifier is a differential-input, differential-output circuit which has two means of gain adjustment. A continuously-variable gain adjustment is obtained by use of an external resistor or potentiometer. Discrete values of gain setting are additionally obtained by applying combinations of logical signal levels to the three GAIN SELECT terminals, G0, G1, and G2.

The Postamplifier receives the output signals of the Preamplifier after frequency selection by an external filter network. The input characteristics of the Postamplifier are such that the inputs may have DC coupling to the Preamplifier output, or may be AC coupled with proper bias of 3V nom.

A suitable coupling capacitor must be connected between the GAIN1, GAIN2 terminals independent of the use of a gain setting resistor.

Signal Level Detect Circuits

The Signal Level Detect circuits consist of detector circuits which compare the amplitude of the signal envelope of the Postamplifier output with a selectable threshold and provide a logical output level which indicates the presence of Postamplifier signal greater than the threshold. AC coupling is required between the Postamplifier output and the Signal Level Detect circuits input. The Signal Level Detect input has internal bias connections so that no external bias network is required.

The threshold to which the Postamplifier signals are compared is selected by means of two THRESHOLD SELECT logical inputs T0 and T1. The result of the comparison is delayed from appearing at the circuit SIGNAL DETECT output terminal by means of a delay circuit which is adjustable by means of external components.

The delay associated with signal detection is set by combinations of capacitor CDS and resistor RDS1. The delay associated with signal loss is set by combinations of CDS and resistors RDS1 plus RDS2.

Data Detection Circuits

The Data Detection circuits are AC coupled to the Postamplifier outputs through an (optional) external filter network and provide logical output pulse signals in response to positive and negative input signal amplitude peaks. This function is performed by differentiating input signals to obtain zero-crossing voltages at points of inflection and detecting these crossings to provide output signals.

To enhance the signal peak detection, spurious inflection points which occur inpairs between true signal peaks are suppressed by means of the Time Domain Filter. The filter inhibits the propagation of detected zero-crossings if they are not sufficiently separated in time. This time period is set by external capacitor CTD and resistor RTD.

Uniform DATA PULSE output signals are provided by the One-Shot Multivibrator which is triggered by outputs of the Time Domain Filter. The time duration of the DATA PULSE signals is set by external capacitor CDP and RDP.

DC paths through the external filter network to the Signal Level Detect circuits inputs are required to properly bias the Data Detection circuits. The resistance of each path is not critical and may be as large as 10 Kohm.

PIN DESIGNATION

Pin Number		Pin Name	Pin Description
DIP	QUAD		
1	1	IN0 –	Channel 0 (–) input
2	2	IN0 +	(+) input
3	3	IN1 –	Channel 1 (–) input
4	4	IN1 +	(+) input
5	5	IN2 –	Channel 2 (–) input
—	6	N/C	No internal connection
6	7	IN2 +	Channel 2 (+) input
7	8	IN3 –	Channel 3 (–) input
8	9	IN3 +	(+) input
9	10	CT VOLT	Center tap voltage
10	11	VCC2	+ 12 Volt supply connection
11	12	AGND	Analog signal ground
12	13	DEL IN	Input to delay comparator
13	14	SIGNAL DETECT	Output of delay comparator
14	15	DPN	External RC for output pulse width
15	16	TDF	External RC for time-domain delay
—	17	N/C	No internal connection
16	18	DATA PULSE	Output of time-domain filter
17	19	DGND	Ground
18	20	VCC1	+ 5 Volt supply
19	21	T0	Threshold select signal (1 of 2)
20	22	T1	Threshold select signal (1 of 2)
21	23	CAP1	External differentiating capacitor connection
22	24	CAP2	
23	25	DIF –	Inputs to active differentiator
24	26	DIF +	
25	27	LEV OUT	Output to level detector
—	28	N/C	No internal connection
26	29	LEV –	Inputs to level detector
27	30	LEV +	
28	31	G0	Postamp gain select (1 of 3)
29	32	PSTOUT –	Outputs of Postamplifier
30	33	PSTOUT +	
31	34	G1	Postamp gain select (1 of 3)
32	35	GAIN 1	External Postamplifier gain adjusting RC terminals
33	36	GAIN 2	
34	37	PSTIN +	Inputs to Postamplifier
35	38	PSTIN –	
—	39	N/C	No internal connection
36	40	G2	Postamp gain select (1 of 3)
37	41	PREOUT +	(+) Output of Preamplifier
38	42	PREOUT –	(–) Output of Preamplifier
39	43	S0	Input channel select (1 of 2)
40	44	S1	Input channel select (1 of 2)

ABSOLUTE MAXIMUM RATINGS

Characteristic	Rating
Storage Temperature	−65 °C. to +150 °C.
Ambient Operating Temperature, Ta	0 °C. to +70 °C.
Junction Operating Temperature, Tj	0 °C. to +130 °C.
Supply Voltage, Vcc1	−0.5 Vdc to +6.0 Vdc
Supply Voltage, Vcc2	−0.5 Vdc to +14.0 Vdc
Voltage Applied to Logic Inputs	−0.5 Vdc to Vcc1 +0.5 Vdc
Voltage Applied to OFF Logic Outputs	−0.5 Vdc to Vcc1 +0.5 Vdc
Current Into ON Logic Outputs	5.0 mA
Lead Temperature (soldering, 10 sec)	+260 °C.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: Vcc1 = 4.75V to 5.25V, Vcc2 = 11.4V to 12.6V, Ta = 0 to +70 °C.

Overall Characteristics

Characteristics	Test Conditions	Min.	Max.	Units
Input Current Logical Inputs HIGH	Vih = Vcc1	—	100	uA
Input Current Logical Inputs LOW	Vil = 0V	—	−400	uA
Output Voltage Delay Comparator OFF	Ioh = −400uA	2.4	—	V
Output Voltage Delay Comparator ON	Iol = 2.0mA	—	0.5	V
Data Pulse Inactive Level Output Voltage	Ioh = −400uA	2.4	—	V
Data Pulse Active Level Output Voltage	Iol = 2.0mA	—	0.5	V
Vcc1 Power Supply Current	Necessary external components and connections No Head Inputs.	—	30	mA
Vcc2 Power Supply Current	Necessary external components and connections No Head Inputs.	—	62	mA

* Characteristic applies to Inputs S0, S1, G0, G1, G2, T0, T1

PREAMPLIFIER AND MULTIPLEXER CHARACTERISTICS

Output Load = 2KΩ line-line, Channel Select Signals (S0, S1): VON = 2V Min., VOFF = 0.8V Max.

Characteristics	Test Conditions	Min.	Max.	Units
Differential Voltage Gain	Vin = 4mV p-p @ 100kHz ref. to C.T. Volt	80	120	V/V
Gain Flatness	Vin = 4mV p-p DC to 0.5MHz ref. to C.T. Volt	±0.5	—	dB
Bandwidth, −1dB	Vin = 4mV p-p	1.5	—	MHz
Bandwidth, −3dB	Vin = 4mV p-p	3.0	—	MHz
Differential Input Impedance	Vin = 4mV p-p @ 100kHz ref. to C.T. Volt	10	—	KΩ
Common-Mode Rejection Ratio	Vin = 300mV p-p @ 500kHz Inputs Shorted to C.T. Volt	50	—	dB
Power Supply Rejection Ratio	Δ Vcc = 300mV p-p @ 500kHz Inputs shorted to C.T. Volt	50	—	dB
Channel Isolation	Interfering Vin = 100mV p-p @ 2MHz. Selected Channel inputs connected to C.T. Volt	60	—	dB
Total Harmonic Distortion	Vin = 0.5 to 6.0mV p-p @ 500kHz	—	2	%
Equivalent Input Noise	Power BW = 10kHz to 1MHz Inputs shorted to C.T. Volt	—	10	μVrms
Small Sig Single-Ended Output Res.	Io = 1mA p-p @ 100kHz	—	35	Ω
Maximum Diff. Output Voltage	Freq = 100kHz THD < 5%	3	—	Vp-p
Output Offset Voltage	Inputs shorted to C.T. Volt Load = Open Circuit	—	±1.0	V
Common-Mode Output Voltage	Inputs shorted to C.T. Volt Load = Open Circuit	2.68	3.5	V
Center Tap Voltage, C.T. Volt		3.0 Typ		

DATA DETECTION CIRCUIT CHARACTERISTICS

Vin = 1.0V p-p diff. square wave, Tr, Tf< 20nsec, dc-coupled (for biasing). RD = 2.5KΩ; CD = 0.1μF; RTD = 7.8 KΩ; CTD = 200 pF; RDP = 3.9 KΩ; CDP = 100 pF. Data Pulse load = 2.5KΩ to Vcc1 plus 20pF or less to PWR GND.

Characteristics	Test Conditions	Min.	Max.	Units
Differentiator Maximum Differential Input Voltage	Vin = 100kHz sine wave, dc-coupled. < 5% THD in voltage across CD. CD = 620pF RD = 0	5.0	—	Vp-p
Differentiator Input Impedance	Vin = 4V p-p diff., 100kHz sine wave. CD = 620pF RD = 0	10	—	KΩ
Differentiator Threshold Differential Input Voltage	Vin = 100kHz square wave, Tr, Tf< 0.4 usec, no overshoot. Data Pulse from each Vin transition.	—	300	mVp-p
Data Pulse Width Accuracy	TDP = .59 RDP × CDP, RDP = 3.9 KΩ to 10 KΩ, CDP = 75 pF to 300 pF Width measured at 1.5V amplitude	.85TDP	1.15TDP	sec
Time Domain Filter Delay Accuracy	TTD = 0.59 RTD × CTD + 50 nsec, RTD = 3.9KΩ to 10 KΩ, CTD = 100pF to 750pF Delay measured from 50% input amplitude to 1.5V Data Pulse amplitude	.85TTD	1.15TTD	sec
Data Pulse Width Drift from +25°C. value	Width measured from 1.5V amplitude	—	±5.0	%
Time Domain Filter Delay Drift from +25°C. value	Delay measured from 50% Input amplitude to 1.5V Data Pulse amplitude	—	±5.0	%

Note: Differentiating network impedance should be chosen such that 1mA peak current flows at maximum signal level and frequency.

SIGNAL LEVEL DETECT CIRCUITS CHARACTERISTICS

Level Comparator Inputs connected in parallel with Differentiator Inputs. Vin (Level Comp) = 100kHz sine wave, ac-coupled. RDS1 = 5kΩ; RDS2, CDS = open

Characteristics	Test Conditions	Min.	Max.	Units
Level Comparator Input Thresholds, Single-Ended, Each Input	T0 VT0 = 0.8V VT1 = 0.8V Vo pulse value <0.5V at MAX LIMIT, >Vcc1 − 0.5V at MIN LIMIT	30	70	mV pk
	T1 VT0 = 2.0V VT1 = 0.8V Vo pulse value <0.5V at MAX LIMIT, >Vcc1 − 0.5V at MIN LIMIT	97	153	mV pk
	T2 VT0 = 0.8V VT1 = 2.0V Vo pulse value <0.5V at MAX LIMIT, >Vcc1 − 0.5V at MIN LIMIT	138	202	mV pk
	T3 VT0 = 2.0V VT1 = 2.0V Vo pulse value <0.5V at MAX LIMIT, >Vcc1 − 0.5V at MIN LIMIT	210	290	mV pk
Level Comparator Diff. Input Resistance	Vin = 5V p-p @ 100kHz	5	—	KΩ
Level Comparator OFF Output Leakage	Vo = Vcc1	—	25	μA
Level Comparator ON Output Voltage	VT0 = 0.8V VT1 = 0.8V Vin = ±140mV diff. dc Io = 2.0mA	—	0.25	V
Delay Comparator Upper Threshold Voltage	Vo > 2.4V	.65Vcc1	.75Vcc1	V
Delay Comparator Lower Threshold Voltage	Vo< 0.5V	.25Vcc1	.35Vcc1	V
Delay Comparator Input Current	0V< Vin< Vcc1	—	25	μA

POSTAMPLIFIER CHARACTERISTICS

Output Load = 2.5KΩ + 0.1μF line-line, Vin = 100mV p-p, 100kHz sine wave, dc-coupled (to provide proper biasing). CG = 0.1μF RG = 0.

Characteristics	Test Conditions	Min.	Max.	Units
Differential Voltage Gain	A0 VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V A1 VG0 = 2.0V VG1 = 0.8V VG2 = 0.8V A2 VG0 = 0.8V VG1 = 2.0V VG2 = 0.8V A3 VG0 = 2.0V VG1 = 2.0V VG2 = 0.8V A4 VG0 = 0.8V VG1 = 0.8V VG2 = 2.0V A5 VG0 = 2.0V VG1 = 0.8V VG2 = 2.0V A6 VG0 = 0.8V VG1 = 2.0V VG2 = 2.0V A7 VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V ARG VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V when RG = 2.5KΩ	A7-14.75 A7-12.75 A7-10.75 A7-8.75 A7-6.75 A7-4.75 A7-2.75 32 A7-7.5	A7-13.25 A7-11.25 A7-9.25 A7-7.25 A7-5.25 A7-3.25 A7-1.25 — A7-4.5	dB dB dB dB dB dB dB dB dB
Differential Input Impedance	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V	10	—	KΩ
Bandwidth, 1dB	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V	1.5	—	MHz
Bandwidth, 3dB	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V	3.0	—	MHz
Maximum Diff. Output Voltage	VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V Vin = 100kHz sine wave THD <5%	5	—	Vp-p
Small Signal Single-Ended Output Res.	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V Vin = 0V Io = 1mA p-p, 100kHz	—	35	Ω
Input Bias Offset Voltage Range	VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V THD <2.0%	—	±1.0	V
Input Bias Common-Mode Voltage Range	VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V THD <2.0%	2.68	3.5	V

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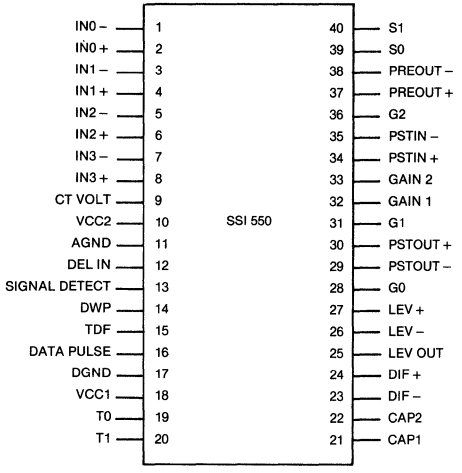
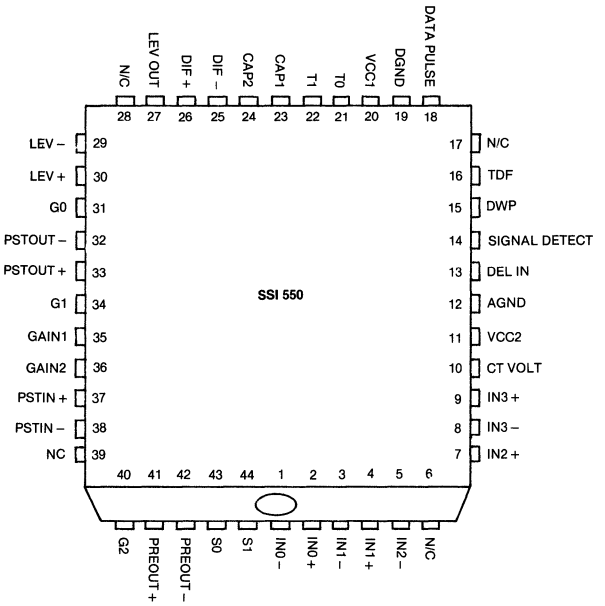


40-PIN DIP
Pin Out (Top View



44-PIN QUAD
Pin Out (Top View)

THERMAL CHARACTERISTICS: θ_{JA}

40-PIN	PDIP	70°C/W
40-PIN	CDIP	45°C/W
44-PIN	QUAD	68°C/W

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INNOVATORS IN INTEGRATION

SSI 67C401/402 First-In First-Out (FIFO) 64x4 or 64x5 Memory

Preliminary Data Sheet

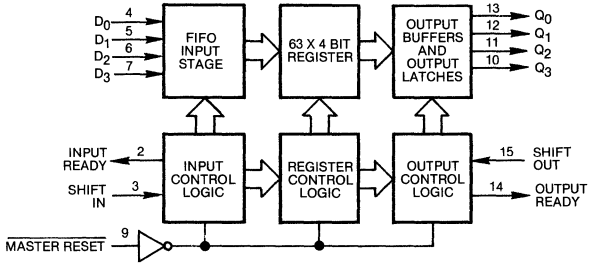
GENERAL DESCRIPTION

The SSI 67C401/402 devices are high speed, expandable memories operating as a First-In, First-Out, (FIFO) asynchronous register of either 64 words by 4-bit (SSI 67C 401) or 64 words by 5-bit (SSI 67C402). The SSI 67C401/402 are CMOS devices. A 10 MHz shift rate provides the fast transfer of data necessary for applications in high speed tape or disc controllers and communication buffers. A single +5V power supply is required.

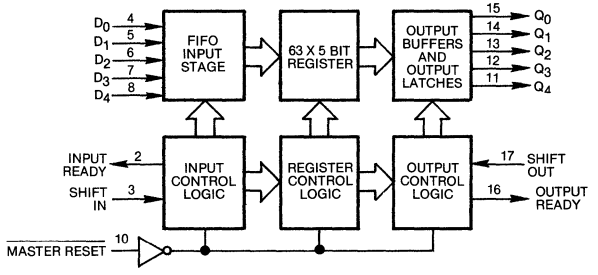
FEATURES

- **10 MHz shift in, shift out rates**
- **Choice of 4-bit or 5-bit width**
- **TTL compatible inputs and outputs**
- **Readily expandable in word and bit dimensions**
- **Output pins directly opposite corresponding input pins**
- **Asynchronous operation**
- **Pin compatible with MMI 67401 Series**
- **Low power consumption**
- **HCT input and output characteristics**

Block Diagrams

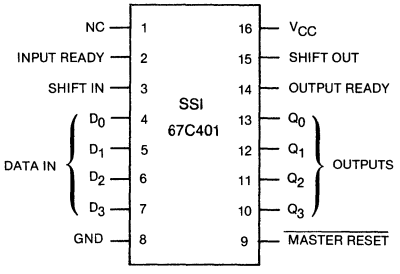


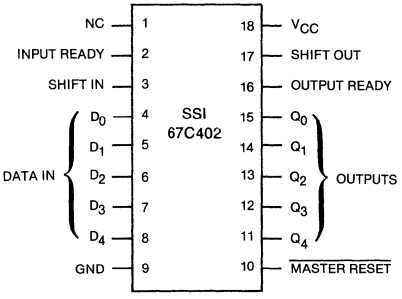
SSI 67C401 64x4



SSI 67C402 64x5

Pin Assignments





Pin Out (Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

CIRCUIT DESCRIPTION

Data Input

When the FIFO is reset, the Master Reset is pulsed low to prepare the device for data input. Data is entered at the D_X inputs as controlled by the Input Ready (IR) and Shift In (SI) logic. With IR high, data can be accepted. Data present at the data inputs is entered into the first position on the rising edge of SI. As SI is taken high, IR goes low indicating the FIFO is busy. When SI is set low, IR goes high if the memory is not full. In the FIFO, data is shifted towards the output progressively until a full memory position is encountered. Thus, the memory is filled with the first data word at the output position and subsequent data words in order behind it. If the memory is full, that is all 64 word positions contain valid data, IR remains low after SI is set low.

Data Transfer

After data input, transfer of a data word from a memory position to an adjacent empty memory position is automatic, activated by on-chip control. Thus, data stacks up at the output end of the FIFO while memory positions that are emptied as data is unloaded are moved to the input end. The time for data (or emptied positions) to move the entire length of the memory is defined as the throughput, or fall through, time (t_{PT}).

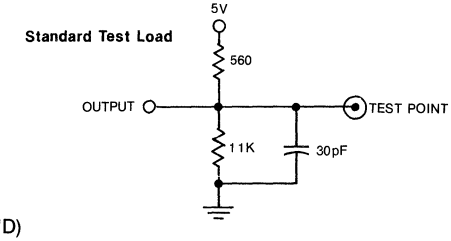
Data Output

Data outputs at the Q_X pins are controlled by the Output Ready (OR) and Shift Out (SO). When valid data is shifted to the outputs, OR goes high. With OR high, data may be shifted out by bringing SO high. The rise of SO causes OR to go low. Valid data is maintained while SO is high. When SO is brought low, the upstream data (providing the next stage contains valid data) is shifted to the output stage and OR goes high. If the FIFO is emptied, OR stays low and the Q_X data remains as before.

Application Notes

The Input Ready (IR) and Output Ready (OR) may be used as status signals indicating that the FIFO is completely full (IR stays low for at least fall through time t_{pt}) or that the FIFO is completely empty (OR stays low for at least t_{pt}).

Since the high speed FIFO is particularly sensitive to small glitches as might be caused by long reflective lines, high capacitances, or poor supply decoupling and grounding, circuit design should account for these potential problems ensuring that adequate ground planes and decoupling measures are taken. For example, it is recommended that a 0.1 μf ceramic capacitor be connected directly between V_{CC} and ground with a very short lead length.



Absolute Maximum Ratings* (All voltages referenced to GND)

Parameter	Symbol	Value	Units
Supply Voltage	V_{CC}	7	VDC
Input Voltage	V_{in}	7	VDC
Output Voltage	V_{out}	5.5	VDC
Storage Temperature Range	T_{stg}	−65 to +125	°C

* Operation above absolute maximum ratings may permanently damage the device

Electrical Characteristics ($4.75 \leq V_{CC} \leq 5.25$ V, $0\,°C \leq T_A \leq 75\,°C$ unless otherwise specified)

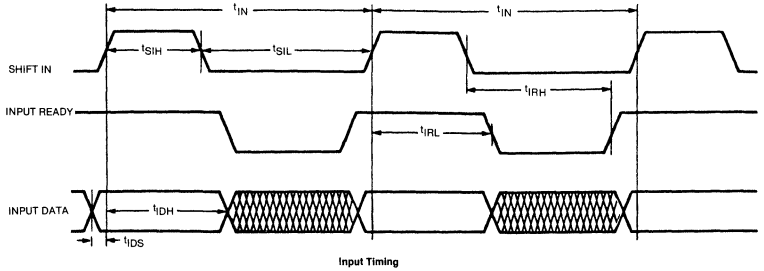
Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IL}	Low-Level Input Voltage	—	—	0.8	V
V_{IH}	High-Level Input Voltage	—	2	—	V
I_{IL}	Low-Level Input Current	V_{CC} = MAX V_{in} = 0.4V	—	−0.4	mA
I_{IH}	High-Level Input Current	V_{CC} = MAX V_{in} = 2.4V	—	50	μA
I_{IMH}	Maximum Input Current, High	V_{CC} = MAX V_{in} = 5.5V	—	1	mA
I_{IML}	Maximum Input Current, Low	V_{CC} = MAX V_{in} = 0.5V	—	15	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN I_{OL} = 8mA	—	0.4	V
V_{OH}	High-Level Output Voltage	V_{CC} = MIN I_{OH} = −4.0mA	4.0	—	V
I_{OS}	Output Short-Circuit Current†	V_{CC} = 5V, V_{out} = 0.5V	—	−80	mA
		V_{CC} = 5V, V_{out} = 4.5V	—	−80	
I_{CC}	Supply Current	V_{CC} = MAX, V_{in} = V_{CC} or GND, Outputs Open Ckt	—	100	μA

† Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

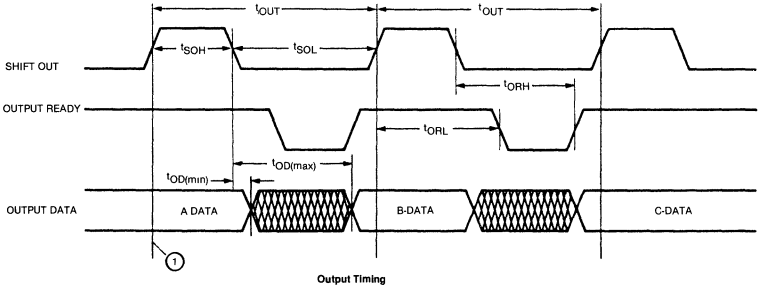
Switching Characteristics Over Operating Conditions

Symbol	Parameter	Min	Max	Unit
t_{IN}	Shift In Rate (Period between data loading)	100	—	ns
t_{SIH}	Shift In HIGH Time	35	—	ns
t_{SIL}	Shift In LOW Time	35	—	ns
t_{IRL}	Shift In to nput Ready LOW	—	45	ns
t_{IRH}	Shift In to Input Ready HIGH	—	45	ns
t_{IDS}	Input Data Set Up	0	—	ns
t_{IDH}	Input Data Hold Time	45	—	ns
t_{OUT}	Shift Out Rate (Period between data unloading)	100	—	ns
t_{SOH}	Shift Out HIGH Time	35	—	ns
t_{SOL}	Shift Out LOW Time	35	—	ns
t_{ORL}	Shift Out to Output Ready LOW	—	55	ns
t_{ORH}	Shift Out to Output Ready HIGH	—	55	ns
t_{OD}	Output Data Delay	10	55	ns
t_{PT}	Data Throughout (fall through) time	—	3	μs
t_{MRW}	Master Reset Pulse[2]	35	—	ns
t_{MRORL}	Master Reset to OR LOW	—	60	ns
t_{MRIRH}	Master Reset to IR HIGH	—	60	ns
t_{MRS}	Master Reset to SI	35	—	ns
t_{IPH}	Input Ready Pulse HIGH	30	—	ns
t_{OPH}	Output Ready Pulse HIGH	30	—	ns

[2] Master reset puts the register logic to "all cells empty", and sets IR high.



Input Timing



Output Timing

Figure 3. Timing Waveforms

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

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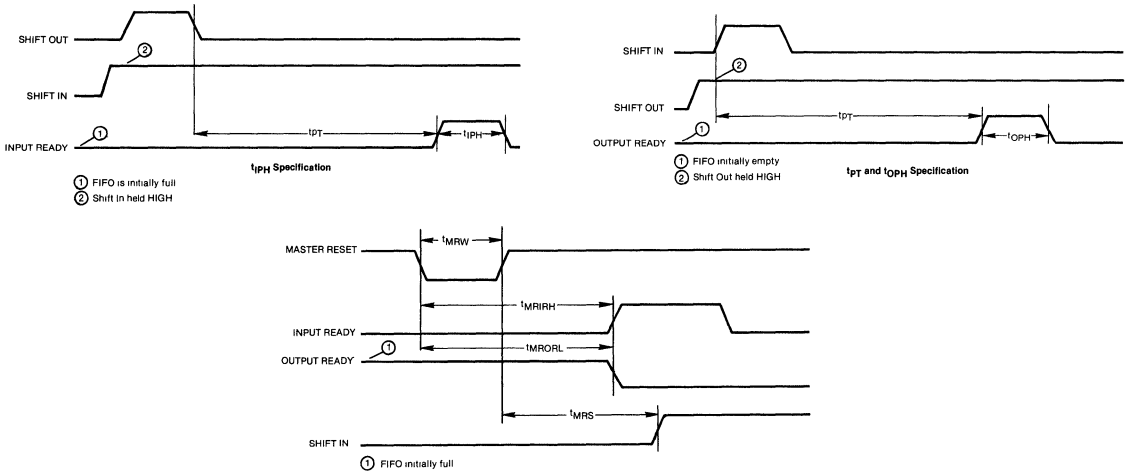


Master Reset Timing

Figure 4. Timing Waveforms

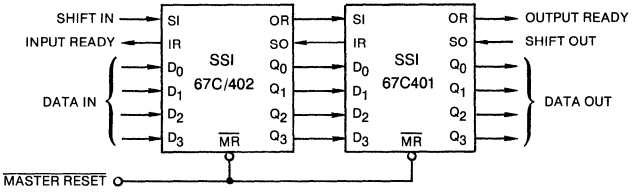


Figure 5. Cascading FIFOs to Form 128x4 FIFO.

FIFOs can be easily cascaded to any desired depth The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves

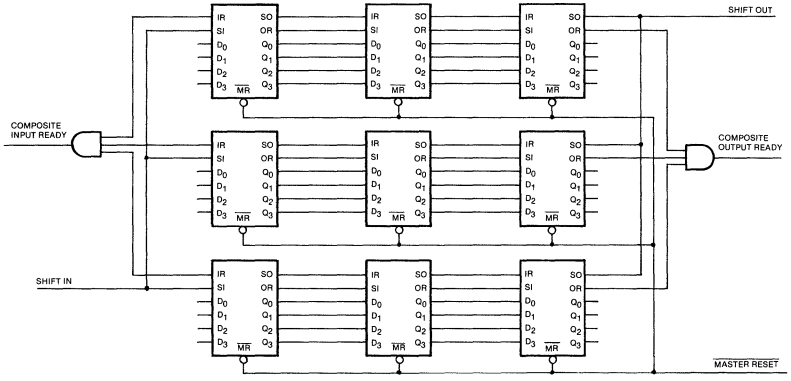


Figure 6. 192x12 FIFO.

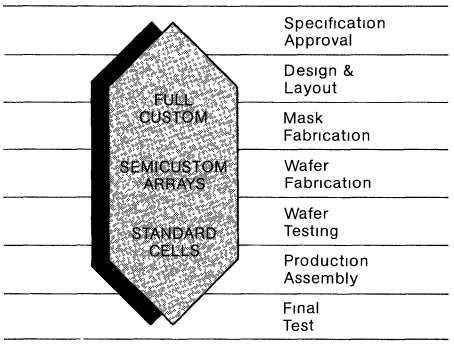
FIFOs are expandable in depth and width However, in forming wider words two external gates are required to generate composite Input and Output Ready flags This need is due to the different fall through times of the FIFOs

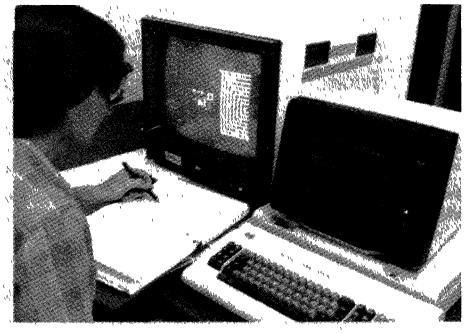
Section 3
CUSTOM/ SEMICUSTOM

SILICON SYSTEMS – LEADING THE WAY IN CUSTOM/SEMICUSTOM IC'S

At SSI, we've been in a leadership role in custom circuits, first with superior IC design capabilities, and then with one of industry's finest wafer fabrication facilities Today we're still pacing the field in the burgeoning market for "application specific" custom/semicustom IC's. We've maintained our position by carefully monitoring evolving market requirements and providing cost-effective, quality solutions for even the most specialized applications

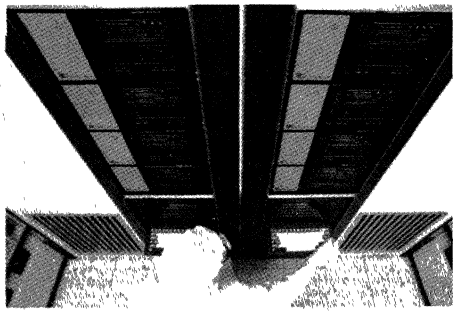
In both engineering and technology, we offer versatility· with design capabilities for digital, analog, and combined digital/analog ICs along with a wafer fabrication capability that includes both Bipolar and CMOS technologies





Custom/Semicustom Approach to Integrated Circuits

Custom IC's are not just a side line at SSI; they've always been our primary business We provide the full range of custom IC design with such practical semicustom options as pre-built standard cells and switched capacitor filter arrays. With a top engineering staff supported by our unique Integrated Design Methodology (IDM), and with a fully automated wafer



fabrication facility designed especially for custom and "Application-Specific" IC's, we can cut custom design time down to readily acceptable limits

Integrated Solution for You

So whether your requirements fall in our specialty areas of telecommunications and rotating memories, or other application areas appropriate for custom/semicustom IC's, we offer the advantages of a complete IC development and production operation; single-point accountability, smooth progress through all phases of a project, and a high level of quality assurance. The result· reduced time and cost to produce the best custom/semicustom IC's available.

VERSATILITY – THE OPTIMUM APPROACH FOR EACH CUSTOMER

Silicon Systems has focused on the ASIC (Application Specific Integrated Circuit) market for over 10 years and has developed a versatile offering of customized components that covers the design spectrum.

The digital market can be satisfied by our Mask Programmed Logic Arrays (MPLA) for implementation of complex logic functions and by our full custom or standard cell library for large scale system designs

ANALOG APPLICATIONS	SSI CAPABILITY
• Functions – (Filters, Signal Conditioning, Etc.)	Switched Capacitor Array
• Systems – (Data Acquisition, Signal Processing, Etc.)	Analog/Digital Full Custom and Standard Cell Design

Table 1

The analog market is served by our Bipolar analog array for moderate complexity needs, by switch capacitor arrays for filter needs and by full custom or standard cell library for higher levels of sophistication. All four design technologies also accommodate full analog and digital integration on the same chip for total system solutions.

Design engineering, semiconductor processing and testing are all housed in the same facility at Silicon Systems which allows quick turn-around from design concept to working silicon The ultra-clean wafer fab supports both Bipolar and CMOS technologies with high and low voltage options as well as single or double layer metal interconnections. These variations permit us to select the optimum process when fabricating a new circuit

DIGITAL APPLICATION SPECTRUM

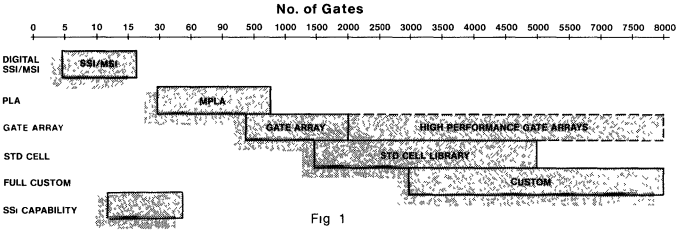


Fig 1

Our standard cell library is implemented on the CC process (3μm silicon gate CMOS) allowing high density, low power digital and analog functions to be integrated, while operating with standard 5-volt levels The proprietary "CD" process extends operation from 3 5V to 14V for higher performance analog or analog/digital functions while our proprietary Bipolar "BJ" process offers extremely high density and performance combined with very low noise.

Silicon Systems also offers full capability for supporting Customer Owned Tooling (COT) with any of our industry standard processes.

CMOS PROCESS CHART

Process Designation	Channel	V_{TPO} (volts)	V_{TO} (volts)	BV_{DSS} (volts)	K'	N or P (Ω/□)	Poly (Ω/□)	Channel Length (microns)	Poly Pitch (microns)	M1 Pitch (microns)	M2 Pitch (microns)	Options/ Comments
CB	P	-20	-0.9	-20	11	80	–	9.0	–	12.5	–	High Voltage Al Gate
	N	20	0.9	20	17	16	–	7.2	–	12.5	–	
CC	P	-12	-0.9	-12	16	55	20	3.0	6.4	8.8	12	Double Metal, Single Poly (includes capacitors) Si Gate
	N	12	0.7	12	45	25	20	3.0	6.4	8.8	12	
CD	P	-18	-0.9	-18	16	55	20	4.0	6.4	8.8	–	Single Metal, Double Poly
	N	18	0.7	18	50	25	20	4.0	6.4	8.8	–	

Table 2A

BIPOLAR PROCESS CHART

Process Designation	h_{FE}	BV_{CEO} (volts)	BV_{CBO} (volts)	Base		epi		n^+BL		Min. geometry (microns)	M1 Pitch (microns)	M2 Pitch (microns)	Options/ Comments
				ρ_s	x_j	ρ_t	t	ρ_s	x_j				
BC	60	12	25	200	1.2	0.75	4.4	25	5.5	5	14	24	Double Metal Al Schottky Typical f_T 1000 MHz
BJ	60	9	20	350	1.0	0.5	3.9	20	5.5	3	9	14	Double Metal Al Schottky Poly Emitter Typical f_T 2000 MHz

Table 2B

When deciding to convert a system or subsystem design to silicon the user can choose either a fully customized approach or a semi-customized approach, each with its own benefits For these designs SSI offers the alternatives of fully "handcrafted" custom design in CMOS and Bipolar or standard cell design in CMOS As seen in Table 3, the fully individualized custom gives the advantages of chip size (lower production cost) and highest performance (speed, input offset, etc.) while semicustom, using a pre-characterized standard cell library, offers the advantages of lower NRE, faster turnaround and somewhat higher first article success rate. SSI adds to the flexibility of the standard cell concept by its willingness to develop special cells as needed to satisfy design requirements that lie between the two custom design technologies.

With Computer Aided Design (CAD) playing a major role in our product development cycle, SSI has developed an Integrated Design system that accommodates an interlocking set of design methods all supported by a single CAD system. This Integrated Design Methodology (IDM™) allows the user to design at the transistor level (either composite or symbolic), at a procedural macro level (silicon compiler), with Parameterized Building Blocks (PBB), or with conventional standard cells. Each of these design levels has a unique set of attributes, as shown in Figure 2, accessible in a "mix or match" manner under IDM. This enables an efficient performance/design-time tradeoff.

INTEGRATED DESIGN METHODOLOGY

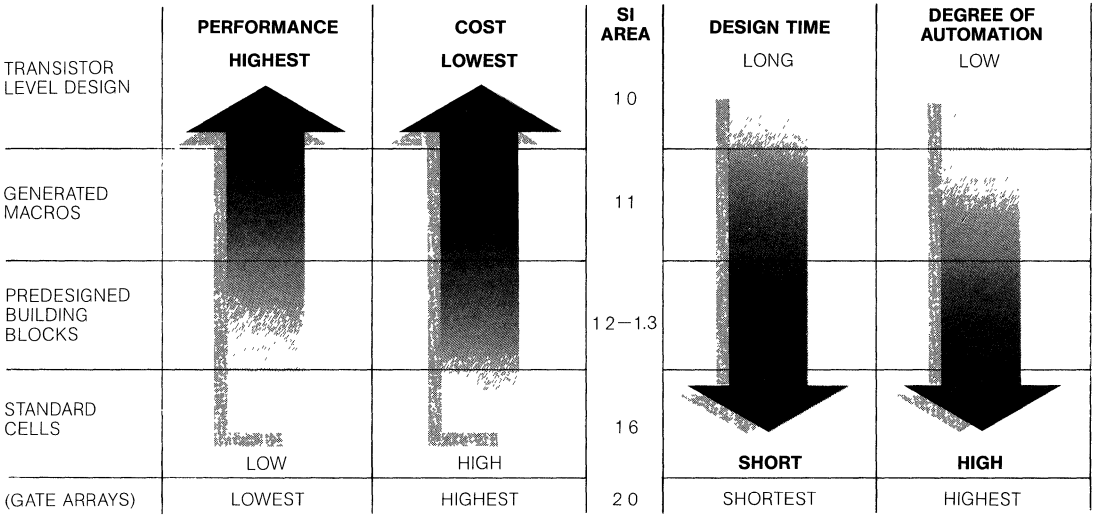


Figure 2

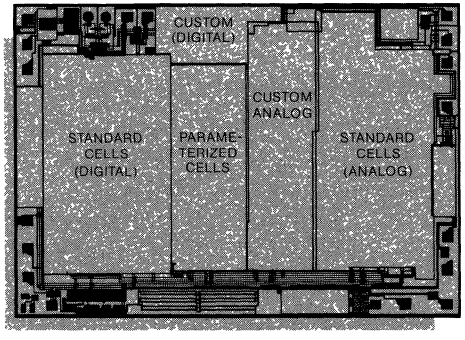
COMPARISON OF CUSTOM/ SEMICUSTOM LSI OPTIONS

Processes	Standard Cell	Full Custom
Bipolar	No	Yes
CMOS	Yes	Yes
Analog	Yes	Yes
Digital	Yes	Yes
Analog/Digital Mix	Yes	Yes
Development Parameters		
Cost	0.3-0.5	1.0
Time	0.25-0.40	1.0
Risk Factor	0.5	1.0
Production Parameters		
Final Die Size	1.3-1.6	1.0
Die Cost	1.5-2.0	1.0

All comparisons normalized to a full custom basis.

Table 3

MACRO IC USING IDM



"CUSTOMIZED SERVICE" – TOTAL SUPPORT FROM CONCEPT THROUGH FINAL TEST

Silicon Systems offers experienced staffing throughout its organization along with state-of-the-art CAD and processing facilities to efficiently develop customized products.

We start with a large, expert staff of design engineers to help define the product from both the system and silicon aspects The design is then developed using our advanced CAD tools and programs including ALICE (Automated Layout for Integrated Circuit Engineering), which accurately handles chip design from schematic input to pattern generator output, all within one system. SSI engineers utilize an advanced version of "SPICE" to simulate DC, transient, noise, distortion, and AC response for CMOS and Bipolar. It accurately models such second order effects as weak-inversion, high-level injection, temperature dependent mobility, etc

SSI has adapted a special program called "SWITCAP" for switched-capacitor filter frequency domain analysis which accurately predicts the frequency response of switched-capacitor filters. Our Automatic Network Intertrace Algorithm (ANITA™) compares the network description generated from the captured circuit to the layout as it proceeds This guarantees that no interconnection errors exist and that all component sizes and tolerances match those used in the design analysis. The completed design goes through a masking procedure and the wafers are run in our ultramodern class 10 (10ppm particulate count) wafer fabrication facility It is a "paperless"

CUSTOM/SEMICUSTOM SUPPORT CAPABILITIES
• SOFTWARE SUPPORT SIMULATION SPICE, DAISY LOGICIAN, ILOGS, SWITCAP LAYOUT and ROUTING ALICE, ANITA, CAL-MP
• COMPUTERS and WORKSTATIONS VAX 11/780, DAISY, MENTOR
• TEST HARDWARE LTX TESTERS EAGLE (LSI-4) TESTERS AUTOMATIC HANDLERS BURN-IN SOCKETS, TEMPERATURE CHAMBERS

Table 4

environment accomplished by downloading process information to in-place terminals and processing equipment The PROMIS (Process Management Information Systems) program that accomplishes this control provides work-in-process tracking, engineering data collection,

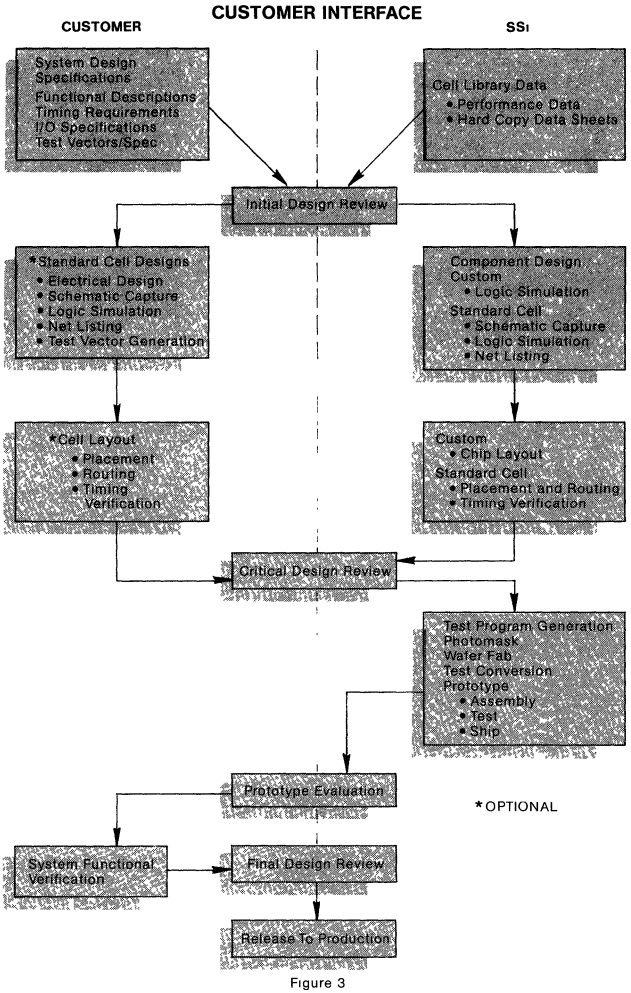


Figure 3

and continuous facility monitoring

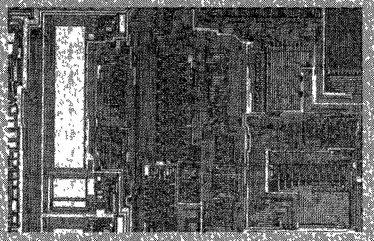
After the wafer prototype is fabricated, SSI packages a few representative chips using in-house assembly for design verification. The units are tested in-house by one of our advanced analog or digital tester We can test your circuit with your existing test program or help you create a test program from your specification.

After approval of prototypes or characterization lots (if needed) the final step is off-shore assembly for volume production

We can also perform hi-rel screening and burn-in, if desired.

CUSTOM – THE "TAILORED" APPROACH

CMOS

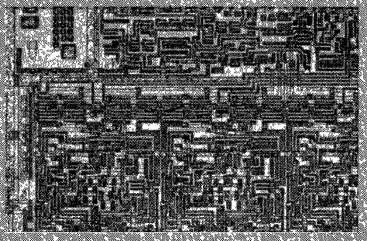


Integrated Circuit Function	Application
Dual Tone Multi Frequency Receiver	*Decodes Touch-Tone® Telephone Signals
1200/2400 Baud Receiver	Phase Shift Keying (PSK) Modem
Phoneme-Based Speech Synthesizer	"Talking" Machines
Error Corrector	Military Radio
Variable Counter	Jam-Resistant Radio
Touch Activated Switch	Home Lamps
Video Processor	Infrared Video System
16 Channel Switching Matrix	Bank Communications System
Custom Microprocessor	Computer Terminal
Digital Loop Detector	Traffic Signal Control
Programmable Digital Receiver	Home Appliance Remote Control

*Touch-Tone is a trademark of AT&T

Table 8

BIPOLAR



Integrated Circuit Function	Application
AGC & Level Control Signal Processor	Infrared Video System
Pulse Width Modulation Controller	Switching Power Supply
5-Channel Read/Write Amplifier	OEM Winchester Disk Drives
Thin-film Read/Write Amplifier	IBM 3370/3380 Compatible Disk Drives
VHF/UHF Gain Mixer	Radio Receiver
Regulator/Timer	Highway Barricade Flasher
8-Channel Bidirectional Buffer	Microprocessor Peripheral IC
12-Bit Range Counter	Laser Range Finder
PCM Encoder/Decoder	Telecommunications System
Video Controller/ Timing Generator	Dot Matrix CRT Terminal

Table 9

AVAILABLE PACKAGES

NO. OF PINS	Dual-in-Line Plastic	Dual-in-Line Cerdip	Flat Pack	Plastic Quad PLCC (Surface Mount)
	PACKAGE DESIGNATOR			
	P	D	F	H
8	●	●	–	–
10	–	–	●	–
14	●	–	–	–
16	●	–	–	–
18	–	–	–	–
22	●	●	–	–
24	●	●	●	–
28	●	●	●	●
32	–	–	●	–
40	●	●	–	–
44	–	–	–	●
68	–	–	–	●
84	–	–	–	●

Table 11

HI-REL SCREENING OPTIONS

- Reliability Screening (Method 5004)
- Qualification and Quality Conformance Procedure (Method 5005)
- Pre-Seal Visual Inspection (Method 2010)
- Stabilization Bake (Method 1008)
- Temperature Cycle (Method 1010)
- Thermal Shock
- Constant Acceleration
- Fine Leak (Method 1014)
- Gross Leak (Method 1014)
- Burn-in
- SEM Analysis of Wafer Lots (Metallization)

Table 10

The above tables show some of our demonstrated high performance design capabilities in Bipolar and CMOS. These analog/digital chips cover a wide range of challenging circuit functions that were designed for a diversity of system applications.

As part of a total capability SSI offers commercial, industrial, and hi-rel product flows, as well as packaging options that include Dual-in-Line, Flatpacks, and plastic Quads. For further detailed information on product flow and packaging call SSI or refer to our Quality and Reliability Brochure.

Section 4
STANDARD CELLS

SSI STANDARD CELL FAMILY (PARTIAL LIST)

ANALOG CELLS	DIGITAL CELLS	DIGITAL CELLS
Analog Switch Array	Two Input NOR	Three Input AND
Switched Capacitor Amplifier	Three Input NOR	Four Input AND
OP Amp. External Use	Four Input NOR	Two Input OR
OP Amp. Internal Use	Two Input NAND	Three Input OR
Gain Block	Three Input NAND	Four Input OR
Capacitor Array	Four Input NAND	3x2 AND-OR-Invert
Bias Generator	Inv/Non-Inverting Buffer	2x2 AND-OR-Invert
RC Oscillator	Buffer Inverter	2x1 AND-OR-Invert
Multiplying Differential D/A Converter	Transmission Gate	D Flip Flop (2 Versions)
High Accuracy Sample and Hold	Single Clock/Dual Transmission Gate	D Flip Flop with Set (Overrides) and Reset
Power On Reset	Inverting Tri-State	D Flip Flop with Set and Reset (Overrides)
OP Amp. Buffer	Non-Inverting Tri-State	Transparent D Latch
Supply Divider	RS NAND Latch	Exclusive OR (2 Versions)
Voltage Comparator	RS NOR Latch	Input Inverting I/O Cell
8 Bit A/D Converter	Low Impedance Inverter	Input Inverting I/O Cell
Low Impedance Driver	High Impedance Inverter	Output Inverting Driver I/O Cell
	Double Buffer Inverter	Bi-Directional Tri-State I/O Cell
	Tri-State Driver	Output Non-Inverting Driver I/O Cell
	Two Input Decoder	Input Transmission I/O Cell
	Two Input AND	Input Pad with Protection
	8 Bit Magnitude Comparator	Input Schmitt Trigger (4 Versions)

Table 5

The standard cells shown in Table 5 represent the basic building blocks or "primitives" of our present library. In addition to these cells, macros are already scheduled for functions such as RAM, ROM, PLA etc. Others can be generated and added to the library on an "as needed" basis. As part of the SSI flexibility in custom we will design new cells to accommodate any feasible "special" requirements.

DIGITAL CHARACTERISTICS

4.5V ≤ VDD ≤ 5.5V, −40°C ≤ Temp ≤ 125°C

		Nom	Max	Units
Propagation Delays				
2 Input NAND	TPLH	2.5	8.0	nsec
	TPHL	1.7	3.8	nsec
RS Flip-Flop	TPLH	5.0	10.7	nsec
	TPHL	1.5	3.3	nsec
D Flip-Flop	TPLH	4.0	8.8	nsec
(clk to QB)	TPHL	3.2	7.6	nsec
Buffer/Driver	TPLH	1.0	3.1	nsec
(inverting)	TPHL	0.8	2.5	nsec

Nominal Measured at 5V, 25°C

Table 6

ANALOG CHARACTERISTICS

4.5V ≤ VDD ≤ 5.5V, −40°C ≤ Temp ≤ 125°C

	Min	Nom	Max	Units
Operational Amplifier				
Input Offset	–	5	15	mv
Unity Gain Bandwidth	–	2.5	–	MHz
Open Loop Gain	3000	–	–	V/V
Comparator				
Input Offset Voltage	–	1	10	mv
Conversion Time	–	–	1.5	μsec
Multiplying Digital/Analog Converter				
Acquisition Time	–	2	6	μsec
Non-Linearity	–	–	1/2	LSB
Clock Frequency	–	20	–	MHz

Nominal Measured at 5V, 25°C

Table 7

The characteristics shown in Table 6 are indicative of our cell library in 5 Volt 3μm Si gate CMOS (CC process). An additional library of higher performance analog cells will be made available on our CD process.

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BASIC STANDARD CELL LIST

CELL NUMBER	DESCRIPTION
BASIC LOGIC FUNCTIONS	
C1120	2 IN NOR GATE
C1130	3 IN NOR GATE
C1140	4 IN NOR GATE
C1220	2 IN NAND GATE
C1230	3 IN NAND GATE
C1240	4 IN NAND GATE
C1300	INVERT/NON-INVERT PAIR
C1310	INVERTER (1X)
C1320	TRANS. GATE (ENABLE*)
C1330	DUAL TRANS. GATE (COMP ENABLES)
C1360	INVERTER TRI STATE (ENABLE*)
C1380	BUFFER TRI STATE (ENABLE*)
C1410	LATCH R*/S*
C1420	LATCH R/S
C1430	LATCH R R/S (CROSS COUPLED NORS)
C1440	LATCH R* R*/S* (CROSS COUPLED NANDS)
C1500	INVERTER (3X)
C1520	INVERTER (2X)
C1540	INVERTER
C1580	NAND NOR/INVERT
C1590	I1 NOR I2 I1 NOR I2*
C1610	I1 NOR I2*
C1620	NAND/AND (2 INPUT)
C1630	NAND/AND (3 INPUT)
C1640	NAND/AND (4 INPUT)
C1720	NOR/OR (2 INPUT)
C1730	NOR/OR (3 INPUT)
C1740	NOR/OR (4 INPUT)
C1840	AND-NOR (6 INPUT)
C1870	AND-NOR (4 INPUT)
D FLIP FLOPS	
C2120	DFF (C*)
C2130	DFF (C)
C2140	DFF (C*, R, S)
C2150	DFF (C, R, S*)
C2160	DFF (C*, R, S*)
C2170	DFF (C, R, S*)
C2820	DFF (C)
C2830	DFF (C*)
C2920	DFF (C*)
C2930	DFF (C)
C20050	D FLIP FLOP (HIGH SPEED)
SPECIAL LOGIC	
C4000	8 BIT MAG COMP WITH ENABLE
C4080	D LATCH (C, R)
C4090	D LATCH (C*, R)
C4110	PRESET FLIP FLOP
C4120	PRESET FLIP FLOP
C4310	XOR
C2310	XOR
FEED THRU CELLS	
C9410	WELL AND SUB TIE-DOWNS FEED THRU
C9450	POLY FEED THRU

CELL NUMBER		DESCRIPTION
I/O CELLS (10MIL PADS)		
C5001	8540	INPUT INVERTER (1X)
C5002	8620	INPUT SCHMITZ TRIG NON-INVERT
C5003	8530	INPUT INVERTER (3X)
C5004	8550	OUTPUT INVERTER
C5005	8630	INPUT SCHMITZ TRIG INVERT
C5006	8580	INPUT NON-INVERT/TRI-STATE OUTPUT NON-INVERT
C5007	8960	INPUT PAD WITH PROTECTION
C5008	8600	OUTPUT NON-INVERT BUFFER
C5009	20160	POSITIVE SUPPLY
C5010	8980	TRANSMISSION GATE INPUT
I/O CELLS (20MIL PADS)		
C8530		INPUT INVERTER (3X)
C8540		INPUT INVERTER (1X)
C8550		OUTPUT INVERTER
C8580		INPUT NON-INVERT/TRI-STATE OUTPUT NON-INVERT
C8600		OUTPUT NON-INVERT BUFFER
C8620		INPUT SCHMITZ TRIG NON-INVERT
C8630		INPUT SCHMITZ TRIG INVERT
C8720		CRYSTAL OSCILLATOR
C8730		CRYSTAL OSCILLATOR WITH ENABLE*
C8960		INPUT PAD WITH PROTECTION
C8980		TRANSMISSION GATE INPUT
I/O CELLS		
C20110		OUTPUT BUFFER INVERTER
C20120		OUTPUT OPEN DRAIN INVERTER
C20130		INPUT BUFFER INVERTER SCHMITZ TRIG
C20140		CRYSTAL OSCILLATOR
C20160		NEGATIVE SUPPLY PAD
C20170		POSITIVE SUPPLY PAD WITH PROTECT DIODE
C20010		OUTPUT BUFFER INVERTER
C20020		OUTPUT OPEN DRAIN INVERTER
C20030		INPUT BUFFER INVERTER SCHMITZ TRIG
C20040		CRYSTAL OSCILLATOR
C20060	C21060	INPUT NEGATIVE SUPPLY
DYNAMIC ANALOG STD CELLS		
ASW		QUAD ANALOG SWITCH
SCMP		SWITCHED CAPACITOR AMPLIFIER
GB −6DB		GAIN BLOCK (−6DB)
GB −3DB		GAIN BLOCK (−3DB)
GB 0DB		GAIN BLOCK (0DB)
GB 3DB		GAIN BLOCK (3DB)
GB 6DB		GAIN BLOCK (6DB)
GB 12DB		GAIN BLOCK (12DB)
CRAY		CAPACITOR ARRAY (UNIQUE PER DESIGN)
MDAC		MULTIPLYING DIFFERENTIAL D/A CONVERTER
HASH		SAMPLE AND HOLD
VCMP		VOLTAGE COMPARATOR
CLASSICAL STD CELLS		
OAEX		OP AMP, EXTERNAL USE
OAIN		OP AMP, INTERNAL USE
BGEN		BIAS GENERATOR FOR USE WITH OP AMPS
RCO		RC OSCILLATOR
POR		POWER ON RESET
OABF		OP AMP, BUFFER
SDIV		SUPPLY DIVIDER

Section 5
GENERAL INFORMATION

TELECOMMUNICATIONS CIRCUITS

Device	Circuit Function	Features	Power Supplies	Package	Page No.
Tone Signaling Products					
SSI 201	Integrated DTMF Receiver	Binary or 2-of-8 output	12V	22 DIP	1-4
SSI 202	Integrated DTMF Receiver	Low-power, binary output	5V	18 DIP	1-8
SSI 203	Integrated DTMF Receiver	Binary output, Early Detect	5V	18 DIP	1-8
SSI 204	Integrated DTMF Receiver	Low-power, binary output	5V	14 DIP	1-12
SSI 207	Integrated MF Receiver	Detects central office tone signals	10V	20 DIP	1-16
SSI 20C89	Integrated DTMF Transceiver	Generator and Receiver, μP interface	5V	22 DIP	1-26
SSI 20C90	Integrated DTMF Transceiver	Generator and Receiver, μP interface, Call Progress Detect	5V	22 DIP	1-32
SSI 957	Integrated DTMF Receiver	Early Detect, Dial Tone reject	5V	22 DIP	1-38
SSI 980	Call Progress Detector	Detects supervision tones, Teltone second-source	5V	8 DIP	1-44
SSI 981	Precise Call Progress Detector	Detects supervision tones, Teltone second-source	5V	22 DIP	1-48
SSI 982	Precise Call Progress Detector	Detects supervision tones, Teltone second-source	5V	22 DIP	1-48
Modem Products					
SSI K212	1200/300 bps Modem	DPSK/FSK, single chip, autodial, Bell 212A	10V	28, 22 DIP	1-52
SSI K214	2400 bps Analog Front End	Analog Processor for DSP V.22 bis Modems	10V	28 DIP	1-60
SSI K222	1200 bps Modem	V.22 version of K212, Pin Compatible	5V	28, 22 DIP	1-62
SSI 223	1200 bps Modem	FSK, HDX/FDX	10V	16 DIP	1-68
SSI K224	2400 bps Modem	V.22 is version of K212, Pin Compatible	10V	28, 22 DIP	1-72
SSI 291/213	1200 bps Modem	DPSK, two chips, low-power	10V	40/16 DIP	1-76
SSI 3522	1200 bps Modem Filter	Bell 212 compatible, AMI second-source	10V	16 DIP	1-82
Speech Synthesis Products					
SSI 263A	Speech Synthesizer	Phoneme-based, low data rate, VOTRAX second-source	5V	24 DIP	1-86
Switching Products					
SSI 80C50	T1 Transmitter	Bell D2, D3, D4, serial format and mux, low power	5V	28 DIP,Q	1-100
SSI 80C60	T1 Receiver	Bell D2, D3, serial synchron. and demux, low power	5V	28 DIP,Q	1-106
SSI 22100	Cross-point Switch	4x4x1, control memory, RCA second-source	12V	16 DIP	1-112
SSI 22101/2	Cross-point Switch	4x4x2, control memory, RCA second-source	12V	24 DIP	1-118
SSI 22106	Cross-point Switch	8x8x1, control memory, RCA second-source	5V	28 DIP	1-124
SSI 22301	PCM Line Repeater	T1 carrier signal recondition	5V	18 DIP	1-132

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SSI MPD Product Selector Guide

MICROPERIPHERAL PRODUCTS

Device	Head Type	# of Channels	Power Supplies	Internal Write Current Source	Internal Center Tap Voltage Source	Internal R_d Option	Read Gain (typ)	Write Current Range (mA)	Read/Write Data Port(s)	Page No.
HDD Read/Write Amplifiers										
SSI 104	Ferrite	4	+6V, −4V			x	35	15 to 45	Differential, Bi-directional	2-2
SSI 104L	Ferrite	4	+6V, −4V			x	35	15 to 45	Differential, Bi-directional	2-2
SSI 108	Ferrite	4	+6V, −4V			x	35	15 to 45	Differential, Bi-directional	2-2
SSI 114	Thin Film	4	±5V	x	N/A	x	123	55 to 110	Differential/Differential	2-6
SSI 115	Ferrite	2,4,5	±5V		x		40	30 to 50	Differential, Bi-directional	2-10
SSI 117	Ferrite	2,4,6	+5V, +12V	x	x	x	100	10 to 50	Differential/TTL	2-16
SSI 117A	Ferrite	2,4,6	+5V, +12V	x	x	x	100	10 to 50	Differential/TTL	2-22
SSI 122	Ferrite	4	+6V, −4V				35	15 to 45	Differential, Bi-directional	2-2
SSI 188	Ferrite	4	+6V, −5V		x		43	35 to 70	Directional, Bi-directional	2-28
SSI 501	Ferrite	6,8	+5V, +12V	x	x	x	100	10 to 50	Differential/TTL	2-34
SSI 510	Ferrite	4	+5V, +12V	x	x	x	100	10 to 35	Differential/TTL	2-40
SSI 520	Thin Film	4	±5V	x	N/A	x	123	30 to 75	Differential/Differential	2-46
SSI 521	Thin Film	6	+5V, +12V	x	N/A	x	100	20 to 70	Differential/TTL	2-50

Device	Function	Power Supplies	Features	Page No.
HDD Head Positioning				
SSI 101A	Preamplifier-Ferrite Head	8.3V/10V	Av = 93, BW = 10MHz, e_n = 7.0nV$\sqrt{Hz}$	2-54
SSI 101A-2	Preamplifier-Ferrite Head	+12V	Av = 93, BW = 10MHz, e_n = 7.0nV$\sqrt{Hz}$	2-54
SSI 116	Preamplifier-Thin Film Head	8.3V/10V	Av = 250, BW = 20MHz, e_n = 0.94nV$\sqrt{Hz}$	2-56
SS116-2	Preamplifier-Thin Film Head	+12V	Av = 250, BW = 20MHz, e_n = 0.94nV$\sqrt{Hz}$	2-56
HDD Read Data Path				
SSI 531	Data Separator	+5V	High Performance PLL, XTAL OSC, Write Precompensation	2-58
SSI 540	Read Data Processor	+5V, +12V	Time Domain Filter	2-66
SSI 541	Read Data Processor	+5V, +12V	AGC, Amplitude & Time Pulse Qualification, RLL Compatible	2-74
HDD Motor Control/Support Logic				
SSI 545	Support Logic	+5V	Includes 57506 Bus Drivers/Receivers	2-80
SSI 590	2-Phase Motor Speed Control	+12V	±0.035% Speed Accuracy	2-84
SSI 591	3-Phase Motor Speed Control	+12V	±0.05% Speed Accuracy	2-88
Floppy Disk Drive Circuits				
SSI 570	Read Data Path	+5V, +12V	2 Channel Read/Write With Read Data Path	2-92
SSI 575	Read/Write	+5V, +12V	2,4 Channel Read/Write Circuit	2-98
SSI 580	Support Logic	+5V, +12V	Port Expander, Includes SA400 Interface Drivers/Receivers	2-102
Tape Drive Circuits				
SSI 550	Read Data Path	+5V, +12V	4 Channel Read/Write w/ Read Data Path	2-108
Memory Products				
SSI 67C401	64 x 4 FIFO	+5V	Low Power, High Speed Buffer (10MHz, 15MHz)	2-114
SSI 67C402	64 x 5 FIFO	+5V	Low Power, High Speed Buffer (10MHz, 15MHz)	2-114

Dual-in-Line Package (DIP)	Pins	Page No.
PLASTIC	8 and 14 Pins	5-7
PLASTIC	16 and 18 Pins	5-8
PLASTIC	20 and 22 Pins	5-9
PLASTIC	24 and 28 Pins	5-10
PLASTIC	32 and 40 Pins	5-11

CERDIP	8 and 16 Pins	5-12
CERDIP	18 and 22 Pins	5-13
CERDIP	24 and 28 Pins	5-14

Surface Mounted Devices (SMD)	Leads	Page No.
PLCC (QUAD)	28 and 44 Leads	5-15

SMALL OUTLINE (SOIC)	8, 14 & 16 Leads SON*	5-16
SMALL OUTLINE (SOIC)	16 and 20 Leads SOL**	5-17
SMALL OUTLINE (SOIC)	24 and 28 Leads SOL	5-18

FLAT PACK	10, 24, 28 and 32 Leads	5-19

*SON is a 150 Mil width package.
**SOL is a 300 Mil width package.

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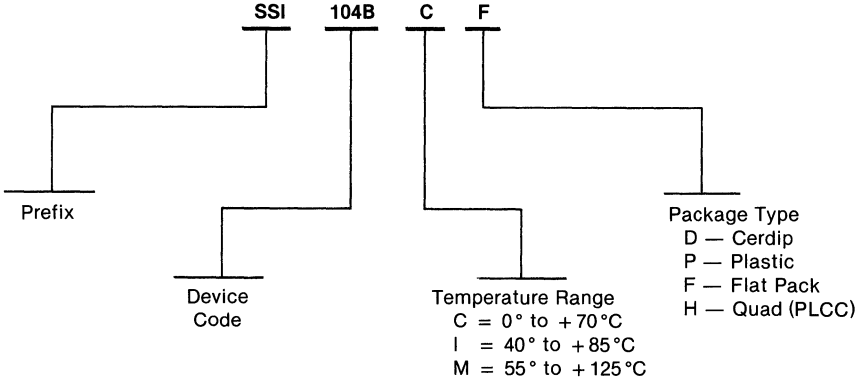
SSI Package Matrix

Device Type	Package Type			
	P Plastic	D Cerdip	F Flatpack	H PLCC
SSI 20C89	22			
SSI 20C90	22			
SSI 67C401	16			
SSI 67C402	18			
SSI 80C50	28			28
SSI 80C60	28			28
SSI 101A	8			
SSI 104			24	
SSI 105			24	
SSI 108	24			
SSI 114			24	
SSI 115-2	18			
SSI 115-4	22			
SSI 115-5	24		24	
SSI 116	8			
SSI 117-2	18			
SSI 117-4	22		24	
SSI 117-6	28		28	28
SSI 122	24			
SSI 188			28	
SSI 201	22	22		
SSI 202	18	18		
SSI 203	18	18		
SSI 204	14			
SSI 207	20			
SSI K212SER	22			
SSI K212	28			28
SSI 213	16			28
SSI K214	28			28
SSI K222SER	22			
SSI K222	28			28
SSI 223	16			

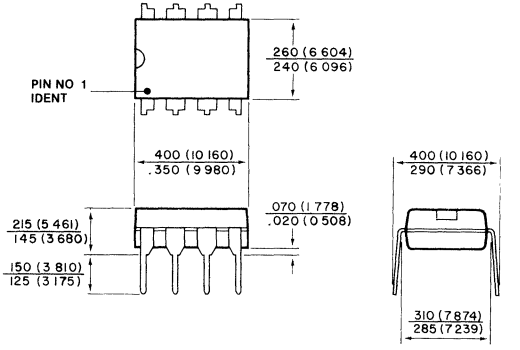
Device Type	Package Type			
	P Plastic	D Cerdip	F Flatpack	H PLCC
SSI K224SER	22			
SSI K224	28			28
SSI 263A	24			
SSI 291	40			
SSI 291Y	28			
SSI 501-6				28
SSI 501-8	40		32	44
SSI 510-4	22		24	
SSI 520			24	
SSI 521				28
SSI 531	24			28
SSI 540	28			28
SSI 541	24			28
SSI 545	40			44
SSI 550	40			
SSI 570	28			28
SSI 575-2	18			
SSI 575-4	24			
SSI 580	28			28
SSI 590-1	8			
SSI 590-2	14			
SSI 591	16			
SSI 957	22			
SSI 980	8			
SSI 981	22			
SSI 982	22			
SSI 3522	16			
SSI 22100	16			
SSI 22101	24			
SSI 22102	24			
SSI 22106	28			
SSI 22301	18			

Check with factory for availability of SOIC's

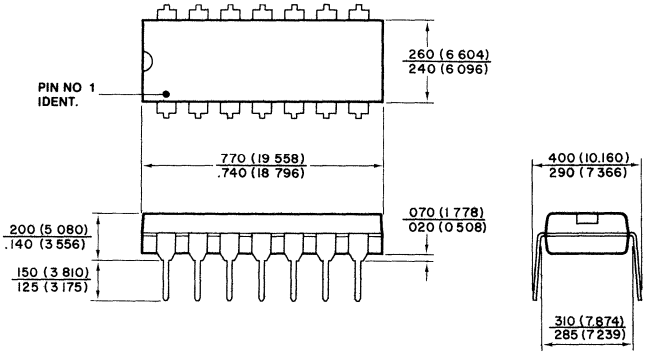
SSI Ordering Information



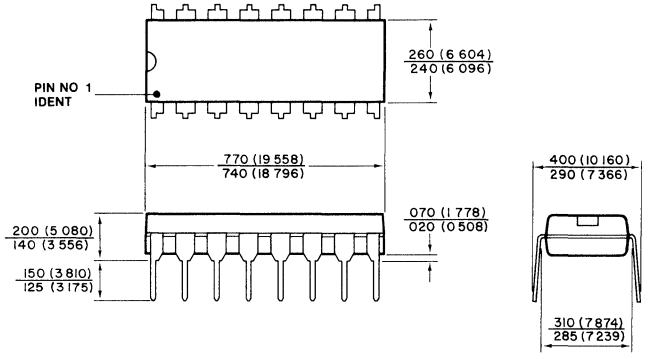
PLASTIC DIP
8 Pins



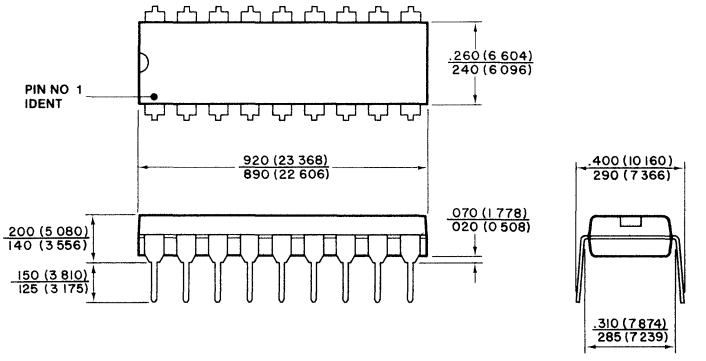
PLASTIC DIP
14 Pins



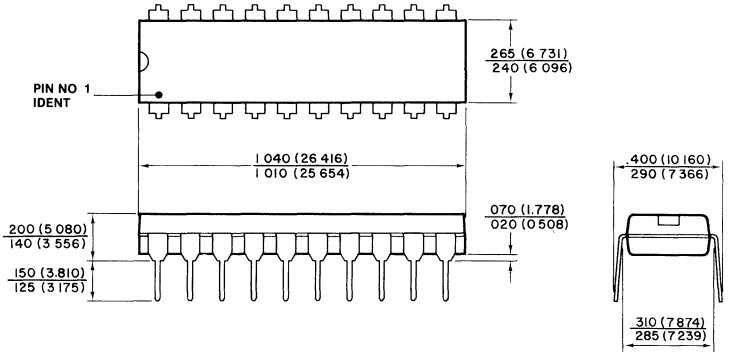
PLASTIC DIP
16 Pins



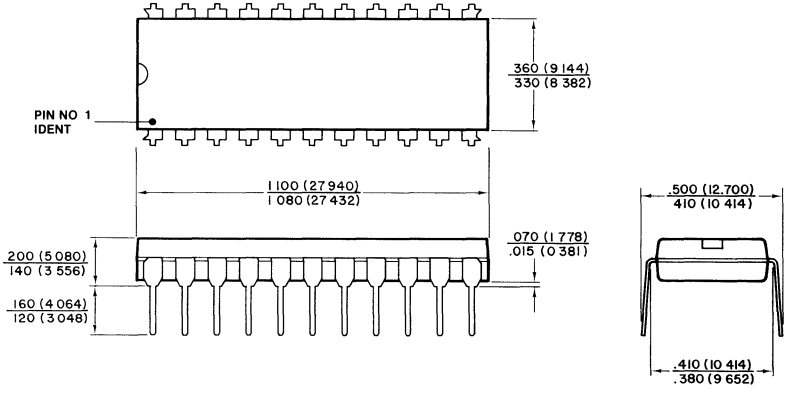
PLASTIC DIP
18 Pins



PLASTIC DIP
20 Pins

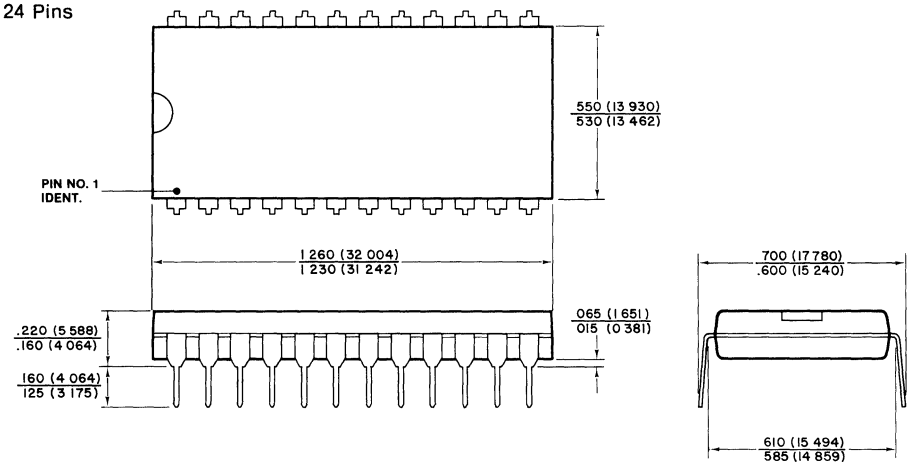


PLASTIC DIP
22 Pins

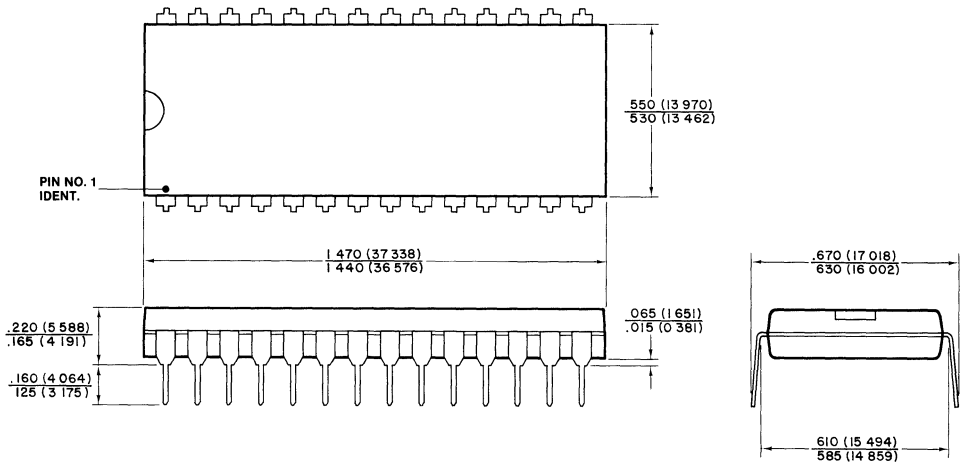


SSI Packaging Diagrams

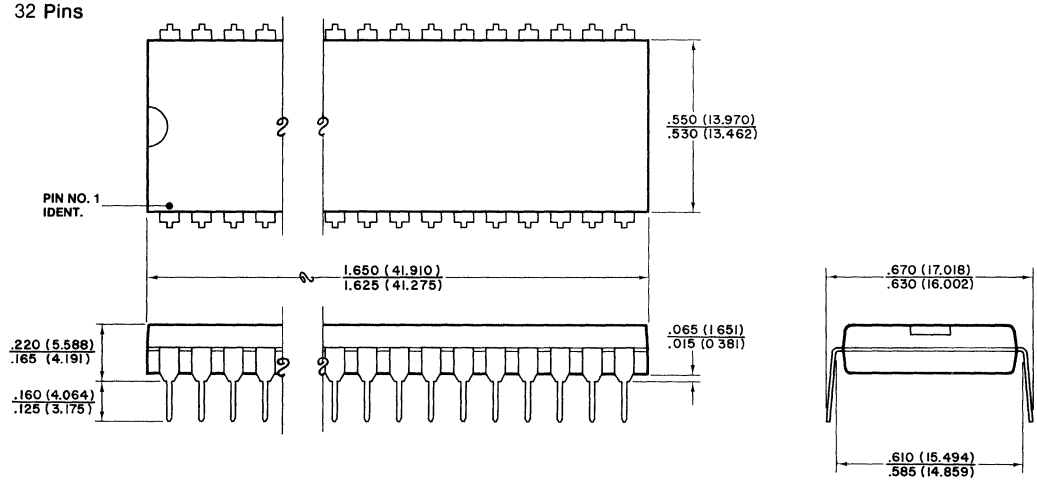
PLASTIC DIP
24 Pins



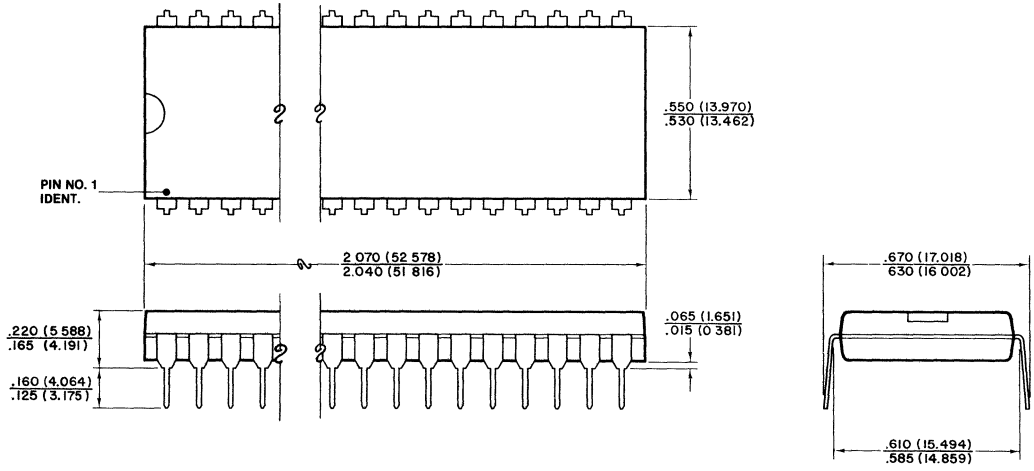
PLASTIC DIP
28 Pins



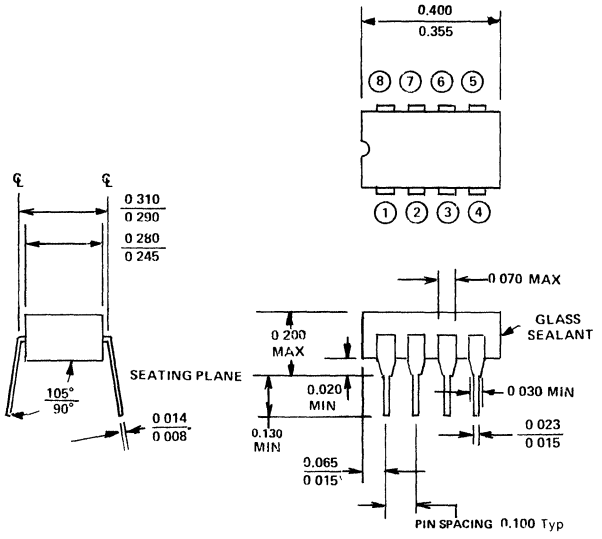
PLASTIC DIP
32 Pins



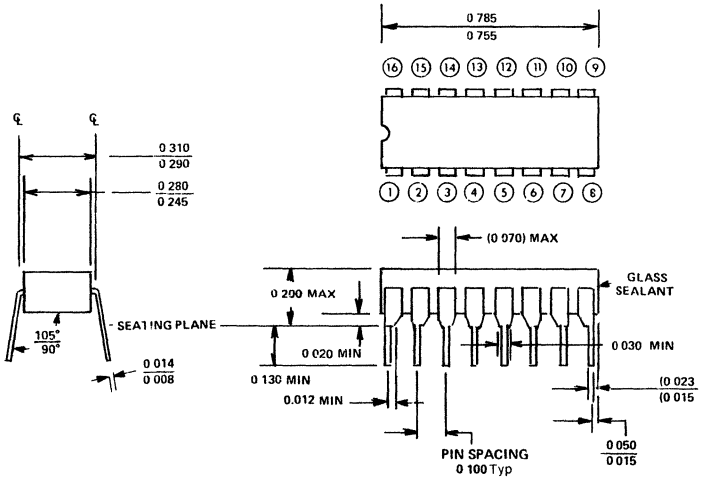
PLASTIC DIP
40 Pins



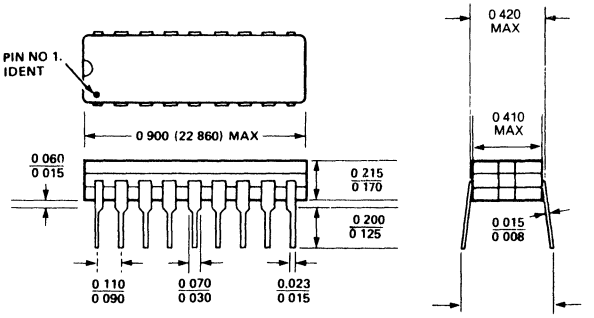
CERDIP
8 Pins



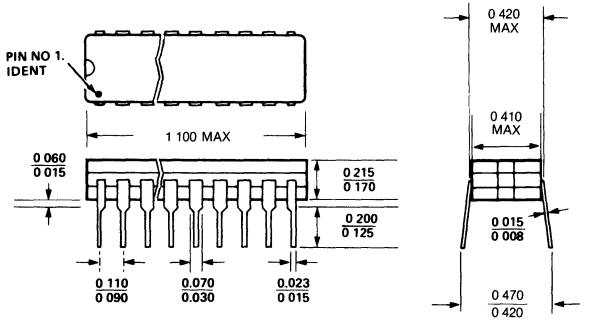
CERDIP
16 Pins



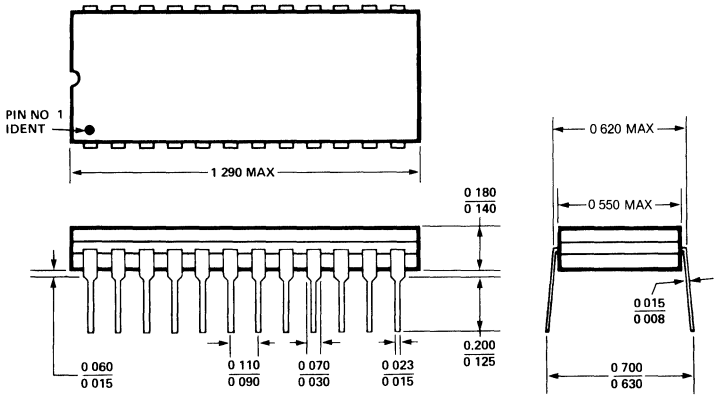
CERDIP
18 Pins



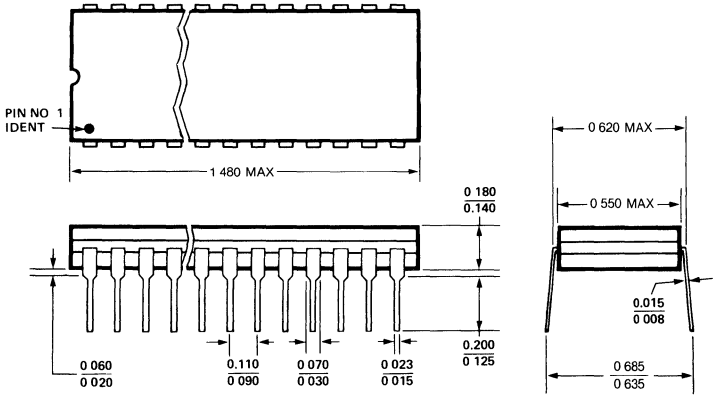
CERDIP
22 Pins



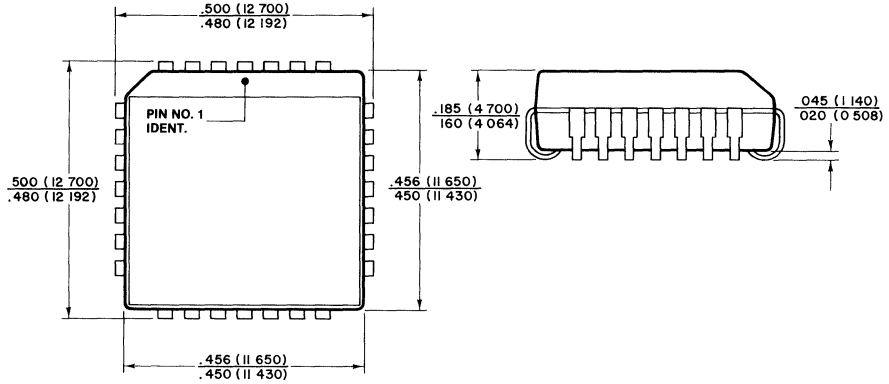
CERDIP
24 Pins



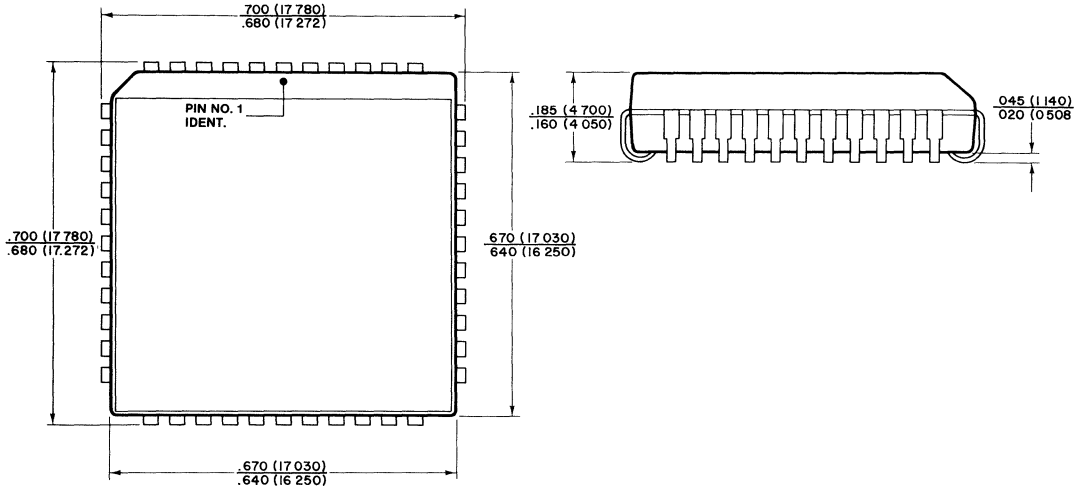
CERDIP
28 Pins



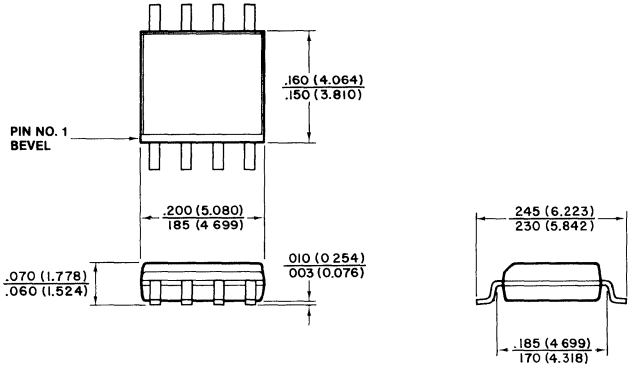
SURFACE MOUNTED
QUAD (PLCC)
28 Leads



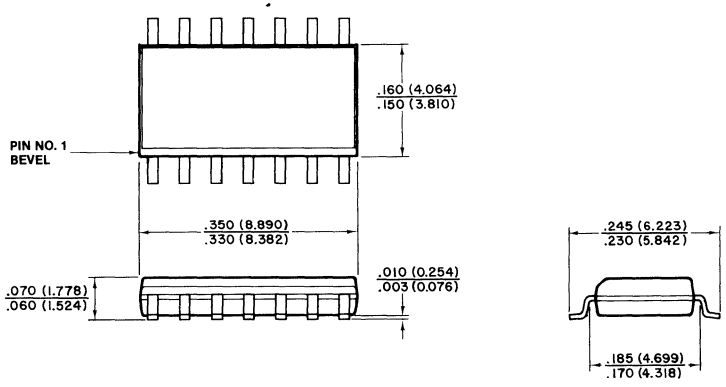
SURFACE MOUNTED
QUAD (PLCC)
44 Leads



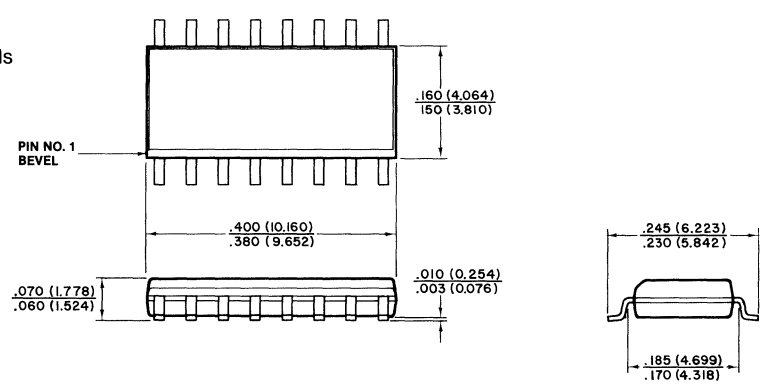
SON
8 Leads



SON
14 Leads

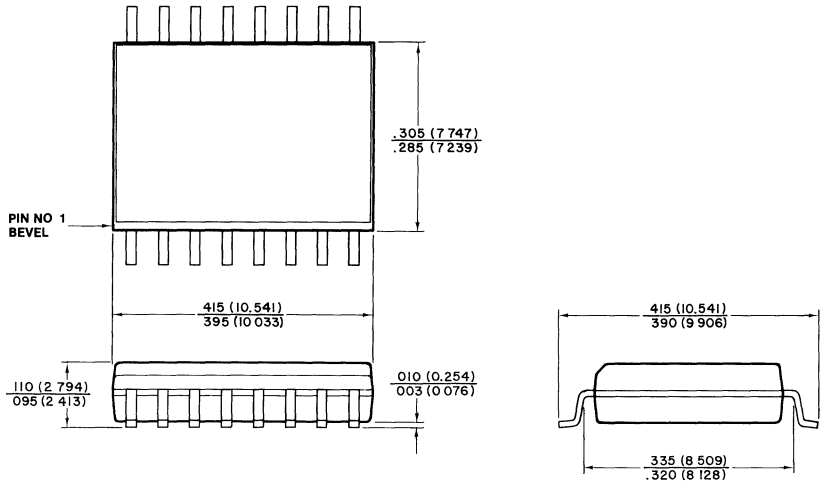


SON
16 Leads

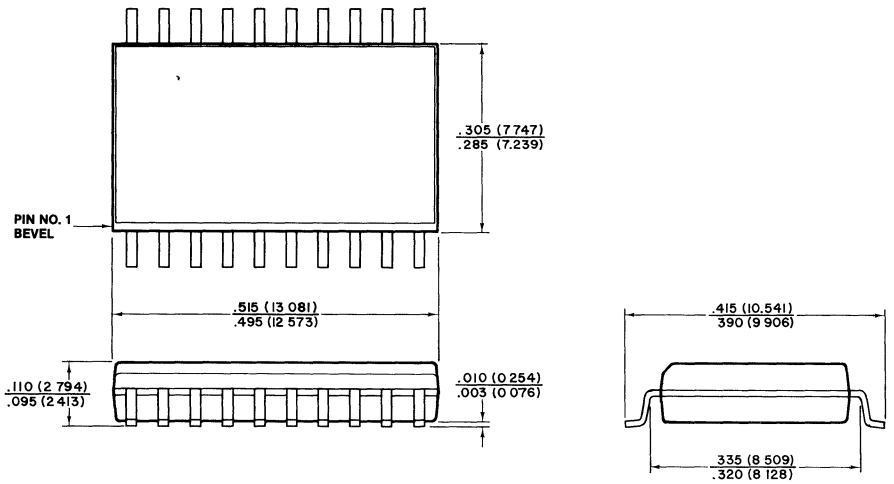


SSI Packaging Diagrams

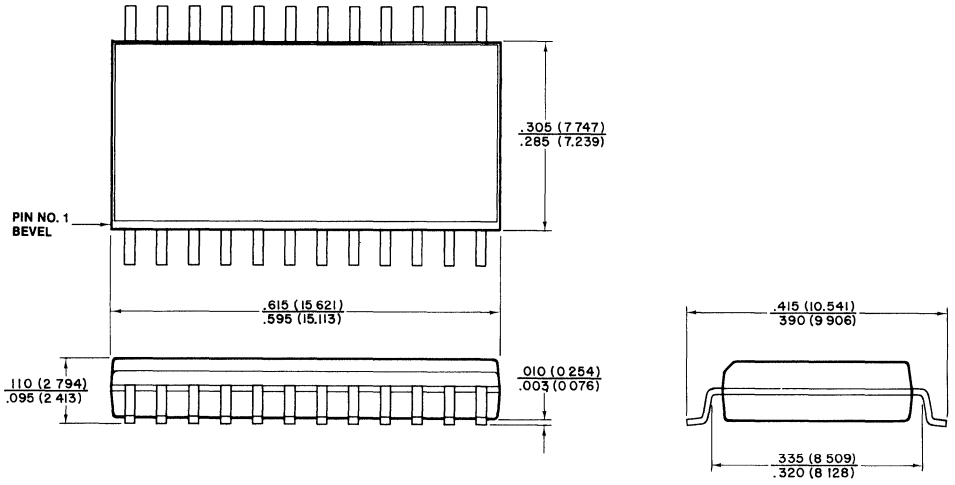
SOL
16 Leads



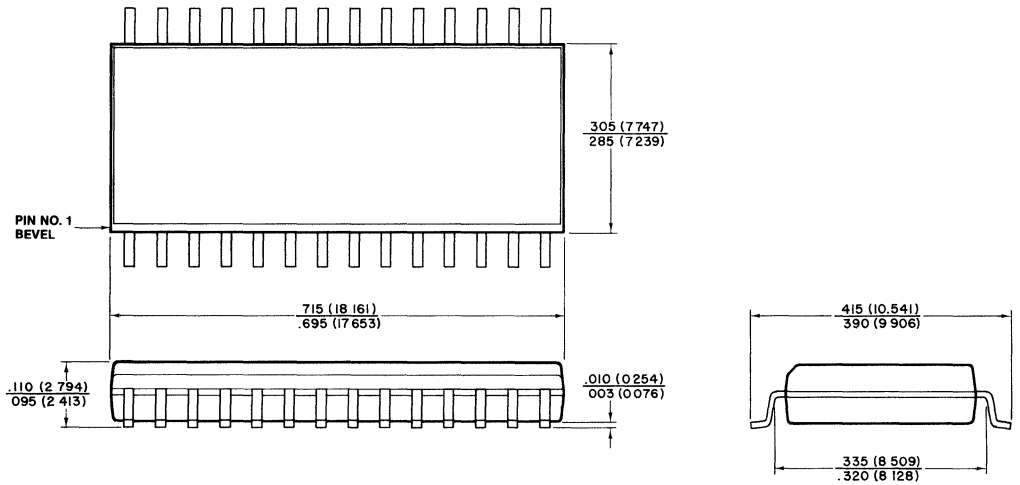
SOL
20 Leads



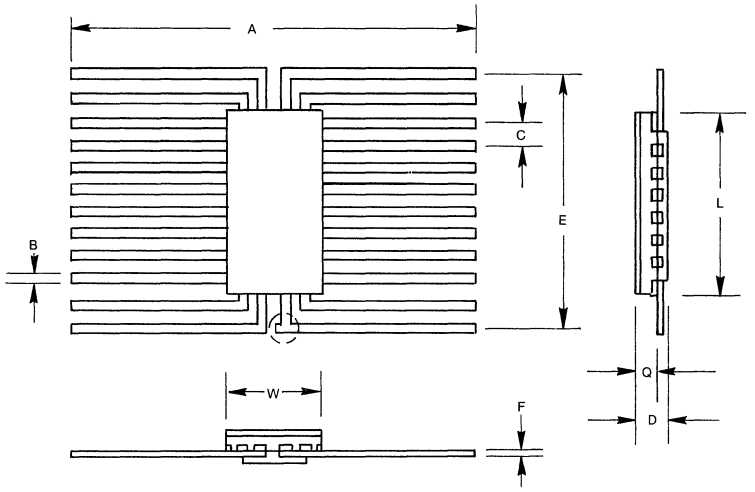
SOL
24 Leads



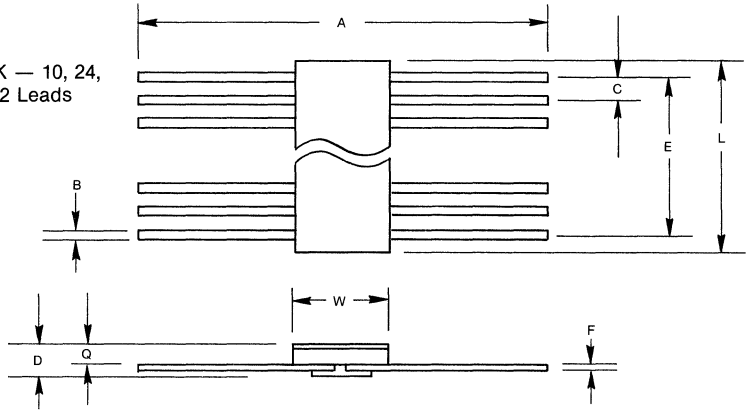
SOL
28 Leads



FLAT PACK
24 Leads



FLAT PACK — 10, 24,
28 and 32 Leads



Pkg. Type	Lead Cnt.	A	B	C	D	E	F	L	Q	W
F	10	.900	.015 .019	.045 .055	.090 max	.200 typ	.004 .007	.250 .260	.074 typ	.250 .260
F	24	.900	.015 .019	.050 typ	.087 max	.567 typ	.002 .004	.391 .405	.075 typ	.264 .276
F	28	1.150	.015 .019	.045 .055	.092 max	.645 .655	.004 .007	.712 .728	.085 .078	.492 .508
F	32	1.150	.015 .019	.045 .055	.092 max	.745 .755	.004 .007	.812 .828	.085 .078	.492 .508

TABLE OF CONTENTS

SECTION 1

A MESSAGE FROM SILICON SYSTEMS' PRESIDENT AND CEO

Quality is the secret to long term success It literally overshadows the short term emphasis on price, delivery, or any other measure of performance

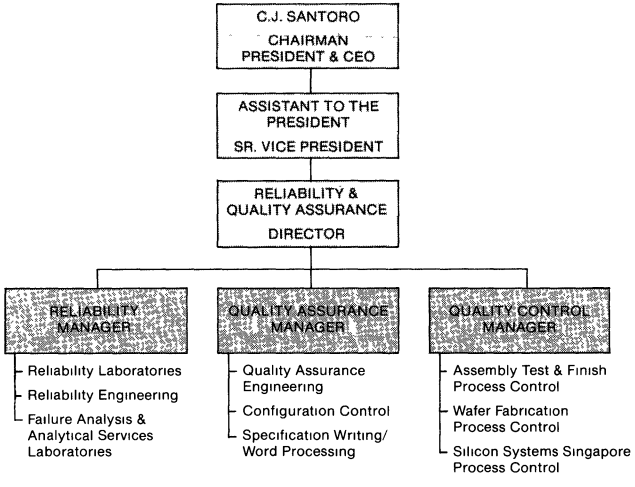
At Silicon Systems, we have based our quality philosophy on the development of a "state of mind" in each employee, related to job performance and to its reflection in the overall level of quality and reliability of our product

You won't hear very many cliches about quality in our environment But we do strive for "zero defects" for "just in time service" and for "doing it right the first time " We think constant reminders of tired phrases can serve more as an irritant than a stimulant Our quality ethic is based on setting examples for others and by intuitive "high quality" job performance propagating the quality ethic throughout the organization to each employee

CARMELO J SANTORO
Chairman, President & CEO

To be sure, we have programs related to quality and reliability They are the subject of this brochure We are dedicated to process control, overall product reliability and outstanding outgoing quality Rapid analysis of failures and returns providing responsive service to our customers also generates quick solutions to our own problems We believe that the high levels which we achieve in quality, reliability and service are directly attributable to belief in the basic tenets of quality within our corporate culture

FIGURE 1.1 ORGANIZATION CHART



1.1 INTRODUCTION

This brochure presents the basic quality and reliability philosophy used by Silicon Systems

Silicon Systems' management philosophy is the manufacture of a quality product consistent with company policy and customer requirements It is the goal of the Quality Assurance and Reliability departments to ensure that these requirements are met

Included in this brochure is Silicon Systems' ongoing program for controlling and improving the quality of devices manufactured

The data clearly illustrates that Silicon Systems is working diligently to maintain its position as a leader in the industry The use of highly specialized equipment, test programs and test procedures allows us to determine product reliability under extreme conditions

Quality is built into Silicon Systems' parts from rigid incoming inspection of piece parts and materials to stringent outgoing quality verification The assembly process flow is encompassed by an elaborate system of test and inspection gates and monitors These gates and monitors ensure a step-by-step adherence to prescribed procedure In this manner, a high level of quality and reliability is produced in all Silicon Systems' products

1.2 QUALITY ASSURANCE AND RELIABILITY

The quality of a semiconductor device is defined by its conformance to specification, the reliability of a semiconductor device is defined by how well it continues to conform to specification over time while under stress This relationship between quality and reliability requires a program that encompasses both Included in this brochure are outlines of our process control program and our PPM (parts-per-million) program These programs assure conformance to specification throughout the manufacturing process

1.2.1 ORGANIZATION PHILOSOPHY

To facilitate the close cooperation and coordination required of the Quality and Reliability functions, a combined organization has been established This organization must have access to and support from the top of the organization The R & Q A organization is shown in Figure 1 1

SECTION 2 QUALITY ASSURANCE

2.1 QUALITY PROGRAM

Quality Assurance has the ultimate responsiblity for the reliable performance of our products This is accomplished through the administration of formal systems which assure that our products meet the requirements of customer purchase orders, and specifications for design, from raw materials through finished product

Quality Assurance supports formal qualifications of suppliers, materials, processes, and products, administration of system and production monitors to assure that our products do meet the desired specifications, and the liaison between Silicon Systems and the customer for all product-related problems

It is the practice of Silicon Systems to have the Quality and Reliability Program encompass all of its activities, starting with a strong commitment of support for the program from the corporate level, and continuing with customer support after the product has been shipped

Silicon Systems firmly believes that quality must be "built into" all of its products by ensuring that employees are trained in the quality philosophy of the company Some of the features built into Silicon Systems' Quality Program include

1 Structured training programs directed at Wafer Fabrication, Test, and Process Control personnel
2 Stringent in-process inspection gates and monitors
3 Total evaluation of designs, materials, and processing procedures
4 Stringent electrical testing (100% and redundant QA AQL testing)
5 Ongoing reliability monitors and process verifications

These structured quality methods result in products which deliver superior performance in the field

2.1.1 LOT ACCEPTANCE TESTING

At Silicon Systems, all sampling for Lot Acceptance Testing is based upon MIL-STD-105D

1 Commercial Testing includes resistance to solvents, Solution A, plus external Visual Inspection to strict SSI standards

2 Industrial Testing includes hermetic-only Destructive Physical Analysis (DPA), as well as Resistance to Solvents, Solutions A and B, plus Solderability, Electrical @ 25°C, and external Visual Inspection to SSI standards

3 Extended Reliability covers hermetic-only DPA and Burn-in, as well as Resistance to Solvents, Solutions A, B, and C, plus Solderability, Fine and Gross Leak Hermeticity, Electrical @ 25°C, and external Visual Inspection to SSI standards

4 High Reliability includes Destructive Physical Analysis and Burn-in, as well as Resistance to Solvents, Solutions A, B, C, and D, plus Solderability, Fine and Gross Leak Hermeticity, Electrical @ max/min temperature limits as well as 25°C, and external Visual Inspection to SSI standards

2.2 PROCESS CONTROL

Silicon Systems' process control program is designed to provide continuous visibility of the performance of manufacturing processes and ensures that corrective action is taken before problems develop

The principal areas of process control which assess the quality of processed product against quality standards are incoming materials inspection and process control monitoring

2.2.1 Incoming Inspections

Incoming inspection plays a very important role in Silicon Systems' quality program Small deviations from material specifications can transverse the entire production cycle before being detected by outgoing quality control By paying strict attention to quality at this early stage, the possibility of failures occurring further down the line is greatly minimized

2.2.2 In-Process Inspections

Every major manufacturing step is followed by an appropriate in-process quality control inspection gate Silicon Systems has established inspection gates in areas such as Wafer Fabrication, Wafer Probe, Prep for Assembly, Assembly, and Final Test areas

In addition to these established gates, Silicon Systems also has established monitors during various stages in the manufacturing process It is this built-in quality that ensures failure-free shipment of Silicon Systems' products

Quality control monitors have been placed throughout the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediate manufacturing steps This data is used to determine quality trends or long term changes in the quality of specific operations A general description of the product flow and QC inspection points are shown in Figure 2 2

2.3 PPM PROGRAM

The main purpose of employing a PPM program is to eliminate defects The action portion of this program is accomplished in three stages

1 Identify all defects by failure mode
2 Identify defect causes and initiate corrective action
3 Measure results and set improved goals

The data generated from an established PPM program is statistically compiled as a ratio of units rejected/tested This ratio is then expressed in terms of parts per million (PPM) with a confidence limit attached The eventual reported PPM result therefore allows proper significance to be attached to every defect found The final aim or goal is to achieve and maintain zero defects

Based on significantly large volumes of PPM data and an established five-year strategic plan identifying industry-wide competitive PPM goals, Silicon Systems has progressively achieved excellent quality standards and will continue to measure the results and, therefore, improve on PPM standards as set by the industry

FIGURE 2.1 AOQ TRENDS

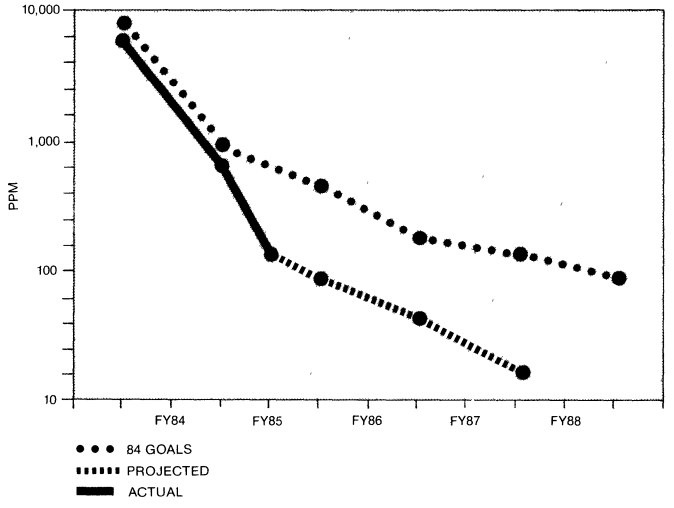
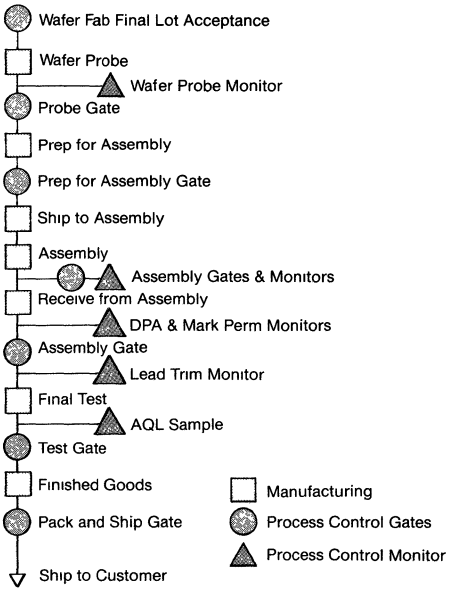


FIGURE 2.2
PROCESS CONTROL GATES AND MONITORS



2.4 COMPUTER AIDED MANUFACTURING CONTROL

Computer Aided Manufacturing (CAM) requires the identification, control, collection and dissemination of vast amounts of data for logistics control. Silicon Systems uses this type of computerized system for statistical process control and manufacturing monitoring

PROMIS (Process Management and Information System) displays document control-released recipes, processes, and procedures, tracks work-in-process, contains accurate inventory information, allows continuous recording of facilities data, contains performance analysis capabilities, and much more PROMIS allows for a paperless facility, which assists in keeping contamination out of the wafer fab clean room

The configuration of PROMIS has been tailored to meet the requirements of Silicon Systems

2.5 GUARANTEED AQL

Silicon Systems currently offers a guaranteed AQL level of 0 05% and has a written plan to implement a guaranteed AQL of 0 01% in 1987

Our PPM program, which allows us to guarantee the AQLs, is key to the continuing improvement in our average outgoing quality AOQ, see Figure 2 1 This program encompasses the ongoing analysis of our product and process performance to continually reduce our process defect densities The ultimate goal of this program is improvement toward zero defects, rather than the acceptance of a given defect density level as an ultimate goal

SECTION 3 RELIABILITY

3.1 RELIABILITY PROGRAM

Silicon Systems' reliability is ensured through continuous monitoring of generic product families

The reliability program includes several highly specialized areas which are equipped with a variety of analytical capabilities

a Scanning Electron Microscope (SEM)
   - Energy Dispersive X-Ray (EDX)
   - Voltage Contrast
   - Electron Beam Induced Current (EBIC)

b Electrical Characterization

c Metallurgical Cross-Sectioning

d Ion Chromatograph

e Micromanipulator Probe Station

f Wet Chemical and Plasma Techniques

g Macro/Microphotography

h X-Ray Techniques

These capabilities allow the prompt and accurate analysis of failure mechanisms

3.2 RELIABILITY METHODS

Various stress tests are utilized that define performance levels of our products Many of these stress tests are per Mil-883 as shown in Table 3 1.

3.3 FAILURE ANALYSIS PROGRAM

A highly visible comprehensive failure reporting, analysis, and corrective action program is extremely important to the continued achievement of high reliability in components produced by Silicon Systems

This detailed failure analysis program is an integral part of every phase of device technology from initial product design review to analysis of our product under actual field use conditions

TABLE 3.1 RELIABILITY STRESS TESTS

TEST	METHODS
Biased Humidity	85°C/85°% RH
Operating Life	Mil-883C, method 1004
Steam Pressure	121°C/15 PSI
Temperature Cycling	Mil-883C, method 1010
Thermal Shock	Mil-883C, method 1011
Salt Atmosphere	Mil-883C, method 1009
Constant Acceleration	Mil-883C, method 2001
Mechanical Shock	Mil-883C, method 2002
Solderability	Mil-883C, method 2003
Lead Integrity	Mil-883C, method 2004
Vibration, Variance Frequency	Mil-883C, method 2007
Thermal Resistance	Silicon System
Electrostatic Damage	Silicon Systems

The failure analysis data generated is used to help our customers implement improved device applications and to allow Silicon Systems to identify and implement product or process improvements

Conclusively, this in-house testing and analysis allows Silicon Systems to monitor all aspects of manufacturing to ensure that a product of highest quality is shipped to our customers

FIGURE 3.1
TYPICAL FAILURE RATIO CURVE

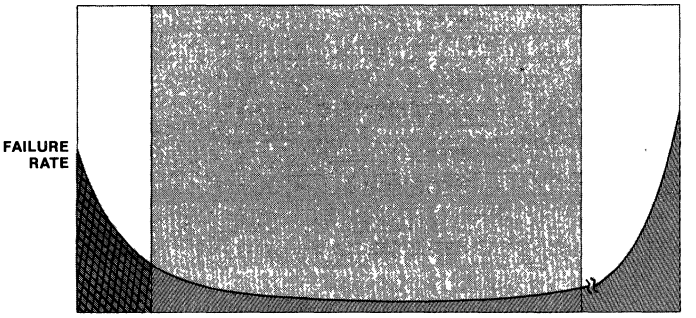


TABLE 3.2
RELIABILITY DATA BASE
Failure Rates in %/1000 Hours[1]

Product Type	Device Hours (10^6)	Number Failed	55°C[2] 60% Confidence Level	FITS
Bipolar	5.424	28	.006	60
CMOS	3.720	89	.029	290
Computer Product	5.424	28	.006	60
Telecom Product	3.720	89	.029	290

Note
1. 01%/1000 hours = 1000 FIT, failure rates are quoted with 60% confidence level
2. 55° C number assume an activation energy of 0 71 eV

TABLE 3.3
ACTIVATION ENERGIES OF MAJOR FAILURE MECHANISMS

Failure Mechanisms	Activation Energy (eV)
Surface Inversion Failures	1.02
Au-Al Intermetallic Bond Failures	1.02-1.04
MOS V_{TH} Shift	1.0-1.6
Aluminum Electro Migration	0.4-0.8
MOS Surface Charge Accumulation	1.2-1.35
Corrosion of Metallization	0.3-0.6
Ion Migration	1.4
Slow Trapping	1.0
Die Surface Charge Spread	0.5-1.0
Oxide Defects	0.3

3.4 RELIABILITY PREDICTION METHODOLOGY

It has been established through Reliability Engineering principles that the failure rate of a group of devices as a function of time will endorse a life curve as shown in Figure 3 1

Basically, the bath tub curve in Figure 3 1, implies that the useful life of the product extends until some basic design or material limitation is experienced At Silicon Systems, the Arrhenius model is used to extrapolate a failure rate at an accelerated temperature test condition to a normal use temperature condition

Silicon Systems uses the Arrhenius equation concept to determine unique failure mechanisms and as a base line for defining the reliability of integrated circuits

The Arrhenius equation for validity requires the following

1 The stress remain constant
2 Activation energy remain constant with temperature
3 The mass remain constant

The model basically states $R = A\, e^{-E_a/KT}$

where R = Reaction rate constant
A = Constant
E_a = Activation energy (eV)
K = Boltzmann's constant 8 63 x 10^{-5} eV/°K
T = Absolute temperature (°K)

SECTION 4 ELECTROSTATIC DISCHARGE PROGRAM

4.1 ESD PREVENTION

Silicon Systems recognizes that procedures for the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity must be incorporated throughout all operations which come in contact with these devices

Silicon Systems' quality program incorporates various protection measures for the control of ESD Some of these preventive measures include handling of parts at static safe-guarded work stations, the wearing of wrist straps during all handling operations, the use of conductive lab coats in all test areas and areas which handle parts, and the packaging of components in conductive and anti-static containers

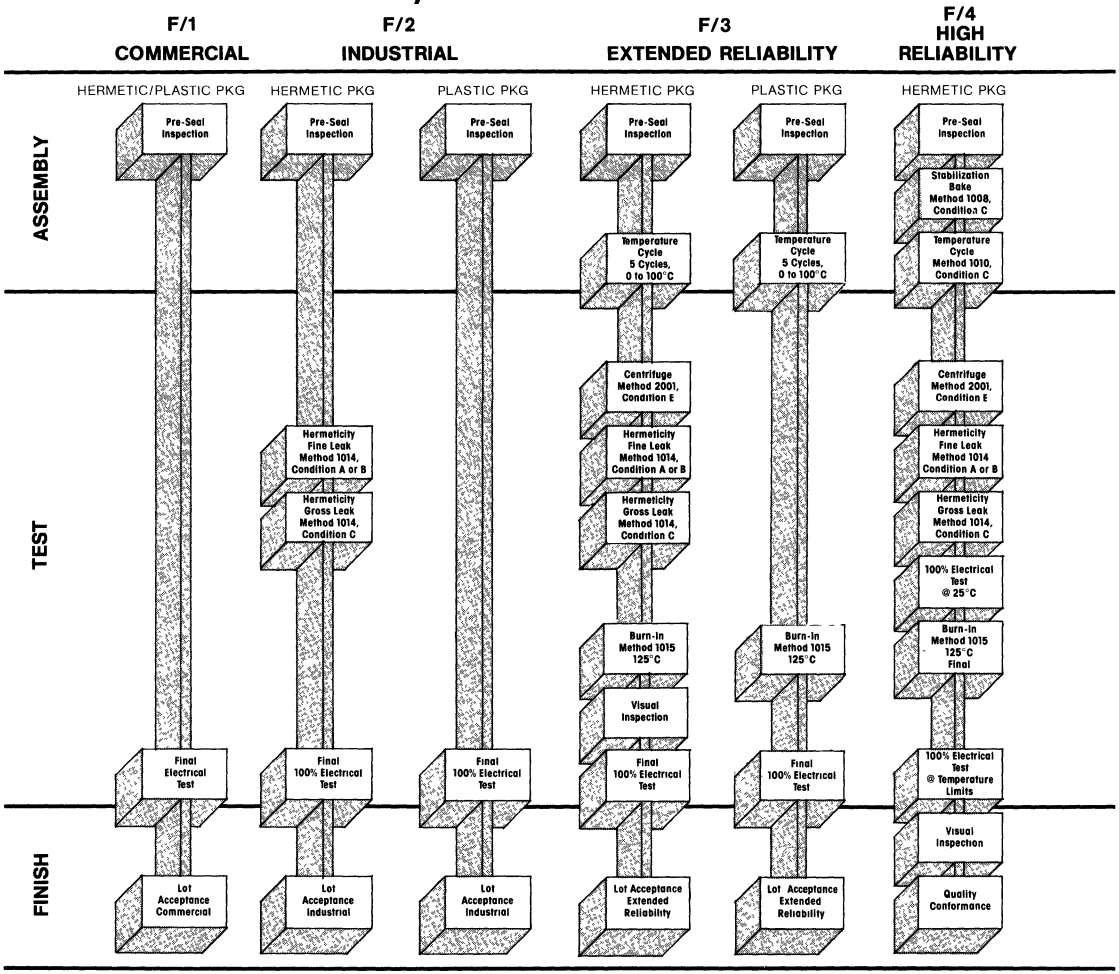
TABLE 3.4
FAILURE MECHANISMS AND DEFECTS

Electrical Failure Mode	Possible Defects	Corrective Action Area
Open	Poor Wire Bonding	Bonding Process
	Incomplete Metallization	Evaporation Process
	Misplaced Bond	Bonding Process
	Metal Migration	Design/Layout
Short	Misplaced Bond	Bonding Process
	Metal Migration	Design/Layout
	Particle Contamination	Surface Passivation
	Moisture Penetration	Surface Passivation or Packaging
	Gate/Junction Short	Protection Diode Design or High Voltage Device Design
	Lead Short	Packaging
	Oxide Film Imperfection	Oxide Film Process
	Mask Misalignment	Photolithographic Process
Degradation	Moisture Penetration	Surface Passivation or Packaging
	Gate/Junction Short	Protection Diode Design or High Voltage Device Design
	Lead Short	Packaging
	Parasitic Transistor	Design/Layout
	Oxide Film Imperfection	Oxide Film Process
	Channeling	Design/Layout, Oxide Film Process, or Surface Processing
	Mask Misalignment	Photolithographic Process
	Surface Contamination	Surface Processing or Environmental Control

TABLE 3.5
RELATIONSHIP BETWEEN FAILURE CAUSES AND ANALYTICAL TEST METHODS

FAILURE CAUSE / TEST	Solderability (2003.2)	Temp. Cycling (1010.2)	Thermal Shock (1011.2)	Constant Acceleration (2001.2)	Mechanical Shock (2002.2)	Vibration, Variable Frequency (2007.1)	Lead Fatigue (2004.2)	Barometric Pressure Reduced (1001)	Moisture Resistance (1004.2)	Salt Atmosphere (1009.2)	Vibration Fatigue (2005.1)	Vibration Noise (2006.1)
Bond Integrity (Chip or Wire)		●	●	●	●	●					●	●
Cracked Chip		●	●		●							●
Internal Structural Defect					●	●						
Contamination-/Contact-Induced Short		●		●	●	●					●	●
Wire or Chip Breakage				●	●	●					●	
Glass Crack	●	●	●		●		●	●				
Lead Fatigue							●					
Contamination of Package Elements	●	●	●									●
Thermal Fatigue		●										
Seal Integrity		●										
Seal Contamination				●	●	●						●
Leakage		●	●				●	●	●	●		
Package/Material Integrity	●	●	●		●			●	●	●		

Quality Assurance Flow Chart



Although full compliance with MIL-STD-883 is not implied, all processes are in accordance with or derived from the methods indicated

LOT ACCEPTANCE TESTING
At Silicon Systems, all sampling for Lot Acceptance Testing is based upon MIL-STD-105D.

Commercial Testing includes resistance to solvents, Solution A, plus external Visual Inspection to strict SSi standards.

Industrial Testing includes hermetic-only Destructive Physical Analysis (DPA), as well as Resistance to Solvents, Solutions A and B, plus Solderability, Electrical @ 25°C, and external Visual Inspection to SSi standards.

Extended Reliability covers hermetic-only DPA and Burn-in, as well as Resistance to Solvents, Solutions A, B, and C, plus Solderability, Fine and Gross Leak Hermeticity, Electrical @ max/min and 25°C, and external Visual Inspection to SSi standards.

High Reliability includes Destructive Physical Analysis and Burn-in, as well as Resistance to Solvents, Solutions A, B, C, and D, plus Solderability, Fine and Gross Leak Hermeticity, Electrical @ max/min and 25°C, and external Visual Inspection to SSi standards.

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